96768600

CONTROL DATA

CDC® MOS MEMORY SUBSYSTEM

AT241, AT275, BA212, DT223

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OPERATION
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MAINTENANCE
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HARDWARE REFERENCE/MAINTENANCE MANUAL

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A (6/76)	Manual released.
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E (10/83)	Manual revised; includes ECO DS022294, providing a new memory interface/address PWA to correct artwork errors.
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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCO'S	COMMENTS
AT241-B	01		
AT275-B	01		
BA212-A	08	DS22294	
	09		
DT223-B	01		

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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4-66	C	6-1	C		
4-67 thru 4-71	A	7-1/7-2	C		
5-1	C	7-3/7-4	C		
5-2 thru 5-5	B	7-5 thru 7-10	C		
5-6 thru 5-9	A	7-10.1	F		
5-10	B	7-10.2 thru 7-10.6	C		
5-11 thru 5-16	A	7-11	F		
5-17	C	7-12/7-13	C		
5-18/5-19	A	7-14	F		
5-20	B	7-15 thru 7-18	C		
5-21	A	7-19	F		
5-22	C	7-20 thru 7-22	E		
5-23 thru 5-27	A	7-22.1	F		
5-28	C	7-22.2 thru 7-22.6	E		
5-29	A	7-23	E		
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PREFACE

This manual contains general descriptions, theory of operation, diagrams, maintenance data, parts lists and spare parts lists for the Control Data ® CYBER 18 MOS memory subsystem. Although designed for use in the standard CYBER 18 product line, the equivalent to the subsystem components are also used in various quoted special equipments (QSEs) which utilize the basic micro-programmable processor. The subsystem may consist of one or more of the following: AT275-B 16K MOS Memory Array, AA241-B 32K MOS Memory Array, BA212-A Main Memory Interface (Address/Control and Data), and DT223-B Error Checking and Correction Array.

Information contained in this manual is intended for use by maintenance personnel in training and in the field with a minimum of six months field-related experience.

The publications listed below provide additional information on the MOS memory and memory interface. These publications are available through Literature and Distribution Services (LDS) or the nearest Control Data Corporation sales office.

Publication	Publication No.
AA132, AA133, AA153, AA155 CYBER 18 Processor with MOS Memory Field Print Package Manual	60475100
AA132, AA133, AA153, DT120, FC402 CYBER 18 Computer Systems Central Processor Field Repair Guide	60475001
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
CYBER 18 Computer Systems Overview Manual	60475000
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
DT120, DT195, FC402 Breakpoint Controller and Breakpoint Panel Hardware Reference/Maintenance Manual	96729000

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FIGURES

TABLES

GENERAL DESCRIPTION 1

This section provides a brief description of the elements that comprise the MOS memory subsystem and the available subystem structures.

SUBSYSTEM COMPONENTS

The MOS memory consists of a data interface card, an address and control interface card, and from one to four memory arrays - one of which may be an ECC (error checking and correction) array. All cards are standard 11 x 14 inch circuit boards, and each requires one card space in the microprocessor chassis. Two memory banks may be coupled together to double total memory size.

The address and control interface card supplies timing and control for the MOS memory, and processes memory requests and addresses from the CPU and peripheral devices. The data interface card provides interfacing for the write data inputs and read data outputs.

The memory arrays are available on either 16K word or 32K word cards, for a total of 131K possible memory words in a four-card bank. The word size is 18 bits, which includes a 16-bit data word, a parity bit, and a protect bit. The total memory capacity with two banks is 262K words.

The memory array and interface cards operate on system power, are cooled by fans located in the processor chassis, and operate under the same environmental conditions.

MOS MEMORY SIZE AND CAPABILITY

The MOS main memory (figure 1-1) is configured as a one-bank, two-port memory that may be expanded to create a two-bank, three-port memory system. Each MOS bank provides from 16K to 131K 18-bit words of storage without error correction, and from 16K to 98K of storage with error correction. The two banks are referred to as local and external banks. Each bank may have only one memory request active at one time. However, each bank operates independently, thus permitting concurrent access by different ports to each bank. Each of the three ports in each bank (local CPU, local DMA and external) has independent address and data control paths to and from memory and may request memory independently of any operation currently in progress on another port.

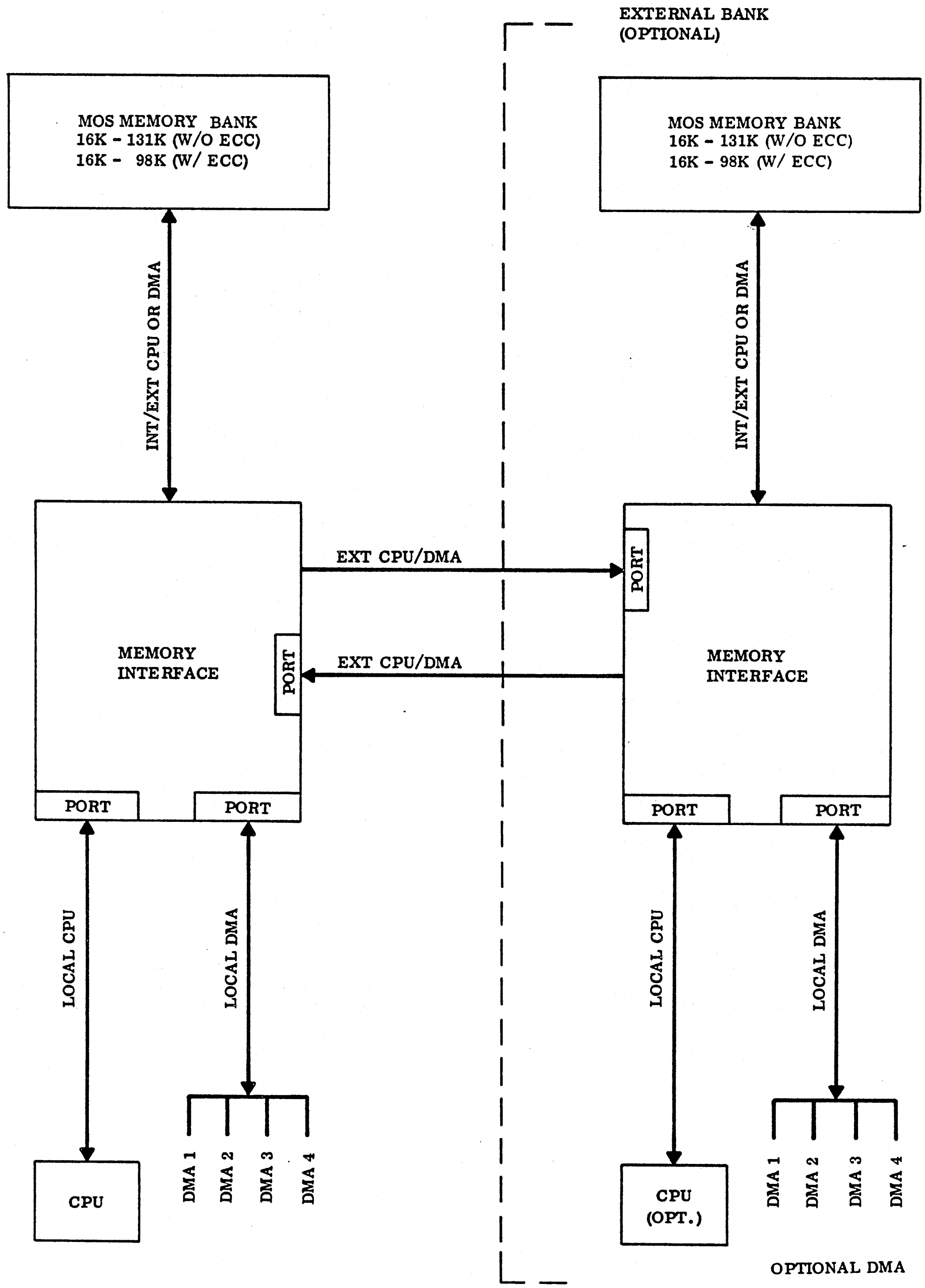


Figure 1-1. MOS Main Memory Configuration

OPERATION 2

There is no operation or programming information applicable to this equipment.

INSTALLATION 3

Installation information for the MOS memory subsystem is contained in the CYBER 18 Computer Systems with MOS Memory Installation Manual.

THEORY OF OPERATION 4

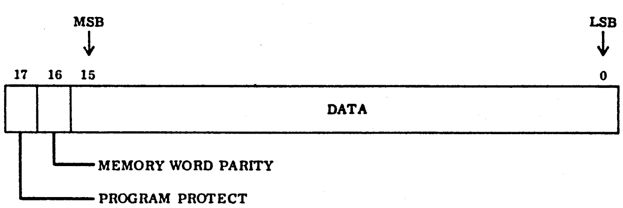
This section contains a functional description of the MOS memory and interface. The description is related to the diagrams in section 5. Other illustrations are presented throughout this section.

ADDRESS, CONTROL AND DATA FLOW

The MOS memory is a one-bank, two-port memory that may be expanded to create a two-bank, three-port memory system. It consists of a data interface, an address and control interface, and from one to four memory arrays. The three ports permit three independent data, address, and control paths to the memory. Any port may request a memory cycle at any time, but only one memory reference can occur at one time. Priority selection and multiplexing of concurrent requests is accomplished by the MOS memory. One port is used by the central processing unit (CPU); the second port is shared by four direct memory access (DMA) subports; the third port is used as a dual bidirectional interface with a second MOS memory bank. The simplified block diagram in figure 4-1 shows the address and data paths.

After priority selection, memory addresses from the CPU, DMA or external ports are decoded to determine a word location in the memory array. Either the CPU or a DMA device may request an external bank address according to the address formats described later in this section.

The memory array for each bank consists of from one to four array boards, each containing either 16K or 32K words of storage, for a total of from 16K to 131K words. Each word contains 18 bits, according to the data format shown below. The word parity and protect bits are described later in this section.



An ECC array may be substituted for one of the array boards. This adds five check bits to each memory data word and restricts the total memory capacity of a bank to 98K words.

A MOS memory cycle can consist of a read operation, a write operation, or both a read and a write operation. MOS memory circuits also require a refresh operation on all row addresses at least each two milliseconds to retain stored data.

During a read operation, data leaves the addressed location in the MOS memory array to the data interface. There the read data is checked for parity and, if an ECC board is employed, single bit errors detected and corrected; the data is then directed to the requesting port. If an external bank was selected, data is accessed from the external port of the external bank by the external port of the local bank, and then directed to the requesting CPU or DMA port.

During a write operation, write data from the requesting port is checked for parity and the appropriate parity bit is generated. If the ECC option is included, a five-bit ECC code is also generated from the word contents. The resulting 18 or 23 bits are sent to the memory array.

A split cycle (read followed by a write operation) is employed when requested by the device requesting a read/modify/write memory cycle; or whenever a normal protected write cycle is requested; or when a character (half word) write cycle is requested. On a requested read/modify/write cycle, memory activity stops between read and write portions of the cycle except for refresh requests. On a protected write cycle, the write portion of the cycle may be aborted if a protect fault is encountered. On a character write cycle, one of the characters read from memory is combined with the new character to be stored in the write portion of the cycle.

INTERFACE SIGNALS

The MOS memory interconnecting diagrams, figures 5-1 through 5-4, show all data, address, and control

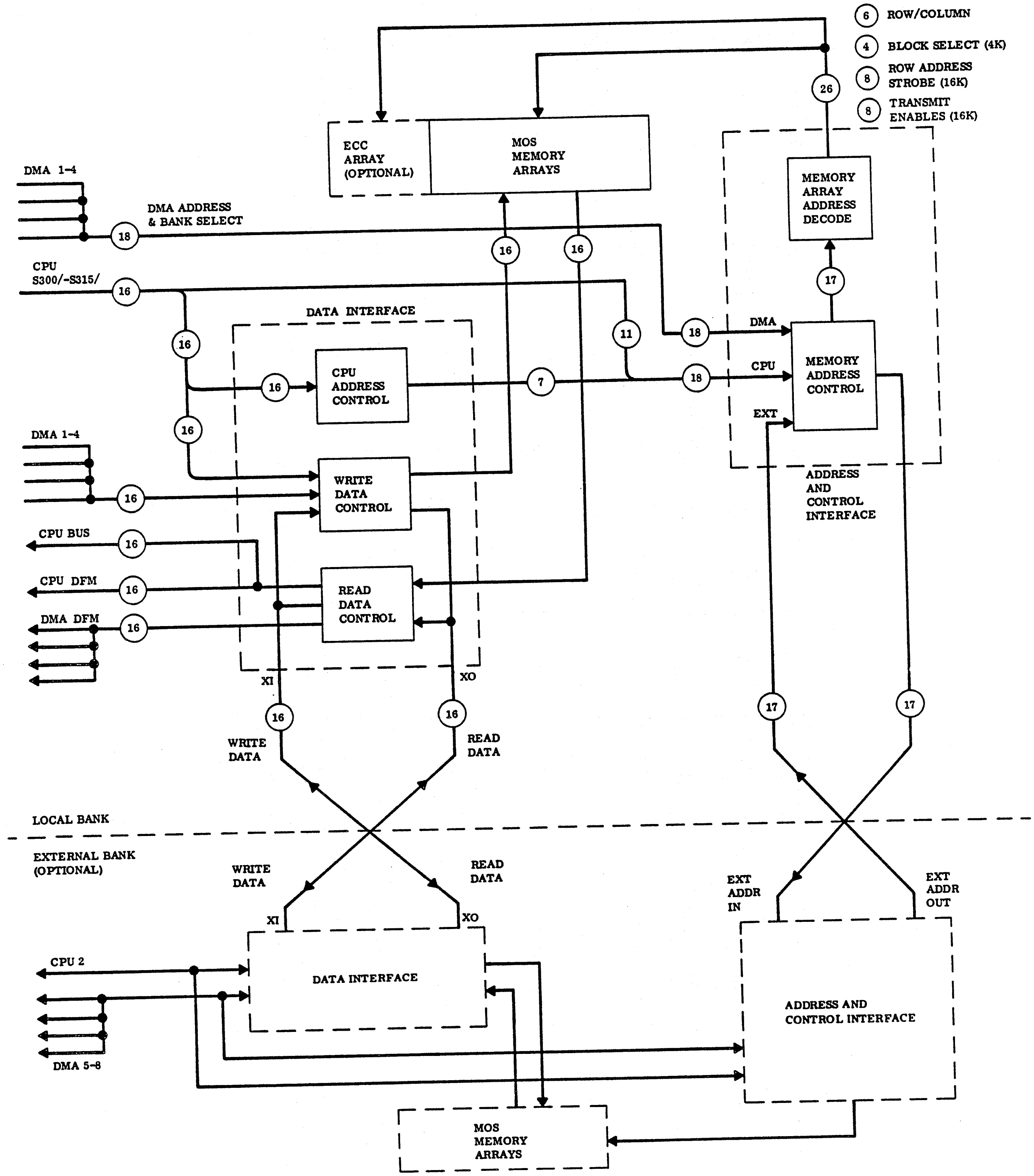


Figure 4-1. MOS Memory Address and Data Paths

lines associated with the data interface, address and control interface, and memory array boards. These diagrams include all origins, destinations, and pin numbers. Address and data paths are highlighted to provide a cross reference to figure 4-1. The functional relationship of these signals is shown in the functional block diagrams in section 5. A functional description of the block diagrams is provided later in this section. Tables 4-1 through 4-4 provide a brief description of each interface signal.

ADDRESS PATHS

CPU Port to Memory Array

The CPU transmits both the memory address and write data over a 16-bit (S300/ through S315/) multipurpose path. Within the MOS memory, the address path taken depends upon the control signals from the CPU to the address and control interface.

- Absolute addressing — The 16-bit path may be used to directly address the first 65K words in memory. The most significant five bits, S304/ through S300/ (MSB), are latched into the CPU address register in the data interface and are available to the address and control interface as lines CPUMAB12/ through CPUMAB16/. The least significant 11 bits, S315/ (LSB) through S305/, are latched into the CPU address register in the address and control interface.

  As the priority select circuits accept the CPU memory request, the 16-bit address is decoded to form the row address, column address, block select, and row address strobe as shown in figure 4-2.

  Since bit 17 of the CPU memory address does not exist, local memory beyond the first 65K words is not accessible with this addressing method. CPU absolute addressing also cannot be used to access the external bank.

- Bounds address loading — The path S300/ through S315/ is utilized to load either the 16-bit lower bounds register or the 16-bit upper bounds register in the data interface. These two registers set the upper and lower boundaries of the unprotected memory area available to the CPU, and a limit comparison is made each time a CPU address is loaded.

- Page mode addressing — In this indirect addressing method the least significant 11 bits of the path, S315/ through S305/, are strobed into the CPU address register in the address and control interface as in absolute addressing, and are used to form the least significant 11 bits of the memory address. However, the upper six bits plus the

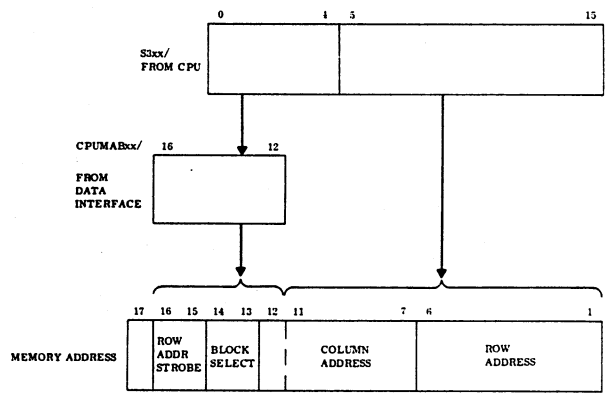


Figure 4-2. CPU Absolute Addressing

TABLE 4-1. MOS MEMORY INTERFACE SIGNALS: CPU

Signal	Source†	Dest.†	Description
BUSxx	D	CPU	Data output lines 00(MSB) through 15 to CPU three-state bus.
CHAR0 CHAR1	CPU	A	Write character 0 or character 1. Enables S300/ through S307/ or S308/ through S315/, respectively, into memory during a write cycle.
CPUBKPWRT	A	Brkpt Contrlr	Signal to breakpoint controller to enable OPERAND breakpoint compare.
CPUDFMxx	D	CPU	CPU data output lines 01 through 16 (MSB) from memory. May also contain breakpoint address.
CPUMDS/	A	CPU	Memory data resume. Read data from memory is available to the CPU
CPU PROTECT/	CPU	A	Program protect line. Indicates the protect status of a CPU operation.
CPU-REQ/	CPU	A	Memory request. Requests a memory cycle.
CPU-SC/	CPU	A	Split cycle request. Requests the read portion of a read/modify/write cycle.
CPU WRITE	CPU	A	Read/write control. On a read/modify/write cycle, requests write portion.
CPU WRTPB	CPU	A	Protect bit enable. Directs protect control to write protect bit (bit 17) into memory.
ENMEMBUS/	CPU	D	Enables memory data to lines BUS00 through BUS15.
ENPRTSYS	CPU	A, D	Enable protect system line. Overrides normal protect system when false.
EVENPAR	D	CPU	Word parity status line. Shows even number of 1 bits in word stored in memory during a write cycle. Does not include protect or ECC bits.
GATEAB/	CPU	A, D	Memory address enable. Loads S300/ through S315/ into the memory address register.
GATELBDS/	CPU	D	Lower bound enable. Loads S300/ through S315/ into the lower bounds register. Selects ECC status to CPUDFMxx lines if MIR28' is true.
GATEUBDS/	CPU	D	Upper bound enable. Loads S300/ through S315/ into the upper bounds register. Enables loading of memory page file if MIR28' is true. Enables loading of address mode register if MIR29' is true.
MC/	CPU	A, D	Master clear. Resets latches.
MEMPROTBT/	D	CPU	Memory protect bit status. Same as memory bit 17 except always false if a CPU operation is in bounds.

†A: Address and control interface
D: Data interface

TABLE 4-1. MOS MEMORY INTERFACE SIGNALS: CPU (Continued)

Signal	Source†	Dest.†	Description
MIRxx'	CPU	D	Inputs from CPU micro instruction register bits 28 through 31. MIR28' enables loading of memory page file or ECC status outputs. MIR29' enables loading of the AMR register, MIR30' selects page mode operation, and MIR31' selects program files when loaded into the AMR register.
MULTIND	CPU	D	Multilevel indirect mode line. When true, inhibits the use of the most significant address bit from line S300/.
PAGE MODE/	D	CPU	Page mode status line indicating memory is operating in page mode when line is true.
PGM FILES/	D	CPU	Status line indicating the upper half (program files) of the memory page file has been selected.
ROPINT/	D	CPU	Read only page interrupt. Write attempt made into a read only page.
S300/ - S315/	CPU	A, D	Multipurpose path from the CPU, used for data and addresses.
SEC STATUS/	D	CPU	Status line indicating a single bit error was detected and corrected (with ECC only).
SET SM 105/	A	CPU	Program protect fault line. Write attempt made to a protected location.
SET SM 108/	A	CPU	Parity error status line. Indicates a parity error (no ECC) or a double error (with ECC) in read data.
STBCPUBKP/	A	CPU	Strobe line to CPU panel interface to compare breakpoint address. Sets CPU status latch SM104.
T0/, T0'/ T2 ODDCLK/ T3-$\overline{\text{MEM}}$/	CPU	A, D	Timing signals from CPU.

†A: Address and control interface
D: Date interface

TABLE 4-2. MOS MEMORY INTERFACE SIGNALS: DMA

Signal	Source†	Dest.†	Description
DMACHAR0 DMACHAR1	DMA	A	Write character 0 or character 1. Enables DMAD09/ through DMAD16/ or DMAD01/ through DMAD08/, respectively, into memory during a write cycle.
DMADxx/	DMA	D	Write data lines 01 through 16.
DMADFMxx	D	DMA	DMA data output lines 01 through 16 from memory.
DMAMABxx/	DMA	A	Address lines 01 through 17.
DMAMAE/	A	DMA	Memory address error. Nonexistent external bank selected.
DMAMDS/	A	DMA	Memory data resume. Read data from memory is available to the DMA.
DMAMPB/	D	DMA	Memory protect bit status. Same as memory bit 17.
DMAMPE/	A	DMA	Parity error status line. Indicates a parity error (no ECC) or a double error (with ECC) in read data.
DMAMPL/	D	DMA	Word parity status line. Shows even number of 1 bits in word stored in memory during a write cycle. Does not include protect or ECC bits.
DMAPROT/	DMA	A	Program protect line. Indicates the protect status of a DMA operation.
DMA-PF/	A	DMA	Program protect fault line. Write attempt made to a protected location.
DMA-SC/	DMA	A	Read/modify/write request. Requests the read portion of a read/modify/write cycle.
DMA WRITE	DMA	A	Read/write control. On a read/modify/write cycle, requests write portion.
DMA-WRTPB/	DMA	A	Protect bit enable. Directs protect control to write protect bit (bit 17) into memory.
DMAx-INT	DMA	A	Local bank request from individual DMA device (1 through 4). False selects external bank.
DMAx-MR/	DMA	A	Memory request from individual DMA device (1 through 4).
DMAx-RA/	A	DMA	Request accept to individual DMA device (1 through 4).
MCTM/	A	DMA	Memory cycle time. Timing signal generated after DMA priority selection.
PRIORITY/	DMA	A	Absolute priority line. Locks out all requests except refresh and selected DMA device.

†A: Address and control interface
D: Data interface

TABLE 4-3. MOS MEMORY INTERBOARD SIGNALS

Signal	Source†	Dest.†	Description
BLK AB/	A	D	Inhibits loading of CPU addresses during CPU read/modify/write cycle operation.
CAS/	A	M	Column address strobe to memory arrays.
CHR-0/ CHR-1/	A	D	Character 0 and character 1 write data enable lines to write data multiplexer.
CPUMABxx/	D	A	CPU memory address lines 12 through 18. CPUMAB18/ selects the external bank.
CPUNBNDS/	D	A	CPU address in bounds. Emulates a true CPU PROTECT/ line.
CS/	A	D, M	Memory chip select. False only during refresh cycle.
DMAREQACT/	A	D	Local DMA request cycle in process. Enables DMA write data to memory.
E16KNx-x/	A	M	Read data transmit enables 0-1 through 1-4. Enable read data from selected 16K of MOS memory (one of eight).
ECCxx	D, M	Bidirec.	ECC check bit lines to/from ECC array (00 through 04).
ECCHERE/	M	A, D	Status line indicating an ECC array is installed.
EMPF	D	A	Status line indicating a load memory page file operation.
ENCPWRTDO/	A	D	Enables CPU write data to external bank over lines XO01 through XO16.
ENDMWRTDO/	A	D	Enables DMA write data to external bank over lines XO01 through XO16.
ENEXTRDO/	A	D	Enables read data to external bank over lines XI01 through XI16.
ENMOS-250	M	A	Fast array status line. Speeds up memory timing chain, if all MOS arrays are fast.
ENMOSWRTD/	A	D	Enables write data to memory arrays.
EXTREQACT/	A	D	External request cycle in process. Enables external write data to local memory bank.
MDxx	D, M	Bidirec.	Data lines to/from memory array (00 through 15).
MOSMAxx	A	M	Column and row address lines 00 through 05 to memory arrays.
MPAR	D, M	Bidirec.	Parity bit line to/from memory arrays.
MPB-L	D	A	Protect bit from read data.

†A: Address and control interface
D: Data interface
M: Memory arrays

TABLE 4-3. MOS MEMORY INTERBOARD SIGNALS (Continued)

Signal	Source	Dest.	Description
MPE+DED/	D	A	Parity error (no ECC) or double error (with ECC).
MPROT	D, M	Bidirec.	Protect bit line to/from memory arrays.
RAS16Kx-x/	A	M	Row address strobes 0-1 through 1-4. Eight lines strobe one of eight selected 16K groups of memory.
RDOPAGE/	D	A	Read-only page addressed; inhibits write operation.
SELCPUEXT/ SELCPUINT/	A	D	Select lines to place internal or external read data on the CPUDFMxx output lines. If both are false, breakpoint address is selected.
SLTBLKx/	A	M	Block select lines 0-3. Selects one of four 4K blocks on MOS array board.
STBCPUDFM/	A	D	Strobes selected read data to CPU output data register, CPUDFMxx.
STBDFM/	A	D	Strobes to latch corrected read data for possible restore operation.
STBDMADFM/	A	D	Strobes selected read data to DMA output register, DMADFMxx.
STCP/EXD/	A	D	Strobes write data into CPU, DMA, and external write data input registers.
T0-MEM/	A	D	T0 pulse from timing chain used to latch write data parity.
WRT-MPF/	A	D	Timing signal used to load the memory page file or generate a read-only page interrupt.
WRT-PB/	A	D	Enables writing of protect bit to memory.
WT-MOS/	A	M	Read/write control line to memory arrays.

†A: Address and control interface
D: Date interface
M: Memory array

TABLE 4-4. LOCAL/EXTERNAL MEMORY BANK INTERFACE SIGNALS

Signal	Interface Board†	Description	External Bank Signal Name
CH0/PF	A	Input: Write character 0. Enables XI09 through XI16 into memory. Output: Protect fault. Write attempt made to a protected location.	PF/CH0
CH1/$\overline{PE}$	A	Input: Write character 1. Enables XI01 through XI08 into memory. Output: Parity error (no ECC) or double error (with ECC) detected.	$\overline{PE}$/CH1
EXTBANK/	A	Input: Status line indicating an external bank is connected.	
EXTIMABxx/	A	Input: Memory address lines 01 through 17 from external bank.	EXTOMABxx/
EXTOMABxx/	A	Output: Memory address lines 01 through 17 to external bank.	EXTIMABxx/
EXTREQIN/	A	Input: Memory cycle request from external bank.	EXTREQOUT/
EXTREQOUT/	A	Output: Memory cycle request to external bank.	EXTREQIN/
EXTRESIN/	A	Input: Memory data resume. Read data available from external bank after trailing edge.	EXTRESOUT/
EXTRESOUT/	A	Output: Memory data resume. Read data avilable to external bank after trailing edge.	EXTRESIN/
EXTWPBIN	A	Input: Protect bit enable. Directs protect control to write protect bit (bit 17) into memory.	EXTWPBOUT
EXTWPBOUT	A	Output: Protect bit enable. Derived from CPU WRTPB or DMA-WRTPB/ inputs.	EXTWPBIN
EXTWRTIN	A	Input: Read/write control. On a read/modify/ write cycle, requests write portion.	EXTWRTOUT
EXTWRTOUT	A	Output: Read/write control. Derived from CPU WRITE or DMA WRITE inputs.	EXTWRTIN
MPB/PRF	A, D	Input: Memory protect bit status. Same as memory bit 17. Output: Program protect line. Derived from CPU PROTECT/ or DMAPROT/ inputs.	PRF/MPB

†A: Address and control interface
D: Data interface

TABLE 4-4. LOCAL/EXTERNAL MEMORY BANK INTERFACE SIGNALS (Continued)

Signal	Interface Board†	Description	External Bank Signal Name
MPL/SC	A, D	Input: Word parity status line. Generates EVENPAR or DMAMPL/ output. Output: Read/modify/write cycle request. Derived from CPU-SC/ or DMA-SC/.	SC/MPL
$\overline{PE}$/CH1	A	Input: Parity error (no ECC) or double error (with ECC) detected by external bank. Generates SET SM 108/ or DMAMPE/ output. Output: Character 1 write enable. Derived from CHAR1 or DMACHAR1 inputs.	CH1/$\overline{PE}$
PF/CH0	A	Input: Program protect fault line from external bank. Generates SET SM105/ or DMA-PF/ outputs. Output: Character 0 write enable. Derived from CHAR0 or DMACHAR0 inputs.	CH0/PF
PRF/MPB	A, D	Input: Program protect line. Output: Memory protect bit status. Same as memory bit 17.	MPB/PRF
SC/MPL	A, D	Input: Split cycle request from external bank. Output: Word parity status line.	MPL/SC
XIxx	D	Input: Write data from external bank (01 through 16). Output: Read data to external bank (01 through 16).	XOxx
XOxx	D	Input: Read data from external bank (01 through 16). Output: Write data to external bank (01 through 16).	XIxx

†A: Address and control interface
D: Date interface

external bank select bit are provided by the memory page file located in the data interface. They are available to the address and control interface as CPUMAB12/ through CPUMAB18/ with CPUMAB18/ as the external bank select bit. The memory page file is a 64-word by 9-bit random access memory employed to fully utilize the large storage capacity of the MOS memory; it is fully discussed later in this section. The file is divided into two 32-word halves; the lower half known as monitor pages, the upper as program pages. The file address is supplied by the most significant five bits of the CPU multipurpose path, S304/ through S300/, plus the MIR31' line from the CPU micro instruction register. All 262K words of an expanded memory may be addressed utilizing the page mode. Figure 4-2 shows both page mode addressing and memory page file loading address formats.

- Memory page file loading — When loading the memory page file with page addresses, the most significant five bits, S304/ through S300/, are the file address, and S305/ is the upper- or lower-half select bit. The page address, which will be written into the memory page file, is formed from the six bits S315/ through S310/. The level on S309/ is stored as the external bank select bit, and S308/ as the read only page flag. S307/ is stored as the ninth bit, but it is not used.

Once the 17-bit memory address has been formed, if the external bank select bit from the memory page file is true and the CPU (external) memory request has been accepted, the address is sent to the external bank over the lines EXTOMAB01/ through EXTOMAB17/ (see figure 4-3). The treatment of this address path, which is received by the external bank as the lines EXTIMAB01/ through EXTIMAB17/, is discussed below.

A local bank CPU request, when accepted, processes the 17-bit memory address as follows:

1. The three most significant bits (15 through 17) of the memory address are decoded to enable one of eight row address strobes or transmit enables, which selects one of up to eight sets of 16K-word memory sections.

2. The next most significant two bits (13 and 14) select one of the four 4K-word (4096 word) blocks within the 16K-word section.

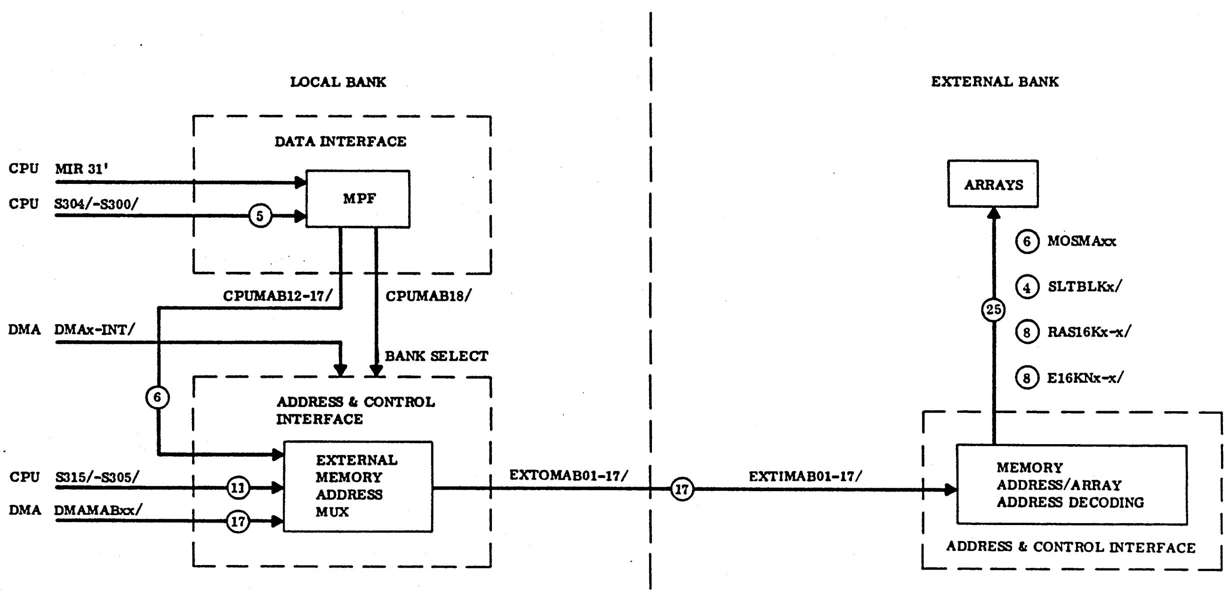


Figure 4-3. External Bank Address Path

3. The next most significant six bits (7 through 12) determine the column address within the 4K block. Each block is divided into 64 columns and 64 rows.

4. The least significant six bits (1 through 6) determine the row address within the block.

The row and column addresses are sent to the memory array over a common six-bit path, MOSMA00 through MOSMA05. The row address is placed on the path first and is strobed into the memory array by the selected row address strobe. Then the column address is placed on the path and strobed into the array by the column address strobe, CAS/.

DMA Port to Memory Array

The DMA devices transmit the memory address over a common open collector 17-bit path, DMAMAB01/ through DMAMAB17/.

The external bank selection is made by individual lines from the four DMA subports, DMA1-INT through DMA4-INT. If a low level is detected on the appropriate line selected by the DMA priority circuit, then when the DMA (external) request is honored, the incoming 17-bit DMA address is placed on the lines EXTOMAB01/ through EXTOMAB17/ to the external bank.

If the DMAx-INT line is high, a local DMA request processes the 17-bit memory address as discussed above for a CPU (local) request.

External Port to Memory Array

Addresses from external bank CPU or DMA memory requests are received on the lines EXTIMAB01/ through EXTIMAB17/. As the external request is accepted, the 17-bit address is processed as discussed above for a CPU (local) request.

READ DATA PATHS

The 18 read data bits enter the data interface from the memory array over the 16-bit bidirectional data path, MD00 through MD15, plus the parity bit line MPAR and the protect bit line MPROT. If the ECC option is installed, the ECC check bits enter on the five lines ECC00 through ECC04. The data, ECC, and parity bits enter the parity check and ECC decoding network, and single bit errors corrected if ECC is available. The resulting corrected data is available to the CPU, DMA, or external ports, or to the memory array for a restore or character write operation.

Read data from the external bank appears at the inputs XO01 through XO16, and is available to the CPU or DMA ports. The parity input is the line MPL/SC, and protect bit input is the line MPB/PRF.

Read Data to CPU Port

Read data from memory is available to both CPU data output paths: the 16-line data path CPUDFM01 through CPUDFM16, and the 16-line operand data path BUS00 through BUS15.

The CPUDFMxx lines from memory are stable with read data a maximum of 5 nanoseconds after the trailing edge of the CPUMDS/ signal and remain stable until the leading edge of the next CPU memory request.

On a CPU local read or protected write cycle the read data is the corrected data from the local bank. For a CPU external read or protected write cycle the read data is derived from the external write data input/read data inputs on XO01 through XO16.

Also available over the CPUDFMxx lines are the last address from the CPU to be loaded via the path S300/ through S315/ and the status of the ECC system, which are discussed later in this section.

A second path for read data to the CPU is the set of lines BUS00 through BUS15, which feeds the CPU tri-state bus directly. Read data is stable at this output a maximum of 120 nanoseconds after the leading edge of the next CPU memory request. (For a read/modify/write cycle request, until the leading edge of the CPUMDS/ signal that follows the leading edge of the write line.) The source of data for this path is the CPUDFMxx lines, but the output path may also be used to read the memory page file status, as discussed later in this section.

Read Data to DMA Port

Read data from memory is available to the DMA devices over the lines DMADFM01 through DMADFM16. On a DMA local read or protected write cycle the read data is the corrected data from the local bank. For a DMA external read or protected write cycle the read data is derived from the external write data output/read data inputs on XO01 through XO16. DMA read data is stable a maximum of 17 nanoseconds after the leading edge of the DMAMDS/ signal, and remains stable a minimum of 340 nanoseconds.

External Bank Read Data Path

The external read data path is shown in figure 4-4. Data stored in the external bank arrays is read and corrected by the external bank data interface, output on the external bank lines XI01 through XI16, and received by the local bank inputs XO01 through XO16. Read data is stable on these lines, after the trailing edge of the EXTRESOUT/ signal from the external bank, which is received by the local bank as the EXTRESIN/ input, and remains stable for a minimum of 80 nanoseconds. The same set of data lines is also used to carry write data to the external bank, but on a protected write cycle the write data will have been latched into a register in the external bank before the read data is placed on the lines. Note the timing diagram for an external bank protected write cycle.

The external bank read data is available to the requesting CPU or DMA port as described in the preceding paragraphs.

The read data path for a request made of the local bank by a CPU or DMA device connected to the external bank is handled in identically the same manner as described here, with the local and external banks switching roles. Note that a completely separate set of address, data, and control lines is used for this operation, and that the two functions may be executed simultaneously (e.g., a request from an external DMA device for the local memory bank may be processed concurrently with a local CPU or DMA request for the external memory bank).

From the standpoint of the requesting device, local and external requests are similar except that ECC status data is not available to the CPU for an external bank cycle.

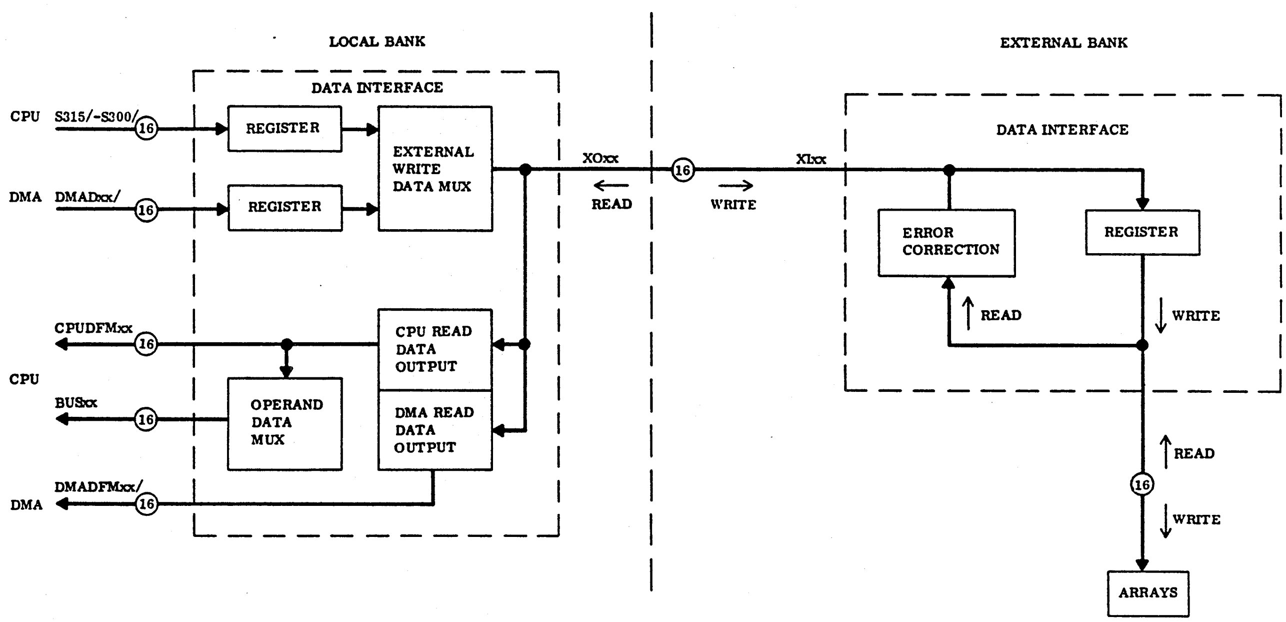


Figure 4-4. External Bank Read/Write Data Path

WRITE DATA PATHS

The data interface accepts write data from four sources: the CPU, the DMA devices, the local MOS memory arrays, and the external memory bank.

Read data from either the read portion of a split cycle request or the first portion of a protected write cycle or character write cycle is stored in the data interface. A write data multiplexer for each half (character) of a 16-bit word selects either the read data or one of the other three write data inputs to form a write data word. For example, on a DMA character 0 write request, the most significant eight bits (character 0) are selected from the DMA write data input, while the least insignificant eight bits (character 1) are selected from the read data to restore that character in memory.

Once selected, the write data word is sent to the memory array over the lines MD00 through MD15. A word parity bit (MPAR) and protect bit (MPROT) are generated and sent to the memory along with the write data. If an ECC array is included, the five ECC check bits ECC00 through ECC04 are also generated and sent to the ECC array.

CPU Write Data Path

The multipurpose path S300/ (MSB) through S315/ from the CPU is used for write data; it must be stable within 170 nanoseconds maximum after the leading edge of the CPU memory request and remain stable until the CPUMDS/ signal (for a split cycle request, from 170 nanoseconds after the leading edge of CPU WRITE until the following CPUMDS/ signal). For character write operation, the CPU places the desired character in the character 0 or character 1 position. Data on the lines is latched after the CPU request has been accepted, and is sent to the write data multiplexer.

DMA Write Data Path

The common open DMA collector data lines DMAD01/ through DMAD16/ must be stable with write data a maximum of 50 nanoseconds after the leading edge of the request accept, DMAx-RA/, and remain stable until DMAx-RA/ goes false (on split cycle requests, from within 10 nanoseconds after the leading edge of DMA WRITE). For character write operation, the DMA device places the desired character in the character 0 or character 1 position. Data on the lines is latched as the memory cycle starts, and is sent to the write data multiplexer.

External Bank Write Data Path

The external write data path is shown in figure 4-4. Write data from either the S300/ through S315/ lines from the CPU or the DMAD01/ through DMAD16/ lines from the DMA devices is enabled to the bidirectional write data out/read data in lines XO01 through XO16.

Write data is received by the external bank on the input lines XI01 through XI16. After the external bank begins the external request cycle, the write data is latched in the external write data register and the signal EXTRESOUT/ is sent to the local bank, which is received on the local bank input EXTRESIN/. At this time the write data is removed from the XO01 through XO16 lines so that read data may be received over the same path.

The write data path for a request made of the local bank by a CPU or DMA device connected to the external bank is handled in the same manner as described here, with the local and external banks switching roles. A second set of address, control, and data lines between the banks is employed for this purpose.

REQUEST AND PRIORITY SELECTION

Each of the three ports requests a memory cycle via a request control line. For the CPU, the CPUREQ/ line is brought low. The four DMA devices have individual request control lines, DMA1-MR/ through DMA4-MR/. Requests from external bank CPU or DMA devices are received by the local bank over the EXTREQIN/ line.

Since only one memory request of a single bank can be processed at one time, a priority scheme is employed to select one among two or more simultaneous inputs. Requests are honored according to the following order:

1. Refresh requests — Each 15.6 microseconds a portion of the memory is refreshed, and a memory cycle is requested internally by the refresh clock. A refresh request has first priority.

2. Priority DMA request — If the PRIORITY/ line is set low, only the DMAx-MR/ request from the DMA device selected by switch S10 on the address and control interface is recognized. All other requests except refresh are locked out until the PRIORITY/ line goes false.

3. External requests — Requests from external bank CPU or DMA devices have priority over local CPU or DMA requests. External requests are received by the local bank over the EXTREQIN/ line.

4. DMA requests — A separate priority selection is made among the four DMA request inputs, DMA1-MR/ through DMA4-MR/, with DMA1-MR/ having the highest priority. Once the highest priority DMA request has been selected, the request accept signal DMAx-RA/ is sent to the requesting device, gating data, address, and control signals from that device to the lines common to all DMA devices. Then, either a DMA local or a DMA external request is generated, which in turn competes with refresh, external, and CPU requests. For a DMA local request, refresh and external requests have higher priority. A CPU local request has lower priority unless a DMA cycle has just been completed, in which case a waiting CPU request takes precedence. A separate priority selection is made between DMA and CPU external requests, again with the DMA request having higher priority than a CPU request unless a DMA cycle is in process.

5. CPU requests — CPU requests have lowest priority, except immediately following a DMA (non-priority) cycle, as discussed above. They are received over a CPUREQ/ line from the CPU.

MODES OF OPERATION

READ REQUESTS

Read or write operation is controlled by the write request line from the requesting device. If the associated write request line is false, a read operation is specified.

CPU Read Request (Local Bank)

For a CPU read cycle the line CPU WRITE must be low within 25 nanoseconds following the leading edge of CPUREQ/, and remain low until the leading edge of CPUMDS/. A CPU read timing diagram is shown in figure 4-5 and the signals described in table 4-5.

After the CPU request has been selected by the priority circuits, the eight-phase timing chain (see section 4.3) is started and the memory address sent to the memory array. Read data from the arrays is gated to the bidirectional MDxx memory data lines by one of the E16KNx-x/ lines, and is then strobed into the CPU data output register by the second STBCPUDFM/ signal. A CPUMDS/ signal is sent to the CPU, the leading edge indicating that the incoming control lines are no longer needed, and the trailing edge indicating that read data is available over the lines CPUDFMxx and available to the BUSxx outputs. The parity error line SET SM 108/ will go low for 80 to 100 nanoseconds within 100 nanoseconds following the CPUMDS/ signal if a parity error or double error (ECC) has been detected.

CPU Read Request (External Bank)

When a CPU request is received and the external bank is addressed, the requirements for the control and data lines remain unchanged but the timing is significantly altered. A CPU read (external) timing diagram is shown in figure 4-6 for the local bank signals. External bank signal activity will be as shown in External bank request timing, figure 4-7. Signals are described in tables 4-6 and 4-7.

After the CPU request is selected by the CPU/DMA external bank priority circuits, a request is sent to the external bank over the line EXTREQOUT/, which is received by the external bank over the line EXTREQIN/. The memory address is gated to the lines EXTOMABxx. When the external bank completes the memory cycle, an EXTRESIN/ signal is received by the local bank, and read data is available over the lines XOxx. This data is strobed into the CPU data output register by the second STBCPUDFM/

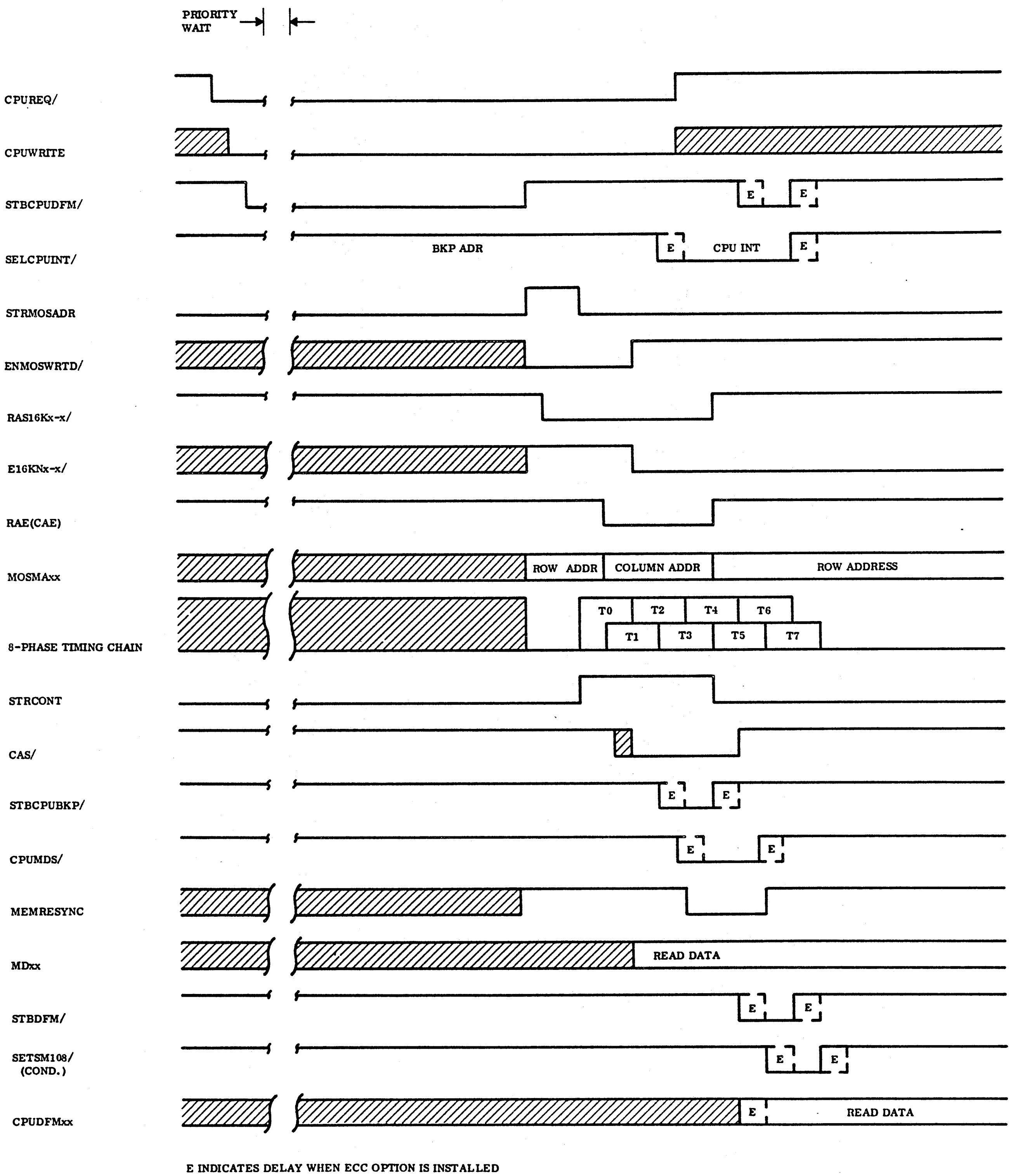


Figure 4-5. CPU Read Cycle Timing (Local)

TABLE 4-5. CPU READ CYCLE (LOCAL)

Signal	Description
CPUREQ/	CPU memory request. Must remain stable until leading edge of CPUMDS/.
CPU WRITE	Read/write control. Must remain low from 25 nanoseconds following CPUREQ/ until leading edge of CPUMDS/.
STBCPUDFM/	First pulse strobes breakpoint address into CPU output register. Second pulse strobes read data into CPU output register.
SELCPUINT/	Selects local read data to CPU output register when low, breakpoint address when high.
STRMOSADR	Begins memory cycle following acceptance of request. Latches selected address in address register.
ENMOSWRTD/	When high, enables selected (read data) E16KNx-x output.
RAS16Kx-x/	Selected row address strobe.
E16KNx-x/	Enables read data to MDxx lines.
RAE ($\overline{\text{CAE}}$)	Row address enabled to MOSMAxx lines when high, column address when low.
MOSMAxx	Row and column address lines to memory arrays.
T0 - T7	Eight-phase timing chain; starts approximately 50 nanoseconds after leading edge of STRMOSADR.
STRCONT	Timing pulse used to set status latches.
CAS/	Column address strobe to memory array.
STBCPUBKP/	Leading edge indicates to CPU read interface that breakpoint address compare is available on CPUDFMxx lines until trailing edge.
CPUMDS/	Memory data resume. Control lines from CPU need no longer be stable. Read data available 5 nanoseconds after trailing edge.
MEMRESYNC	Resync signal to priority select circuit.
MDxx	Bidirectional data lines 00 to 15 from memory, contain read data beginning at T2 time.
STBDFM/	Timing signal to data interface.
SET SM108/	Goes low at T6+50 nanoseconds for 80 to 100 nanoseconds if a parity error is detected (T7+50 nanoseconds if ECC double error).
CPUDFMxx	CPU data output lines 01 through 16 from data interface. Contain read data 5 nanoseconds after trailing edge of CPUMDS/.

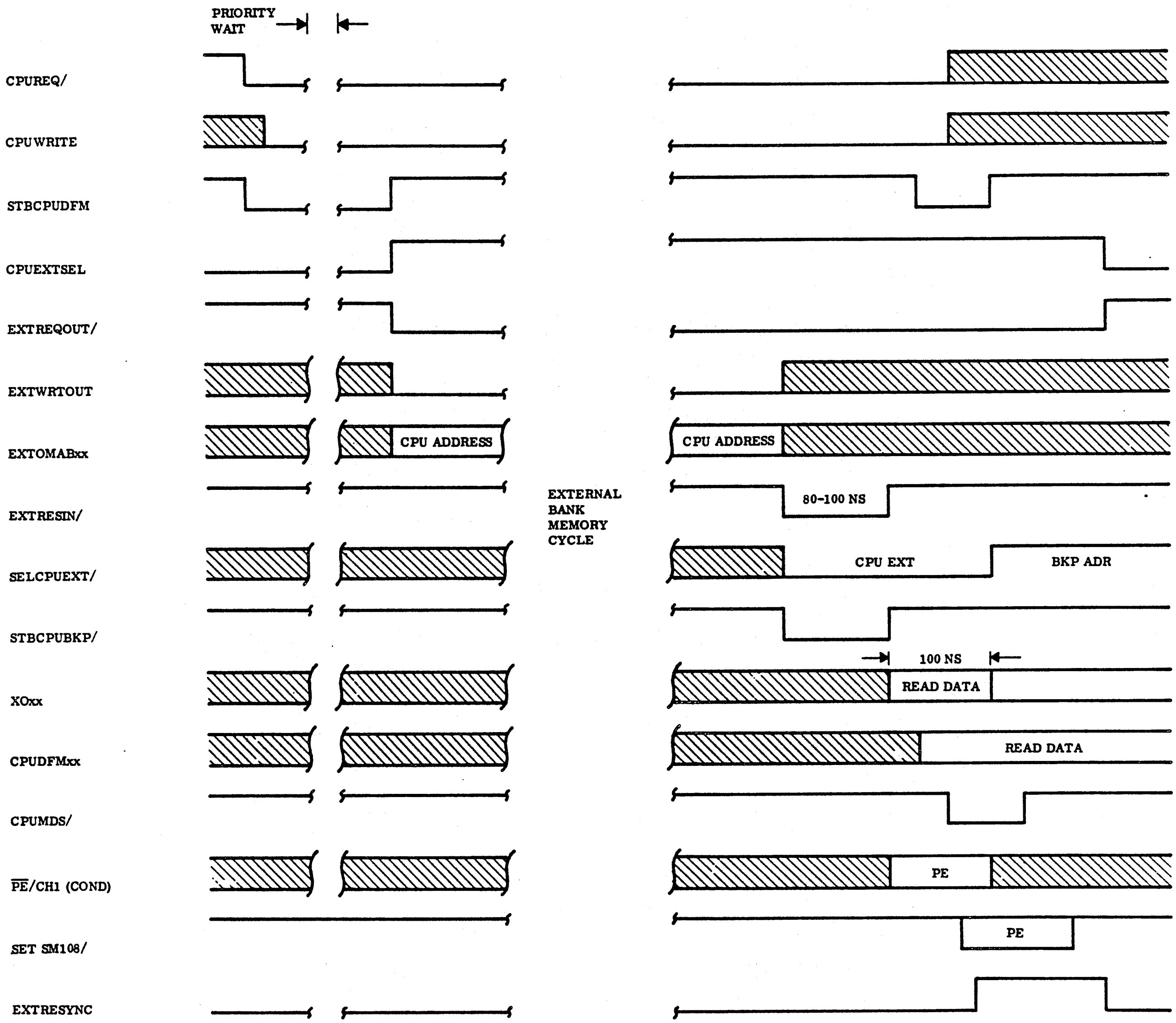


Figure 4-6. CPU Read Cycle Timing (External)

TABLE 4-6. CPU READ CYCLE (EXTERNAL)

Signal	Description
CPUREQ/	Same as local read cycle.
CPU WRITE	Same as local read cycle.
STBCPUDFM/	Same as local read cycle.
CPUEXTSEL	Enables CPU memory address to lines EXTOMABxx and CPU control lines to external bank.
EXTREQOUT/	Memory cycle request sent to external bank.
EXTWRTOUT	Read/write control line to external bank. Set to level of CPU WRITE by CPUEXTSEL.
EXTOMABxx	Memory address lines 01 through 17 to external bank.
EXTRESIN/	Memory data resume from external bank.
SELCPUEXT/	Selects external read data to CPU output register when low, breakpoint address when high.
STBCPUBKP/	Same as local cycle.
XOxx	Read data input lines 01 through 16 from external bank. Contains read data for 100 nanoseconds following trailing edge of EXTRESIN/.
CPUDFMxx	CPU data output lines 01 through 16 from data interface. Contains read data at leading edge of CPUMDS/.
CPUMDS/	Memory data resume. Control lines from CPU no longer needed. Read data available on CPUDFMxx.
$\overline{PE}$/CH1	Parity error input from external bank. Enabled for 100 nanoseconds following trailing edge of EXTRESIN/.
SET SM108/	Goes low 60 nanoseconds following trailing edge of EXTRESIN/ if the $\overline{PE}$/CH1 line is true (low).
EXTRESYNC	Resync signal to external priority select latches. Trailing edge allows next CPU or DMA external request to be processed.

signal, and the memory data resume signal CPUMDS/ leading edge indicates that incoming control signals are no longer needed and that read data is available over the CPUDFMxx lines and available to the BUSxx output. If a parity error (or double error, with ECC) is detected by the external bank, the line $\overline{PE}$/CH1 will be low following the EXTRESIN/ signal, and the SET SM 108/ line to the CPU is set low for 80 nanoseconds within 40 nanoseconds following the leading edge of the CPUMDS/ signal.

After the external request has been selected by the priority circuits, the eight-phase timing chain is started, and the memory address from lines EXTIMABxx decoded and sent to the memory array. Read data from the arrays is placed on the XIxx lines to the external bank by the ENEXTRDO/ signal, a 100 nanosecond pulse which begins at the trailing edge of the EXTRESOUT/ memory data resume signal. A parity error (no ECC) or double error (with ECC) is shown by a low level on the CH1/$\overline{PE}$ output during the same 100 nanosecond period.

External Read Request

An external read cycle is requested by a low EXTREQIN/ line. The incoming read/write control line EXTWRTIN is also low to request read operation. An external read cycle is shown in figure 4-7, and the signals described in table 4-7.

DMA Read Request (Local or External)

A DMA read cycle is requested by one of the four DMAx-MR/ signals. The local/external bank select line DMAx-INT from the highest priority DMA request

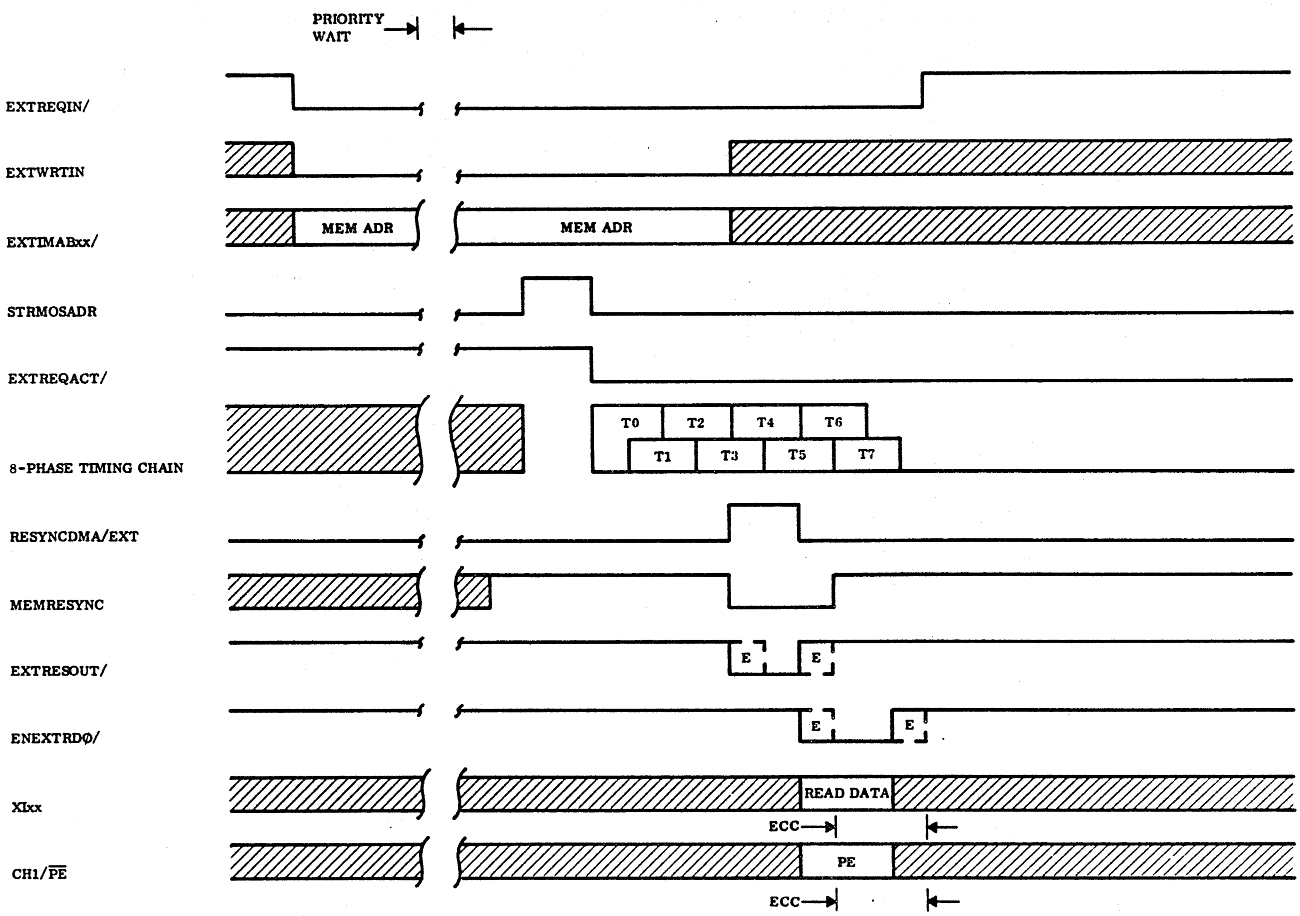


Figure 4-7. External Read Cycle Timing

TABLE 4-7. EXTERNAL READ CYCLE TIMING

Signal	Description
EXTREQIN/	Memory cycle request from external bank.
EXTWRTIN	Read/write control line from external bank; low for a read cycle.
EXTIMABxx/	Memory address lines 01 through 17 from external bank.
STRMOSADR	Begins memory cycle following acceptance of request. Latches memory address in address register.
EXTREQACT/	Status latch set at start of timing chain.
RESYNCDMA/EXT	Leading edge resets refresh, external and DMA request latches in priority circuity at T4 time.
MEMRESYNC	Resync signal to priority select circuit.
EXTRESOUT/	Memory data resume to external bank, sent at T4 time (T5 with ECC).
ENEXTRDO/	Enables read data from memory arrays to lines XIxx from T6 time to T6+100 nanoseconds (with ECC: T7 to T7+100 nanoseconds).
XIxx	Read data output lines 01 through 16 to external bank. Contain read data during ENEXTRDO/.
CH1/$\overline{PE}$	Parity error output (ECC: double error output). Conditional signal enabled during ENEXTRDO/.

will cause either a DMA local or DMA external request to be generated. Both lines must stay stable until the request accept line DMAx-RA/ goes low. The DMA device selected must then place control and address information on the lines common to all DMA devices. For a read cycle request, the DMA WRITE line must be low until the leading edge of DMAMDS/. A DMA local read cycle timing diagram is shown in figure 4-8, with signal descriptions in table 4-8. A DMA external read cycle is similar to a local cycle for signals to and from the DMA devices, and internal timing is similar to a CPU external read cycle, discussed previously.

If an external bank is selected but no external bank is connected, the memory address error line DMA-MAE/ is set low within 50 nanoseconds after DMAx-RA/. A local read cycle from the same memory address is performed, and the DMA-MAE/ signal is cleared at DMAMDS/ time.

Read data is strobed into the DMA data output register by the STBDMADFM/ signal, and a DMAMDS/ signal is sent to indicate address and control lines are no longer needed, and read data is available on the DMADFMxx outputs. The parity error signal DMAMPE/ is an 80 to 100 nanosecond pulse within 100 nanoseconds after the leading edge of DMAMDS/ if a parity error (or ECC double error) exists.

WRITE REQUESTS

A write cycle is initiated by a memory request plus a true write line from the requesting port. Two types of write cycles are used. The normal (protected, or automatic split cycle) write cycle consists of a read followed by a write portion; the read portion detects parity errors or protect faults, and may abort the write portion. The read portion in character write mode also stores the unchanged character of the addressed word so that it may be restored in the write portion. If the line ENPRTSYS is false and a word write operation is specified, a shortened write cycle without a read portion will be performed (full or unprotected write) and the protect bit automatically set regardless of the condition of previously stored data.

CPU Write Request (Local Bank, Protected)

For a CPU write cycle the control line CPU WRITE must be high within 25 nanoseconds after the leading edge of CPUREQ/ and remain high until the leading edge of CPUMDS/. The write character lines CHAR0 and CHAR1, plus the program protect line CPUPROTECT/ must also be stable over the same time period. Write data is stable on the multipurpose path S300/ through S315/ within 170 nanoseconds of CPUREQ/ until at least 25 nanoseconds after the leading edge of CPUMDS/. A timing diagram is shown in figure 4-9 and signals described in table 4-9.

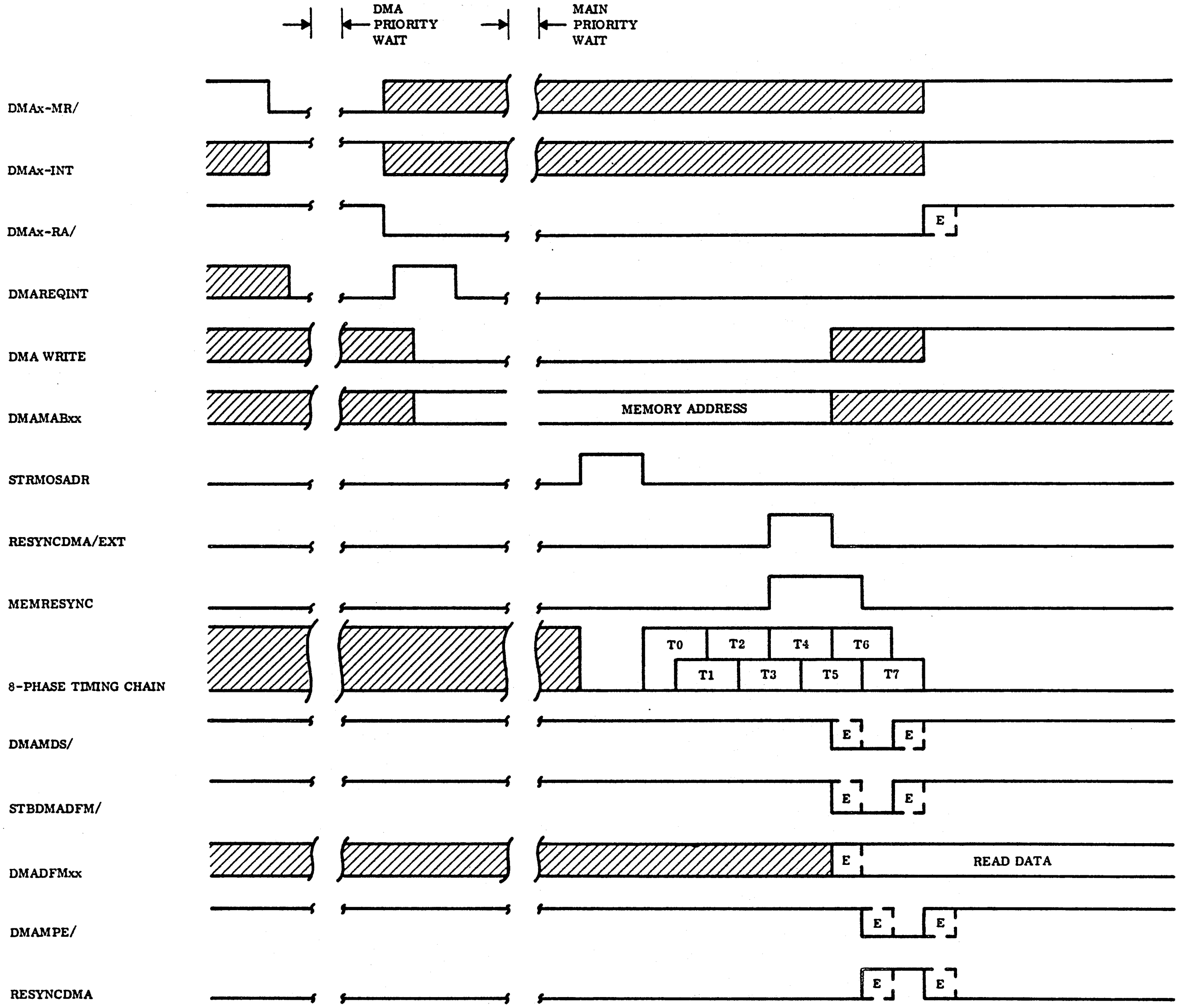


Figure 4-8. DMA Read Cycle Timing (Local)

TABLE 4-8. DMA READ CYCLE TIMING (LOCAL)

Signal	Description
DMAx-MR/	Memory cycle request from one of four (1-4) DMA devices. Must remain low until the associated DMAx-RA/ signal is sent, and must return high within 50 nanoseconds after the leading edge of DMAMDS/.
DMAx-INT	Local/external bank select line (1-4). Must remain high for local bank request from DMAx-MR/ until DMAx-RA/.
DMAx-RA/	Request accept signal (1-4). Set low when the request is accepted by the DMA priority circuits; instructs DMA device to place address and control levels on common lines within 50 nanoseconds. Returns high at T6+50 nanoseconds (T7+50 nanoseconds with ECC), trailing edge.
DMAREQINT	DMA local request pulse to main priority select circuits following selection of highest priority DMA request.
DMA WRITE	Read/write control line. Must be low within 50 nanoseconds following DMAx-RA/, remain low until DMAMDS/, and must be disabled within 50 nanoseconds following the trailing edge of DMAx-RA/.
DMAMABxx	DMA memory address bus (01-17). Must contain memory address within 50 nanoseconds following DMAx-RA/, remain stable until DMAMDS/, and be disabled within 50 nanoseconds after the trailing edge of DMAx-RA/.
STRMOSADR	Begins memory cycle following acceptance of DMAL-RQ request. Latches memory address in address register.
RESYNCDMA/EXT	Leading edge resets refresh, external, and DMA request latches in priority circuit at T4 time.
MEMRESYNC	Resync signal to priority select circuit.
DMAMDS/	Memory data resume. Control lines from DMA device no longer needed. Read data stable within 17 nanoseconds after leading edge.
STBDMADFM/	Strobes read data into DMA output register at T6 time (T7 with ECC).
DMADFMxx	DMA read data lines 01 through 16. Stable within 17 nanoseconds of DMAMDS/ for a minimum of 340 nanoseconds.
DMAMPE/	Memory parity error line. Goes low at T6+50 nanoseconds if a parity error is detected (T7+50 nanoseconds if ECC double error).
RESYNCDMA	Trailing edge resets DMA priority latches, allowing next DMA request to be selected.

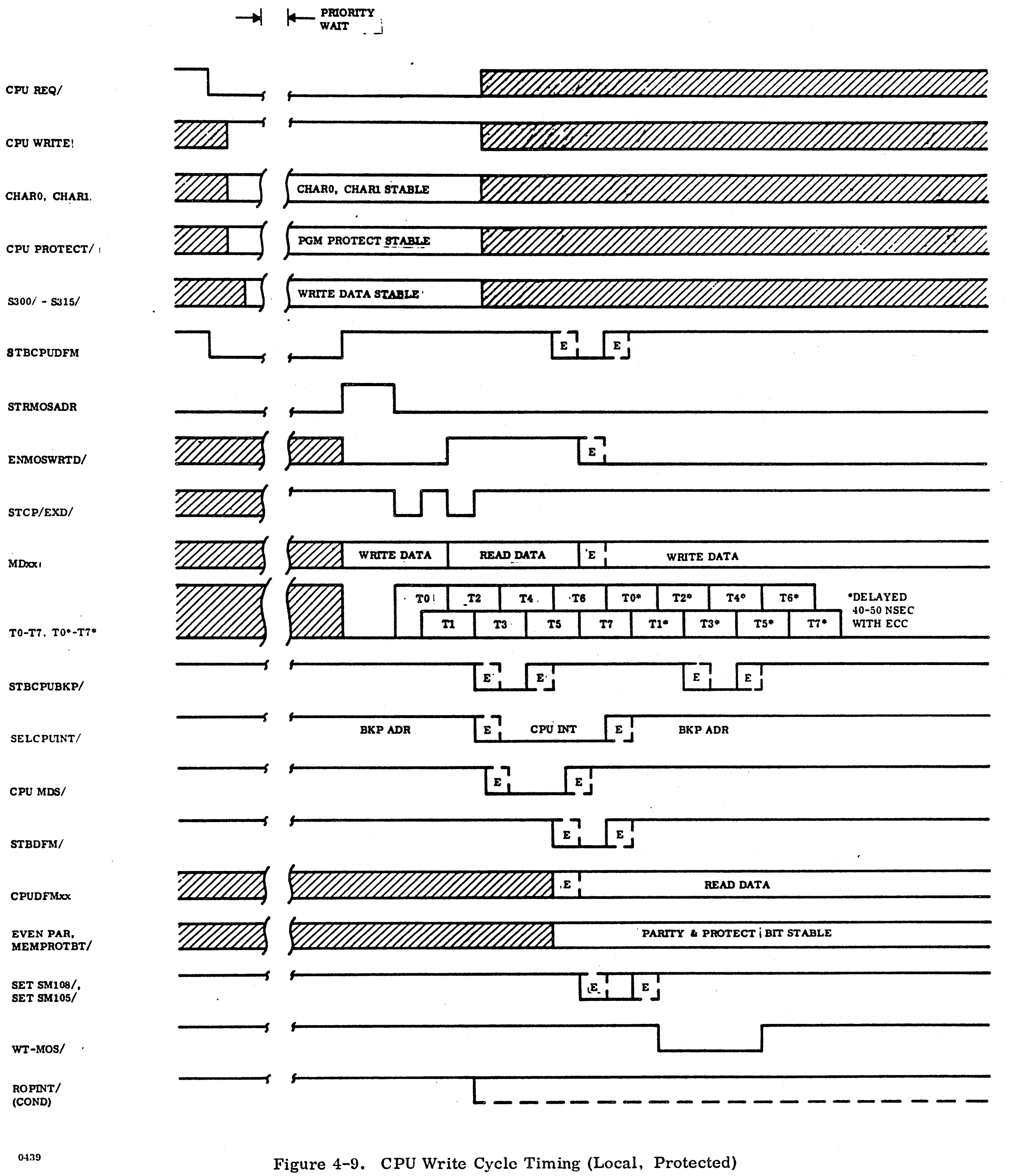


Figure 4-9. CPU Write Cycle Timing (Local, Protected)

TABLE 4-9. CPU WRITE CYCLE TIMING (LOCAL, PROTECTED)

Signal	Description
CPUREQ/	CPU memory request. Must remain stable until leading edge of CPUMDS/.
CPU WRITE	Read/write control. Must remain high from 25 nanoseconds after CPUREQ/ until leading edge of CPUMDS/.
CHAR0, CHAR1	Write character 0 and character 1 control. Must remain stable from 25 nanoseconds after CPUREQ/ until leading edge of CPUMDS/.
CPUPROTECT/	Program protect line. Must remain stable from 25 nanoseconds following CPUREQ/ until leading edge of CPUMDS/.
S300/ - S315/	CPU write data lines. Write data must be stable from 170 nanoseconds (NOTE: Should be less than 50 nanoseconds to generate parity) after leading edge of CPUREQ/ until 25 nanoseconds after leading edge of CPUMDS/.
STBCPUDFM/	First pulse strobes breakpoint address into CPU output register if previous CPU cycle was a read cycle. Second pulse strobes read data into CPU output register.
STRMOSADR	Begins memory cycle following acceptance of request. Latches selected address in address register.
ENMOSWRTD/	Enables write data to generate parity bit until T2 time, then enables selected E16KNx-x line to place read data on MDxx lines until T6+50 nanoseconds (T7+50 nanoseconds with ECC), then enables write data to MDxx lines.
T0-T7, T0*-T7*	Eight-phase timing chain. T0* to T7* is second cycle of chain. T0* starts at end of T6 without ECC, at end of T7 with ECC.
STCP/EXD/	Strobes write data from S300/ to S315/ into CPU write data input register.
MDxx	Bidirectional data lines 00 through 15 to/from memory arrays. Contain read data from T2 to T6+50 nanoseconds time (T7+50 nanoseconds with ECC), then write data.
STBCPUBKP/	Leading edge of each pulse indicates to CPU that breakpoint address compare is available on CPUDFMxx lines until trailing edge.
SELCPUINT/	Selects local read data to CPU output register when low, breakpoint address when high.
CPUMDS/	Memory data resume. Control lines from CPU need no longer be stable. Read data available 5 nanoseconds after trailing edge.
STBDFM/	Latches read data for use in character write or restore operation.
CPUDFMxx	CPU data output lines 1 through 16 from data interface. Contain read data 5 nanoseconds after trailing edge of CPUMDS/.
EVENPAR	Write data word parity. High if number of 1 bits in write data is even.
MEMPROTBT/	Memory protect bit output line.
SET SM105/	Protect fault line. Goes low at T6+50 nanoseconds (T7+50 nanoseconds with ECC) if a protect fault detected.
SET SM108/	Goes low at T6+50 nanoseconds for 80 to 100 nanoseconds if a parity error is detected (T7+50 nanoseconds if ECC double error).
WT-MOS	Write enable line to memory arrays, high from T2* to T6* time.
ROPINT/	Read only page interrupt. Goes low at T3 time if a write attempt made on a read only page. Cleared when new address loaded. (NOTE: This signal shown in write timing diagram only for reference; memory will operate in a read cycle only.)

After the CPU request has been accepted, the eight-phase timing chain is started, write data is latched in the CPU write data input register and temporarily gated to the MDxx lines for the purpose of determining the word parity of the incoming write data. Read data is then applied to these lines, and strobed into the CPU data output register (after error correction, with ECC) by the line STBCPUDFM/. A CPUMDS/ memory resume is sent to the CPU, the leading edge indicating the end of the need for input control and write data, and the trailing edge indicating read data, write word parity and the memory protect bit status is available to the CPU over the lines CPUDFMxx, EVENPAR and MEMPROTBT/, respectively. Read data output is also available to the BUSxx output. The parity error (SET SM108/) and protect fault (SET SM105/) lines will indicate the appropriate status approximately 100 nanoseconds later by an 80 to 100 nanosecond pulse.

Write data is then again gated to the MDxx lines and the eight-phase timing chain started on a second cycle. The WT-MOS/ control line to the memory arrays is set low for a 160 to 200 nanosecond period to write the data in memory. This signal is inhibited, leaving the memory contents unchanged, if a protect fault or protect parity error is encountered (see discussion on protection later in this section).

If a read only page has been addressed, the write line is inhibited and the memory will execute only a read cycle, but the read only page interrupt ROPINT/ will be generated at the time shown in the timing diagram.

CPU Write Request (External Bank, Protected)

When a CPU write request is received and the external bank is addressed, the requirements for the control and data lines remain unchanged from local bank requirements. A CPU write (external) timing diagram is shown in figure 4-10 for the local bank signals, with descriptions in table 4-10. External bank signal activity will be as shown in external write request timing.

After the CPU request is selected by the CPU/DMA external bank priority circuits, a request is sent to the external bank over the line EXTREQOUT/, which is received by the external bank as the signal EXTREQIN/. The memory address is gated to the lines EXTOMABxx, write data from lines S300 through S315/ to the lines XOxx, and CPU control lines to the appropriate external bank control lines.

When the external bank completes the memory cycle, an EXTRESIN/ signal is received by the local bank, at which time the local bank removes the address, write data and control information from the local/external bank lines. At the trailing edge of EXTRESIN/ read data is available over the XOxx lines, and parity and protect bit status over the appropriate control lines. The read data is strobed into the CPU data output register by the STBCPUDFM/ signal, and the memory resume signal CPUMDS/ indicates that incoming control signals and write data are no longer needed, and that read data is available over the CPUDFMxx lines as well as available to the BUSxx output. If a parity error (double error with ECC) or a protect fault is detected by the external bank, the appropriate SET SM108/ or SET SM105/ line to the CPU will be set low for 80 nanoseconds within 40 nanoseconds following the leading edge of the CPUMDS/ signal.

If no external bank is connected, the external bank request is inhibited and the memory will perform a read cycle from the same address in the local bank. If a read only page has been addressed, the write line is inhibited and the external bank will execute only a read cycle. The read only page interrupt signal ROPINT/ will be generated coincident with the leading edge of the STBCPUDFM/ signal.

CPU Write Request (Protection Disabled)

A shortened write-only cycle is available if the normal write protection system is disabled by a low ENPRTSYS line. Since no read portion is included, only a full word write (CHAR0 and CHAR1 both true) may be used as no restore data will be available. The protection scheme is overridden in that the previously stored protect bit is not read, no protect fault or write abort can occur, and the protect bit is set into memory bit 17 on every instruction. Only a read only page error or memory addressing error (no external bank) will defeat a write operation.

Processing of the request is the same as for a protected write request except that no parity error or protect fault signals will be generated and no read information is available. A timing diagram is shown in figure 4-11. Note that only one cycle of the eight-phase timing chain is utilized. Signal descriptions are included in table 4-11.

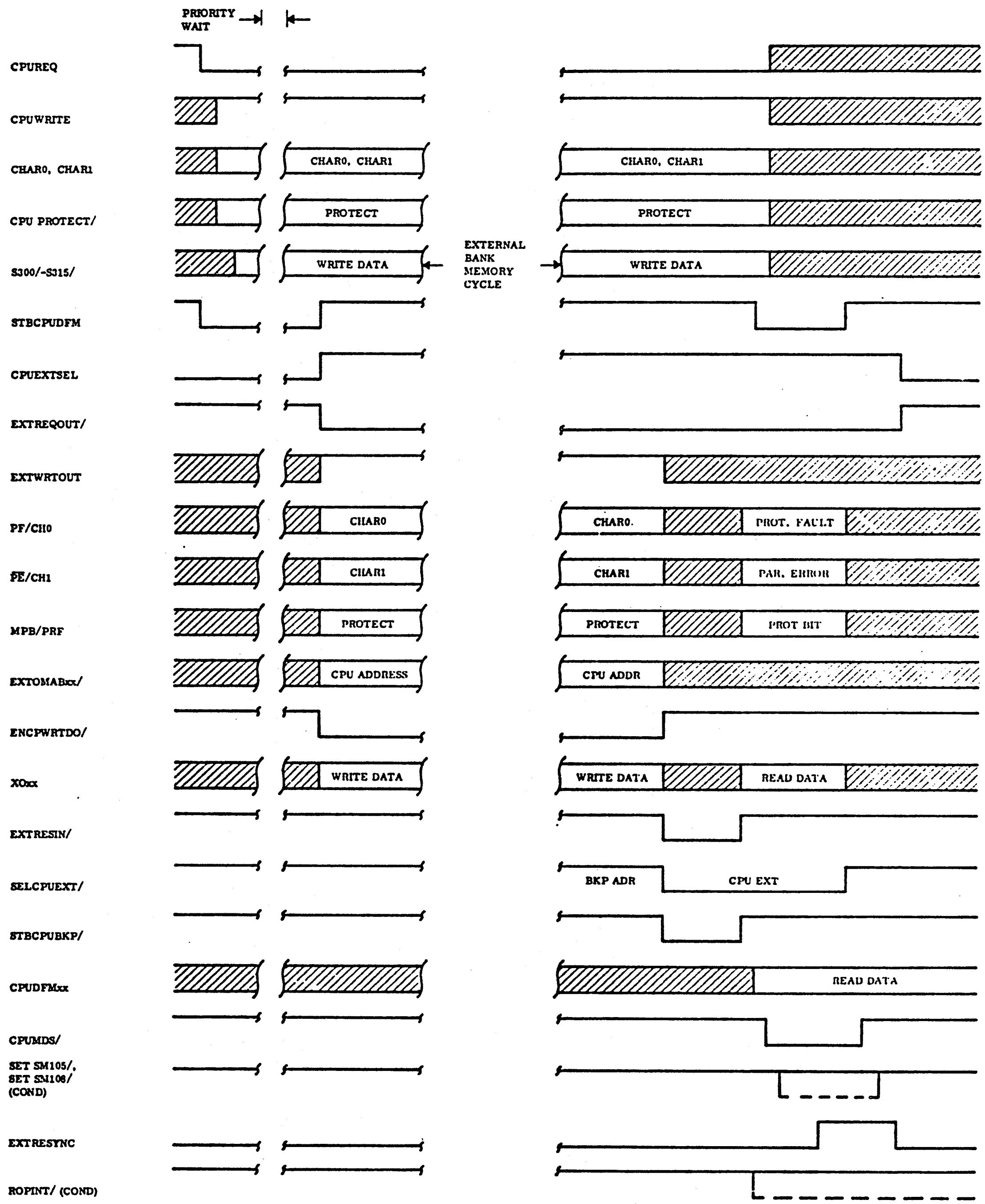


Figure 4-10. CPU Write Cycle Timing (External)

TABLE 4-10. CPU WRITE CYCLE TIMING (EXTERNAL)

Signal	Description
CPUREQ/	CPU memory request. Must remain stable until leading edge at CPUMDS/.
CPU WRITE	Read/write control. Must remain high from 25 nanoseconds after CPUREQ/ until leading edge of CPUMDS/.
CHAR0, CHAR1	Write character 0 and character 1 control. Must remain stable from 25 nanoseconds after CPUREQ/ until leading edge of CPUMDS/.
CPUPROTECT/	Program protect line. Must remain stable from 25 nanoseconds following CPUREQ/ until leading edge of CPUMDS/.
S300/ - S315/	CPU write data lines. Write data must be stable from 170 nanoseconds. (NOTE: Should be less than 50 nanoseconds to generate parity) after leading edge of CPUREQ/ until 25 nanoseconds after leading edge of CPUMDS/.
STBCPUDFM/	First pulse strobes breakpoint address into CPU output register if previous CPU cycle was a read cycle. Second pulse strobes read data into CPU output register.
CPUEXTSEL	Enables CPU memory address to lines EXTOMABxx and CPU control lines to external bank.
EXTREQOUT/	Memory cycle request sent to external bank.
EXTWRTOUT	Read/write control line to external bank. Set to level of CPU WRITE by CPUEXTSEL.
PF/CH0	Dual purpose line. Set to level of CHAR0 by CPUEXTSEL until EXTRESIN/. Contains conditional protect fault signal from external bank for 100 nanoseconds following trailing edge of EXTRESIN/.
$\overline{\text{PE}}$/CH1	Dual purpose line. Set to level of CHAR1 by CPUEXTSEL until EXTRESIN/. Contains conditional parity error signal from external bank for 100 nanoseconds following the trailing edge of EXTRESIN/.
MPB/PRF	Dual purpose line. Set to complement of CPU PROTECT/ by CPUEXTSEL until EXTRESIN/. Contains level of protect bit from external bank for 100 nanoseconds following trailing edge of EXTRESIN/.
EXTOMABxx	Memory address lines 01 through 17 to external bank.
ENCPWRTDO/	Enables write data from lines S300/ through S315/ to lines XOxx.
XOxx	Dual purpose data lines 01 through 16 to/from external bank. Contain write data from EXTREQOUT/ until EXTRESIN/. Contain read data for 100 nanoseconds after trailing edge of EXTRESIN/.
EXTRESIN/	Memory resume signal from external bank.
SELCPUEXT/	Selects external read data to CPU output register when low, breakpoint address when high.
STBCPUBKP/	Leading edge indicates CPU breakpoint address compare is available on CPUDFMxx lines until trailing edge.
CPUDFMxx	CPU data output lines 10 through 16 from data interface. Contain read data after leading edge of CPUMDS/.
CPUMDS/	Memory data resume. Control lines from CPU need no longer be stable. Read data available at leading edge.
SET SM105/	Protect fault line. Goes low 60 nanoseconds following trailing edge of EXTRESIN/ if the PF/CH0 line is true (high).
SET SM108/	Parity error line. Goes low 60 nanoseconds following trailing edge of EXTRESIN/ if the $\overline{\text{PE}}$/CH1 line is true (low).
EXTRESYNC	Resync signal to external priority select latches. Trailing edge allows next CPU or DMA external request to be processed.
ROPINT/	Read only page interrupt. Goes low at leading edge of CPUMDS/ if a write attempt made on a read-only page. Cleared when new address loaded. (NOTE: This signal shown in write timing diagram only for reference; external bank operates in a read cycle only.)

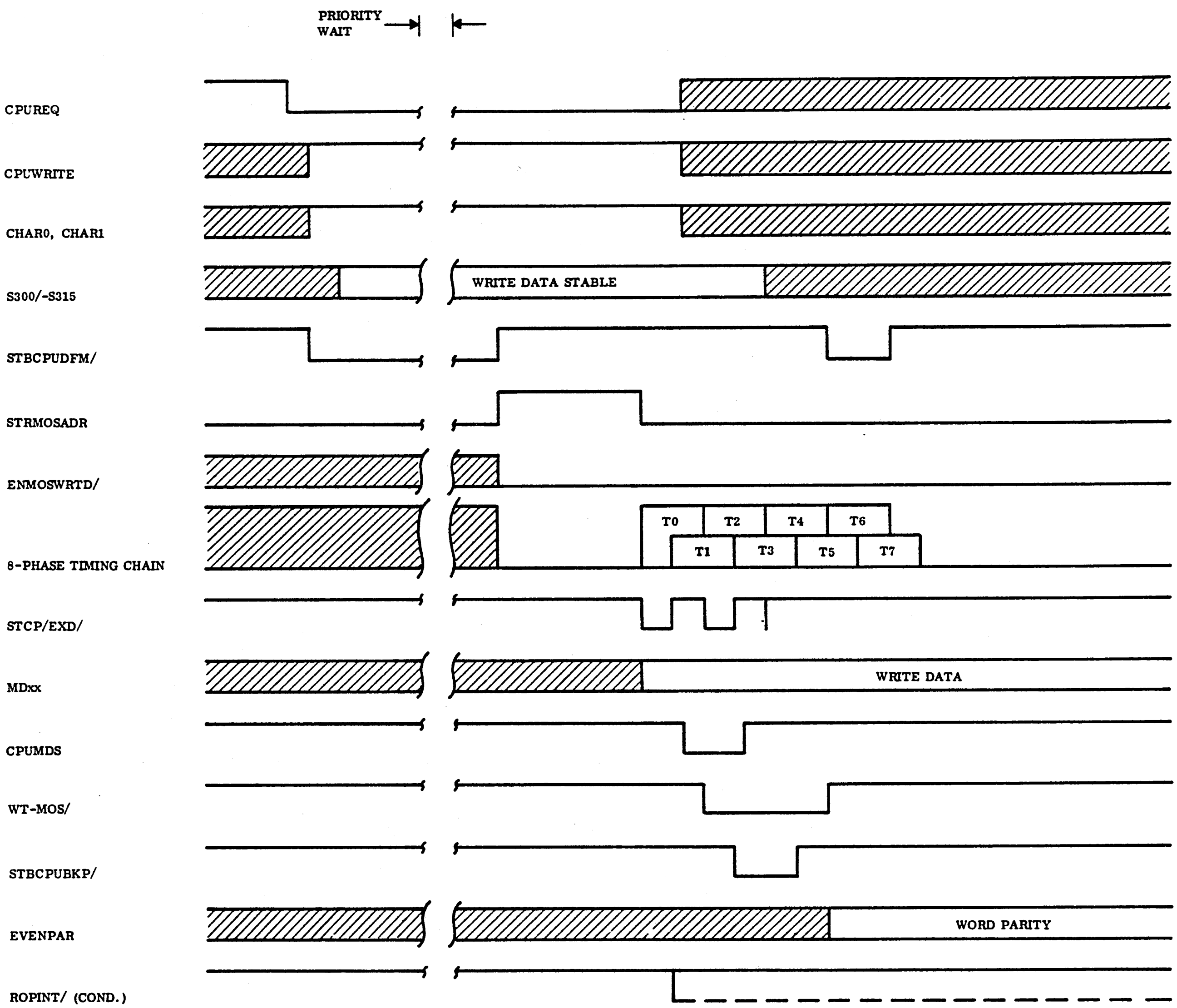


Figure 4-11. CPU Write Cycle Timing (Local, Protection Disabled)

TABLE 4-11. CPU WRITE CYCLE (LOCAL, PROTECTION DISABLED)

Signal	Description
CPUREQ/	CPU memory request. Must remain stable until leading edge of CPUMDS/.
CPU WRITE	Read/write control line. Must remain stable from 25 nanoseconds after CPUREQ/ until leading edge of CPUMDS/.
CHAR0, CHAR1	Both character write lines must be true (high) from 25 nanoseconds after CPUREQ/ until leading edge of CPUMDS/.
S300/ - S315/	CPU write data lines. Must be stable from 100 nanoseconds after CPUREQ/ until 50 nanoseconds after trailing edge of CPUMDS/.
STBCPUDFM/	First pulse strobes breakpoint address into CPU output register if previous cycle was a read cycle. Second pulse unused.
STRMOSADR	Begins memory cycle following acceptance of request. Latches selected address in address register.
ENMOSWRTD	Enables write data to MDxx lines.
STCP/EXD/	Strobes write data from S300/ through S315/ lines into CPU write data input register.
MDxx	Write data lines to memory.
CPUMDS/	Memory data resume. Control lines from CPU need no longer be stable.
WT-MOS/	Write enable line to memory arrays. Low from T2 to T6 time.
STBCPUBKP/	If previous cycle was a read cycle, leading edge indicates breakpoint address available on CPUDFMxx lines until trailing edge.
EVENPAR	Write data word parity. High if number of 1 bits in write data is even.
ROPINT/	Read only page interrupt. Conditional at T1 time.

If the external bank is address and the ENPRTSYS line on the external bank is not also set low, a normal CPU (external) write cycle will be executed (complete with read data) except that the external bank will see a true protect line (MPB/PRF). If ENPRTSYS is low on the external bank, the short cycle will be executed and protect bit set even if ENPRTSYS was not set low on the local bank.

External Write Requests

An external write cycle is requested by a low EXTREQIN/ line. The read/write control line EXTWRTIN is high to indicate a write request. The control lines CH0/PF, CH1/$\overline{PE}$, and PRF/MPB contain the control information dictated by the CPU or DMA control lines for write character and program protect. An external write cycle is shown in figure 4-12 and the signals described in table 4-12.

After the external request has been selected by the priority circuits, the eight-phase timing chain is started, and the memory address from EXTIMABxx/ and write data from XIxx is sent to the memory array. Read data from the arrays is placed on the same XIxx lines by the ENEXTRDO/ signal, a 100 nanosecond pulse which begins at the trailing edge of the EXTRESOUT/ memory data resume signal. Parity and protect status information is transmitted over the bidirectional control lines CH0/PF, CH1/$\overline{PE}$ and PRF/MPB during the same 100 nanosecond period.

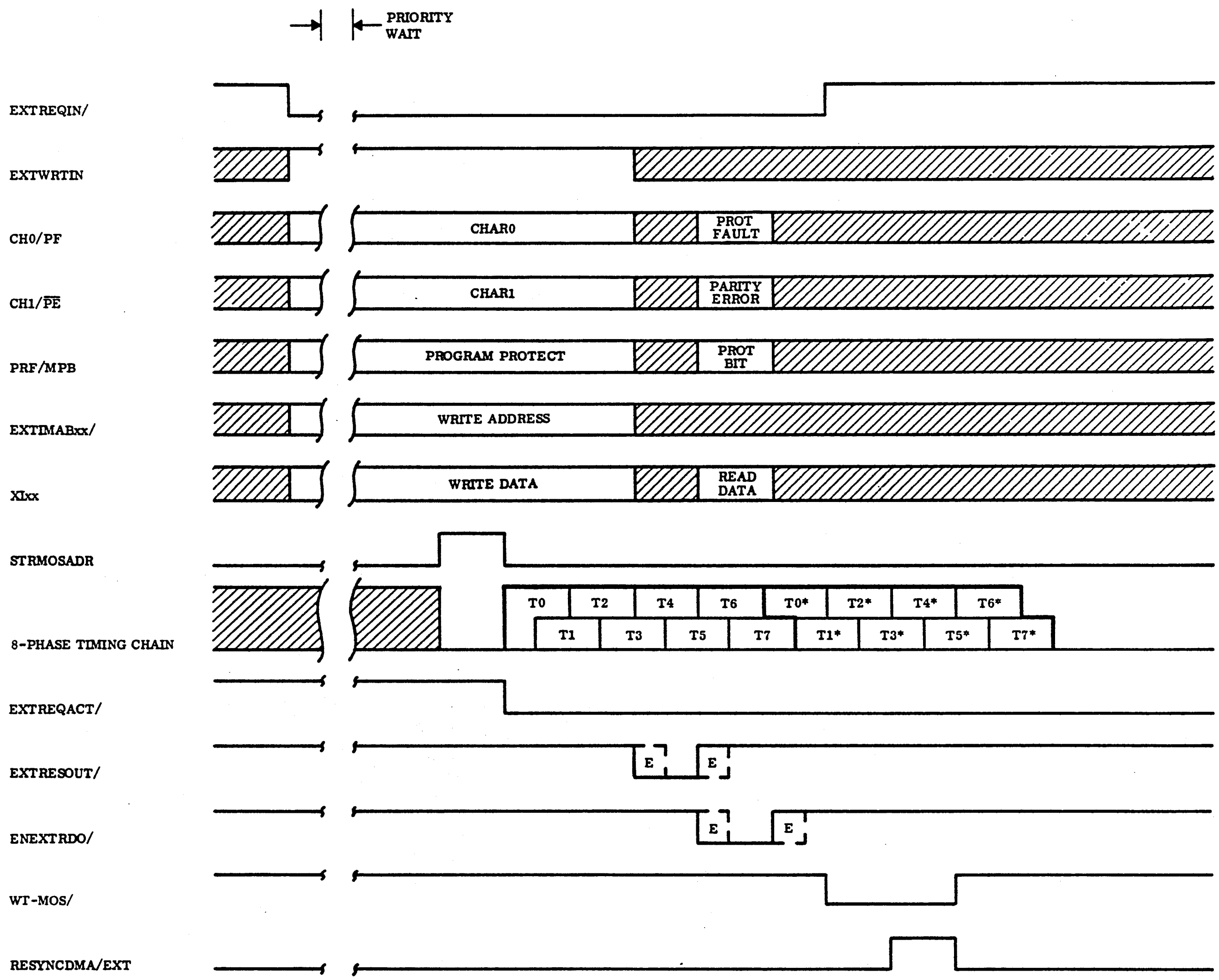


Figure 4-12. External Write Cycle Timing (Protected)

TABLE 4-12. EXTERNAL WRITE CYCLE TIMING (PROTECTED)

Signal	Description
EXTREQIN/	Memory cycle request from external bank.
EXTWRTIN	Read/write control from external bank; high for a write cycle.
CH0/PF	Write character 0 control line until T4 time; protect fault conditional output during ENEXTRDO/.
CH1/$\overline{\text{PE}}$	Write character 1 control line until T4 time; parity error or ECC double error conditional output during ENEXTRDO/.
PRF/MPB	Protect control line until T4 time; memory protect bit 17 during ENEXTRDO/.
EXTIMABxx	Memory address lines 01 through 17 from external bank.
XIxx	Write data input lines 10 through 16 from external bank until T4 time; read data output lines during ENEXTRDO/.
EXTREQACT/	Enables write data from XIxx lines to memory arrays.
ENEXTRDO/	Enables read data from memory arrays to lines XIxx from T6 time to T6+100 nanoseconds (with ECC: T7 to T7+100 nanoseconds).
WT-MOS/	Write enable line to memory arrays; low from T2* to T6* time.
RESYNCDMA/EXT	Leading edge resets refresh, external and DMA request latches in priority circuit at T4* time.

DMA Write Requests (Local and External)

A DMA write cycle is requested by one of the four DMAx-MR/ signals. The local/external bank select line DMAx-INT from the highest priority DMA request will cause either a DMA local or DMA external request to be generated. Both lines must stay stable until the request accept line DMAx-RA/ goes low. The DMA device selected must then place control and address information on the lines common to all DMA devices. For a write cycle request, the DMA WRITE line must be high until the leading edge of DMAMDS/. The write character lines DMACHAR0 and DMACHAR1, the program protect line DMAPROT/, and the write data lines DMADxx must also be stable over the same period. A timing diagram for a DMA local protected write cycle is shown in figure 4-13, with signal descriptions in table 4-13. A DMA external write cycle is similar to a local cycle for signals to and from the DMA devices, and internal timing is similar to a CPU external write cycle, discussed previously. A shortened DMA unprotected write cycle is possible when the ENPRTSYS line is low, with internal timing similar to a CPU unprotected write cycle.

If an external bank is selected but no external bank is connected, the memory address error line DMA-MAE/ is set low within 50 nanoseconds after DMAx-RA/. A local read cycle from the same memory address is performed, and the DMA-MAE/ signal is cleared at DMAMDS/ time.

After the DMA request has been accepted by both the DMA and main priority select circuits, write data from the lines DMADxx/ are latched in the DMA write data input register and the parity determined. Read data is

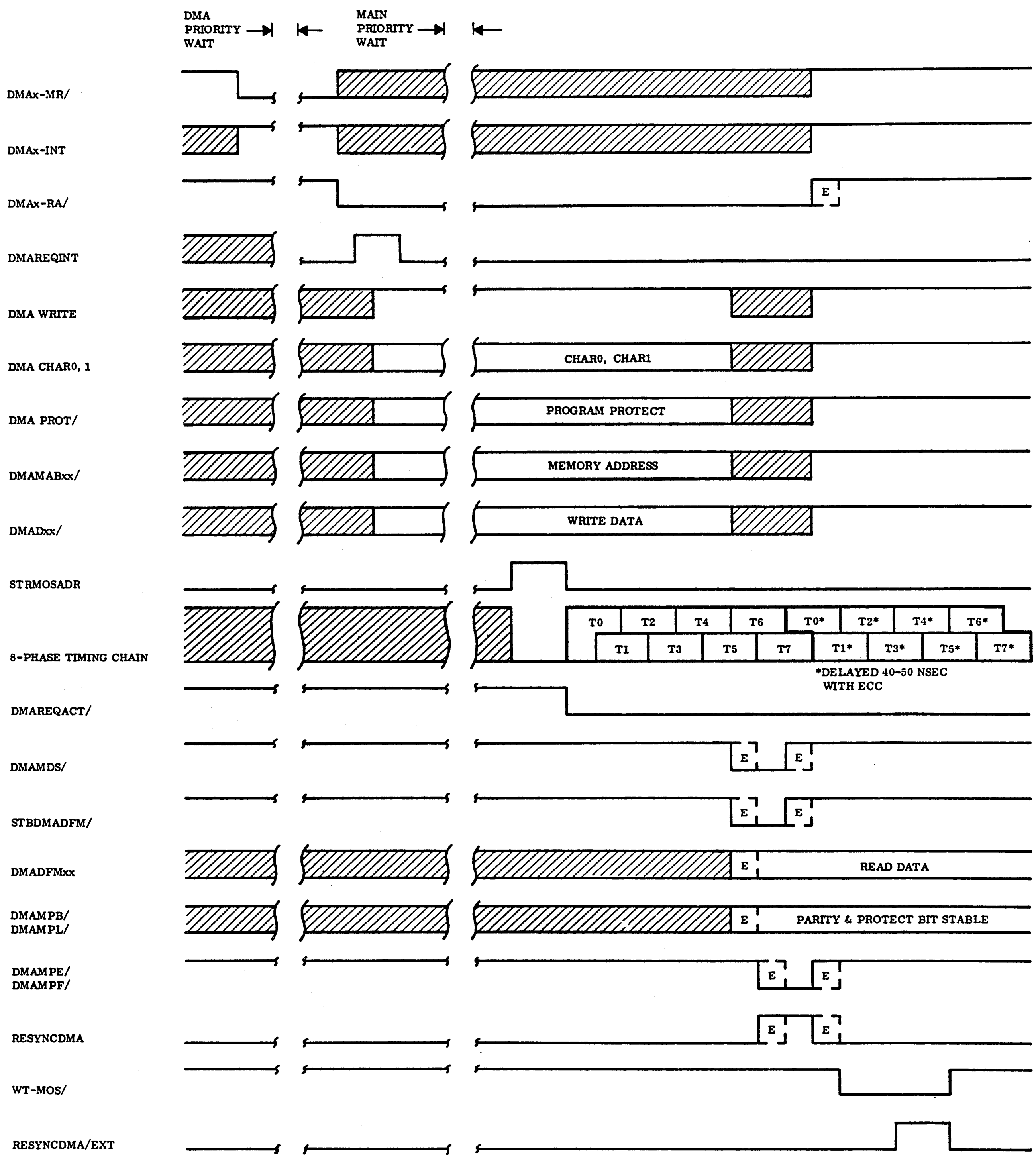


Figure 4-13. DMA Write Cycle Timing (Local, Protected)

TABLE 4-13. DMA WRITE CYCLE TIMING (LOCAL, PROTECTED)

Signal	Description
DMAx-MR/	Memory cycle request from one of four (1-4) DMA devices. Must remain low until the associated DMAx-RA/ signal is sent, and must return high within 50 nanoseconds after leading edge of DMAMDS/.
DMAx-INT	Local/external bank select line (1-4). Must remain high for local bank request from DMAx-MR/ until DMAx-RA/.
DMAx-RA/	Request accept signal (1-4). Set low when the request is accepted by the DMA priority circuits, and instructs DMA device to place address, write data and control levels on the common lines within 50 nanoseconds. Returns high at T6+50 nanoseconds (T7+50 nanoseconds with ECC), trailing edge.
DMAL-RQ	DMA local request pulse to main priority select circuits following selection of highest priority DMA request.
DMA WRITE	Read/write control line. Must be high within 50 nanoseconds following DMAx-RA/, remain high until DMAMDS/, and must be disabled within 50 nanoseconds following the trailing edge of DMAx-RA/.
DMACHAR0 DMACHAR1	Write character 0 and character 1 control. Must remain stable from 50 nanoseconds following DMA-RA/, remain stable until DMAMDS/, and be disabled within 50 nanoseconds after the trailing edge of DMAx-RA/.
DMAPROT/	Program protect line. Must remain stable from 50 nanoseconds following DMAx-RA/, remain stable until DMAMDS/, and be disabled within 50 nanoseconds after the trailing edge of DMAx-RA/.
DMAMABxx	DMA memory address bus (01-17). Must contain memory address within 50 nanoseconds following DMAx-RA/, remain stable until DMAMDS/, and be disabled within 50 nanoseconds after the trailing edge of DMAx-RA/.
DMADxx/	DMA write data lines. Write data must be stable within 50 nanoseconds following DMAx-RA/, remain stable until DMAMDS/, and be disabled within 50 nanoseconds after the trailing edge of DMAx-RA/.
STRMOSADR	Begins memory cycle following acceptance of DMAL-RQ request. Latches memory address in address register.
DMAREQACT/	Enables write data from DMADxx lines to memory arrays.
DMAMDS/	Memory data resume. Write data and control lines from DMA device no longer needed. Read data stable within 17 nanoseconds after leading edge.
STBDMADFM/	Strobes read data into DMA output register at T6 time (T7 with ECC).
DMADFMxx	DMA read data lines 01 through 16. Stable within 17 nanoseconds of DMAMDS/ for a minimum of 340 nanoseconds.
DMAMPB/	Memory protect bit output line.
DMAMPL/	Write data word parity output line. Low if number of 1 bits in write data word is even.
DMAMPF/	Protect fault line. Goes low at T6+50 nanoseconds (T7+50 nanoseconds with ECC) if a protect fault is detected.
DMAMPE/	Goes low at T6+50 nanoseconds for 80 to 100 nanoseconds if parity error is detected (T7+50 nanoseconds if ECC double error).
RESYNC DMA	Leading edge resets DMA priority latches, allowing next DMA request to be selected.
WT-MOS /	Write enable line to memory arrays; low from T2* to T6* time.
RESYNCDMA/EXT	Leading edge resets refresh, external, and DMA request latches in priority circuit at T4* time.

strobed into the DMA output register (after error correction, with ECC) by the line STBDMADFM/. A DMAMDS/ signal is sent to indicate address, write data and control lines are no longer needed from the DMA; read data is available on the DMADFMxx output and word parity as well as memory protect bit status is available over the lines DMAMPL/ and DMAMPB/. The parity error (DMAMPE/) and protect fault (DMAMPF/) lines will indicate the appropriate status approximately 50 nanoseconds later by an 80 to 100 nanosecond pulse.

Write data is then gated to the arrays and the WT-MOS/ control line is set low to write the data into the selected location. This signal is inhibited, leaving the memory contents unchanged, if a protect fault or protect parity error is encountered (see discussion on protection later in this section).

SPLIT CYCLE OPERATION

Two types of split cycle operation are utilized in the MOS memory system. The automatic read/write split cycle is used in a normal, protected write operation, and is discussed in previous paragraphs. A read/modify/write cycle may be requested which will allow certain controls and data to be changed between the read and write portions. The request is made via the split cycle control line from any port, and either local or remote bank may be addressed.

The first portion of the cycle is a read portion, with the same input and output requirements as a standard read cycle except that the split cycle control line (CPU-SC/ or DMA-SC/) must remain true throughout the read portion and the read/write control line must stay false.

After the read cycle has ended, the memory will halt. The read/write control line must be held false during the modify period, as this line going true triggers the write portion of the cycle. As the read information is digested, changes in the write data and character write control lines may be changed. The write portion may not be aborted, however the original data may be restored to memory by having both write character lines pulled false by the requesting device.

The write portion of a read/modify/write split cycle is initiated by the write line going true, and the split cycle control line must return false within 50 nanoseconds of that time. Normally, a read/write automatic split cycle will constitute the write portion of a read/modify/write requested split cycle, as shown in the timing diagram of figure 4-14, and in the signal description of table 4-14.

WORD/CHARACTER MODE

Certain applications utilize memory more efficiently in eight-bit segments, or characters, rather than in 16-bit words. The character mode of operation allows memory information to be modified one 8-bit character at a time.

Character 0 is the most significant eight bits of the data word, received by the CPU port on lines S300/ through S307/ and by the DMA port on DMAD09 through DMAD16/. Character 1 is the least significant eight bits. Read operations are not affected by the character mode, and the requesting device must extract the wanted character from the full 16-bit word. Character write operations are accomplished by reading the addressed word, then writing a new word consisting of the one new character along with the remaining eight bits just read from the addressed location. This rewriting of read data is known as a restore operation. Thus, in a character 0 write cycle character 0 is written with new information while character 1 is restored.

The character write control lines CHAR0, CHAR1, DMACHAR0 and DMACHAR1 direct write operations in memory according to the following truth table:

CHAR0 or DMACHAR0	CHAR1 or DMACHAR1	Write Function
True	True	Full word write
True	False	Write character 0, restore character 1
False	True	Write character 1, restore character 0
False	False	Restore entire word

The full word restore operation may be used in read/modify/write split cycle requests when the requesting

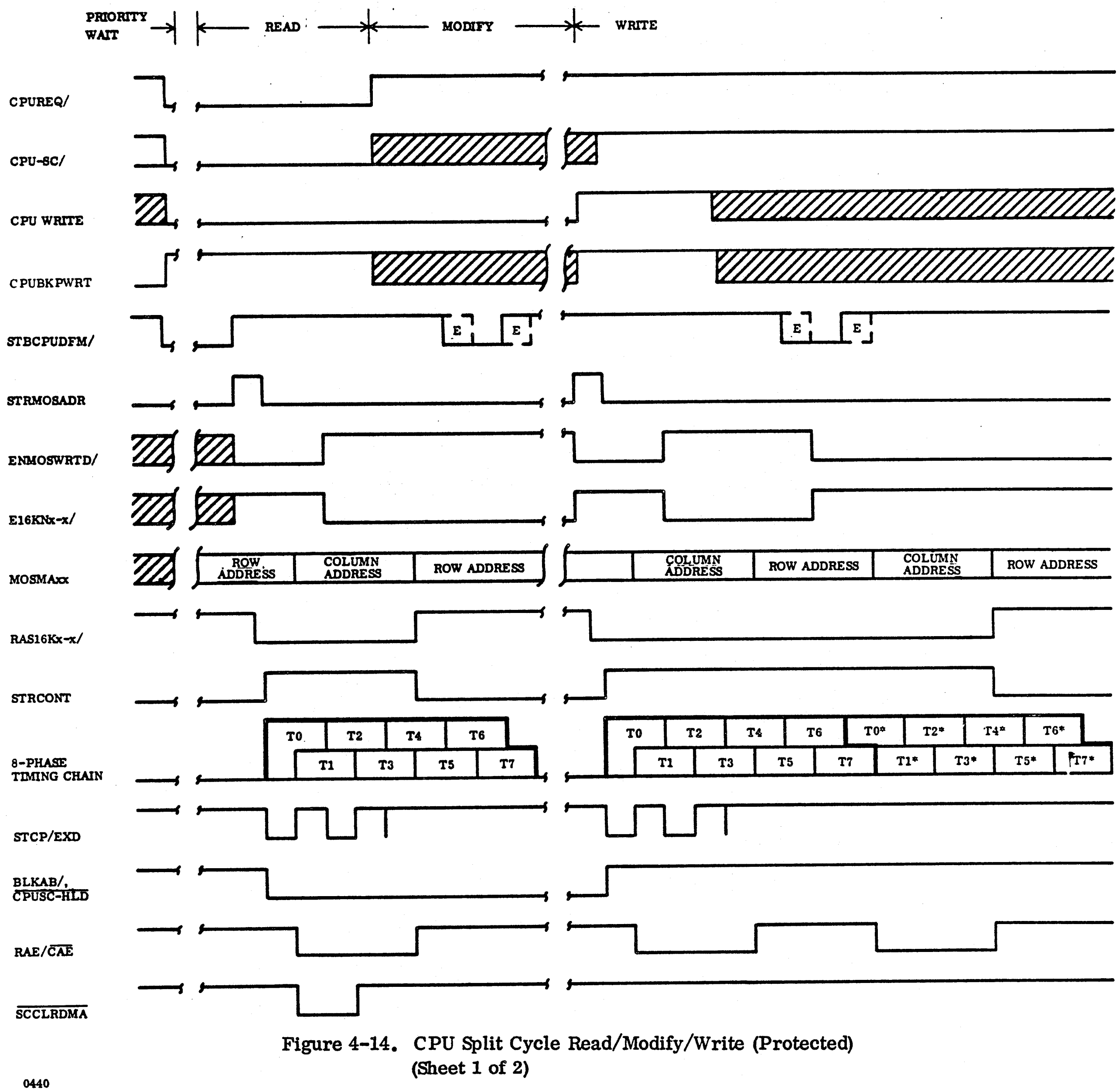


Figure 4-14. CPU Split Cycle Read/Modify/Write (Protected)
(Sheet 1 of 2)

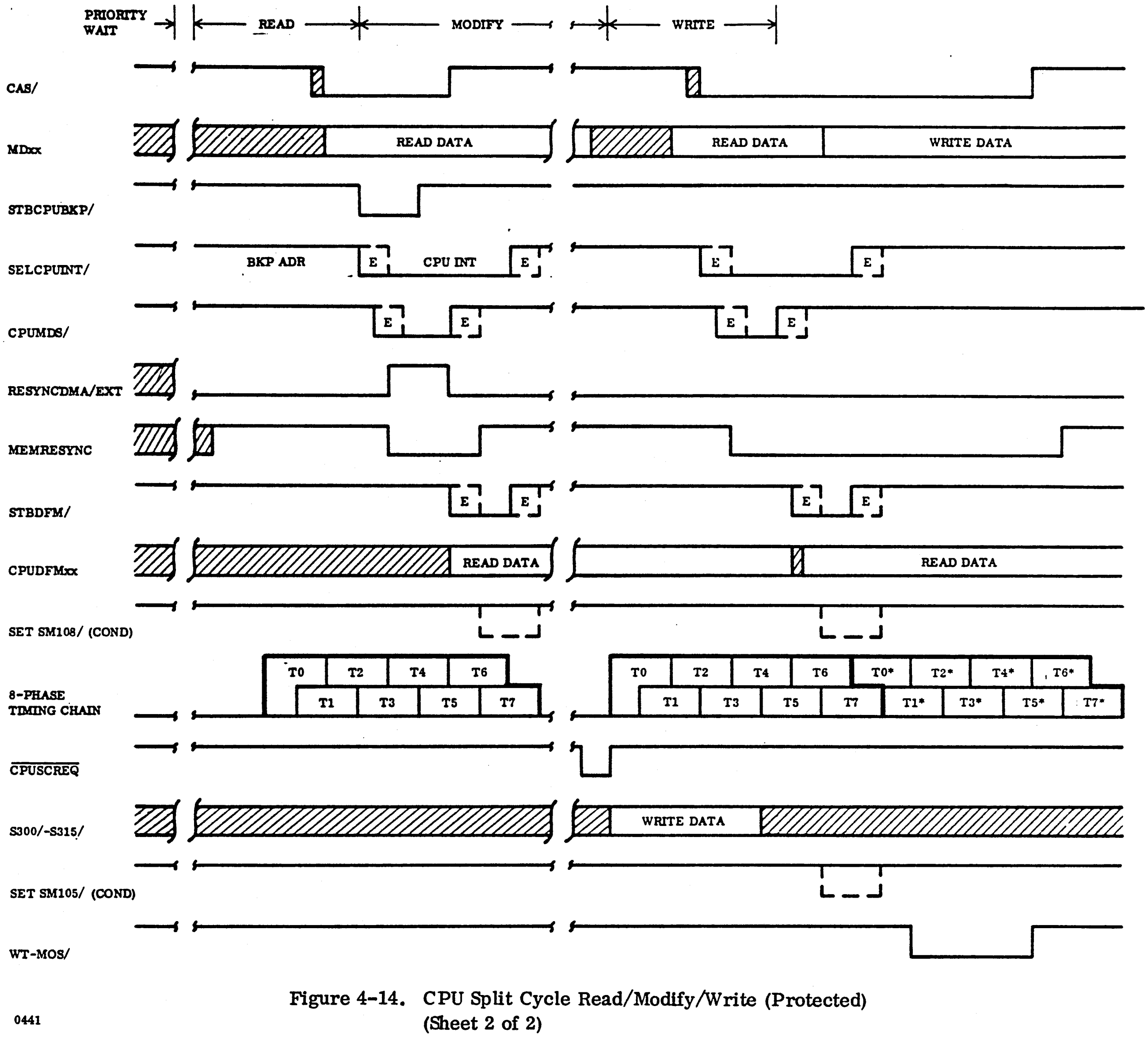


Figure 4-14. CPU Split Cycle Read/Modify/Write (Protected)
(Sheet 2 of 2)

TABLE 4-14. CPU READ/MODIFY/WRITE SPLIT CYCLE (PROTECTED)

Signal	Description
CPUBKPWRT	CPU breakpoint write control line becomes true whenever the CPU-SC/ is false or when the $\overline{\text{CPUWRT}}$ condition is false.
CPUREQ/	CPU memory request. Must stay low until leading edge of first CPUMDS/ signal.
CPU-SC/	CPU split cycle control line. Muststay low from 25 nanoseconds following CPUREQ/ until the first CPUMDS/. Must return false before 10 nanoseconds following change of CPU WRITE to a true level.
CPU WRITE	Read/write control line. Must be low until first CPUMDS/. Change of state to true (high) level initiates write portion of cycle.
STBCPUDFM/	First pulse strobes breakpoint address into CPU output register if previous CPU cycle was a read cycle. Second and third pulses strobe read data into CPU output register.
STRMOSADR	Begins read memory cycle after acceptance of request. Second pulse begins write cycle following initiation by write line.
EN MOSWRTD/	First high portion enables E16KNx-x/ output to memory array for read data. At the start of STRMOSADR in the write portion a low level enables write data input for parity generation. Returns high at T2 time to enable read data from memory, and returns low to enable write data at T6+50 nanoseconds.
E16KNx-x/	Transmit enables (0-1 through 1-4) place read data to MDxx lines.
MOSMAxx	Row and column address lines (00 through 05) to memory arrays.
RAS16Kx-x/	Row address strobes (0-1 through 1-4).
STRCONT	Timing pulse used to set status latches.
T0-T7, T0*-T7*	Eight-phase timing chain. Run once for read portion of split cycle; run twice during write portion. T0*-T7*, the write section of the write cycle, begins at end of T6 without ECC, at end of T7 with ECC.
STCP/EXD/	Strobes write data from S300/ through S315/ into CPU write data storage register.
BLK AB/	Inhibits change of memory address by CPU until split cycle is complete.
$\overline{\text{CPUSC-HLD}}$	Generates resync and inhibit signals to block other requests from priority circuits until split cycle is complete.
RAE/CAE	Row address enabled to MOSMAxx lines when high/ column address when low.
$\overline{\text{SCCLRDMA}}$	Resync pulse at T1 time to priority circuits to clear any waiting DMA request.
CAS/	Column address strobe to memory array. Shaded portion shows early strobe used with fast arrays.
MDxx	Memory data lines 01 through 16 to memory arrays. Contain read data from first T2 time until write line goes high; read data again from the second T2 time until T6+50 nanoseconds (T7+50 nanoseconds with ECC); then write data.
STBCPUBKP/	If previous cycle was a read cycle, leading edge of pulse indicates breakpoint address is available on CPUDFMxx lines until trailing edge.

TABLE 4-14. CPU READ/MODIFY/WRITE SPLIT CYCLE (PROTECTED) (Continued)

Signal	Description
SELCPUINT/	Selects local read data to CPU data output register when low, breakpoint address when high. Data is strobed into register by STBCPUDFM/.
CPUMDS/	Memory data resume. First pulse indicates read data available within 5 nanoseconds after trailing edge on CPUDFMxx lines, and CPU WRITE may go high any time thereafter to begin write cycle. Second pulse indicates control lines from CPU are no longer needed, and that read data from write portion of cycle available 5 nanoseconds after trailing edge.
RESYNCDMA/EXT	Resync pulse during read portion to clear waiting DMA or higher priority requests.
MEMRESYNC	Resync pulses to priority select circuits.
STBDFM/	Timing signals to data interface.
CPUDFMxx	CPU data output lines 01 through 16 from data interface. Contain read data 5 nanoseconds after trailing edges of CPUDMS/.
SET SM108/	Conditional parity error signal. Goes low at T6+50 nanoseconds time if a parity error is detected (T7+50 nanoseconds for ECC double error) on read and write portions.
$\overline{\text{CPUSCREQ}}$	Internal memory request generated to begin write portion of split cycle when write line goes true.
S300/ - S315/	Write data lines from CPU. Must contain write data within 50 nanoseconds after change of write line to true state until following CPUMDS/ signal.
SET SM105/	Conditional protect fault signal. Goes low at T6+50 nanoseconds (T7+50 nanoseconds with ECC) during write portion if a protect fault is detected.
WT-MOS/	Write enable line to memory arrays. True (low) from T2* until T6* time during write cycle.

device chooses not to write new information, thus effectively aborting the write portion of the cycle.

When either or both of the character write control lines are false, a read/write (automatic split cycle) is always performed during a write request, even if protection is disabled by a low ENPRTSYS line.

ABSOLUTE/PAGE MODE

All addresses from the DMA and external ports use a direct 17-bit address, and the DMA devices include an extra line for bank selection so that the full 262K word expanded memory may be addressed. The CPU, however, is limited to a 16-bit address and therefore must use an indirect addressing scheme to fully utilize the MOS memory capability. The page mode is used only for CPU requests.

Absolute mode refers to the use of a direct 16-bit addressing method that the CPU may utilize to access the first 65K bits of memory. Page mode refers to the indirect addressing method in which the least insignificant 11 bits (2K words) are directly addressed but the most significant seven bits are supplied by a random access memory known as the memory page file. Thus the memory is divided into 2K word segments, or pages, with the page address stored in the memory page file.

Up to 64 page addresses may be stored in the file, out of the 128 pages possible. The memory page file is divided into two 32-word locations, with the upper half known as program files (or pages) and the lower half as monitor pages. Each 9-bit word in the memory page file consists of a 7-bit page address, one bit to flag read only pages, and a bit currently unused. The memory page file is accessed and controlled through the micro instruction register lines MIR28' through MIR31'.

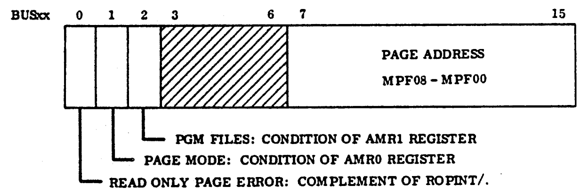
Loading the Memory Page File

Loading of the memory page file is accomplished with the micro command LOAD MPF, which consists of two steps. The first, GATE MPF ADR places the line MIR28' true while the GATEUBDS/ line is brought low, which places the memory page file in a write mode. Next, a standard CPU write operation is commanded, with the memory page file address contained in AB05 (upper half select) through AB00 and the memory page file data in AB15 through AB07. See figure 4-15 for the memory page file loading and address format. While the memory page file is being loaded, the memory executes a dummy read cycle from a location in which the memory page file loading code is interpreted as an absolute address.

If AB08 is true, the read-only page bit is set (see below), prohibiting any further writing to the 2K words within that page in main memory.

Memory Page File Status

The contents of the memory page file may be checked by the micro command READ MPF, which enables the following output of the BUSxx lines:



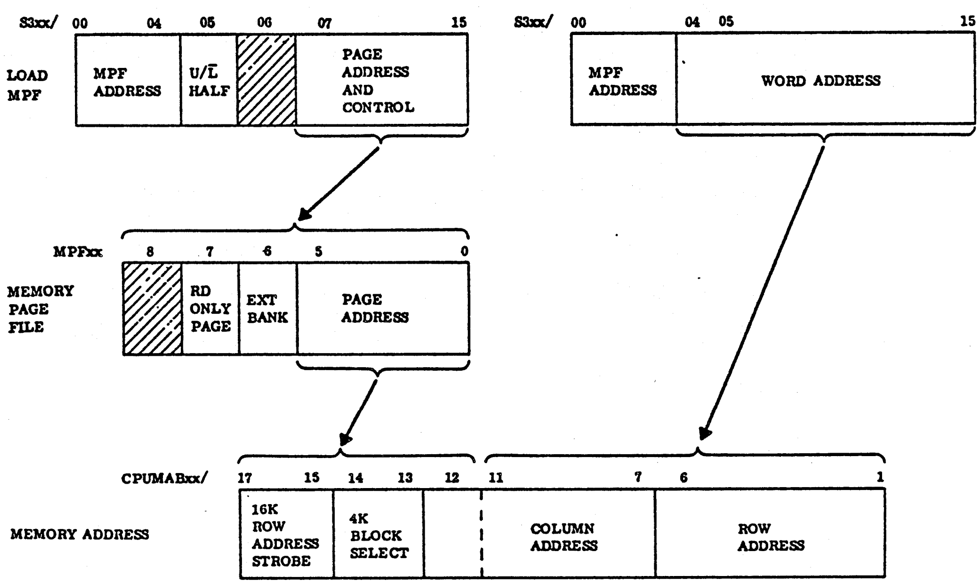


Figure 4-15. Page Mode Address Formats

Page Mode Selection

The page mode is a latched condition that is set with a GATE AMR command (GATEUBDS/, MIR29' true) with MIR30' true, setting the AMR0 register. The page mode remains in force for all subsequent CPU requests until a similar command is given with MIR30' false, or a master clear signal clearing the AMR0 register. The page mode status has no effect on requests from the DMA or external ports.

On the same command the AMR1 register is loaded with the level on the MIR31' line, a true level selecting the upper half or program files, a false level the monitor pages.

Page Mode Read/Write

Once the page mode has been selected, a CPU memory cycle must be preceded in the normal manner by a CPU memory address loading consisting of a GATE AB command, loading the contents of the address register with the contents of lines S300/ through S315/. Lines S300/ through S304/ contain the 5-bit memory page file address, while lines S305/ through S315/ contain the word address within the selected 2K word page.

It is the output of this address register that is compared with the breakpoint address (see Protection, below) to determine an in- or out-of-bounds condition. Thus in page mode the bounds comparison is made against the logical address from the CPU rather than the actual memory address.

Read-Only Pages

If the read-only page bit 7 in the memory page file is set by a true level on line S308/ during loading, all the 2K words within that page become read-only addresses. If an attempt is made to write into a read-only page, the write line is inhibited and the memory executes a read cycle from the same location, and the read-only page interrupt line ROPINT/ is set low. This line remains low until the memory page file is loaded or read, or cleared by a master clear. Note, however, that if a read-only page is located in the first 65K of memory, a write request made using absolute addressing mode will alter the addressed word. Read-only page protection applies in page mode only.

To change the contents of a read-only page the memory page file must be reloaded with the page address, and the read-only page bit false. When the desired changes are made to the page contents, the memory page file must again be reloaded with the same page address and the read-only page bit true. This operation restores the read-only page protection.

MULTILEVEL INDIRECT MODE

If multilevel indirect addressing is selected by the CPU (MULTIND line high) the most significant bit of the CPU address register and both bounds registers is forced false. The following conditions would then apply:

- Absolute mode — The CPU maximum addressable physical memory is the least significant 32K words of the local bank, as only a 15-bit address is being utilized. Note that since the breakpoint comparison addresses are affected also, even if the in-bounds segment is in the second 32K of memory a duplicate in-bounds segment is established in the first 32K when in multilevel indirect mode.
- Page mode — The addressable pages are limited to the least significant 16 monitor pages and 16 program pages, thus limiting the immediate addressing space to 65K words. However, each page may be located anywhere in the possible 262K of memory.

PROTECTION

Memory protection is a method of identifying certain words or groups of words as being protected from ordinary write operations. Two methods are used in the MOS memory: the read-only page protection previously discussed in this section, which applies only to CPU page mode write requests, and the protect bit. Read-only page protection is the highest priority protection, and the protect bit is unimportant until the read-only page protection is removed.

The protect bit is stored along with the data word in the most significant bit position (bit 17) of the 18-bit memory word. When the protect bit is true, the word is considered a protected location. Read operations are not affected by the condition of the protect bit, but will provide the status of the protect bit over the lines MEMPROTBT/ to the CPU port, DMAMPB/ to the DMA port, or PRF/MPB to the external port. (An exception to this is that on a CPU in-bound condition, the MEMPROTBT/ line is false regardless of the status of the protect bit.) Timing for the memory protect bit output is the same as for read data output for the type of cycle requested.

Protect Bit Write

To change the condition of the protect bit, the write protect bit line from the requesting port must be true and a write cycle must be requested. The protect bit then assumes the level of bit 10 (on a scale of 1 through 16, with 1 LSB) in the incoming write data word:

Port	Protect Bit Write Line	Bit 10 Line
CPU	CPUWRTPB	S306/ (inverted)
DMA	DMAWRTPB	DMAD10/ (inverted)
External	EXTWPBIN	XI10

The condition of the protect bit remains unchanged through subsequent write operations until the write protect bit function is again employed. (Exception: ENPRTSYS line low; see below.) A protect bit write operation is aborted if a parity error exists.

Write Operations to Protected Location

To write to a protected location requires a true program protect line during the write operation. The condition of the protect bit remains unchanged unless a protect bit write operation is requested.

Port	Program Protect Line
CPU	CPUPROTECT/
DMA	DMAPROT/
External	PRF/MPB

Writing to a protected location without a true protect line may only be accomplished when the ENPRTSYS line is low, which disables the normal protection system, and on a CPU in-bounds condition (see below).

Protect Faults

When write operations to a protected location are attempted, and the conditions discussed above for a successful write operation are not met, the write operation is aborted (the write cycle is completed, but the write enable line WT-MOS/ to the memory arrays is inhibited).

A protect fault signal is also generated to the requesting port to indicate the aborted operation. Timing for protect fault signals for the various types of write cycles are shown in the timing diagrams earlier in this section.

Port	Protect Fault Line
CPU	SET SM105/
DMA	DMA-PF/
External	CH0/PF

CPU Bounds Address Operation

The CPU may establish up to 65K of memory as an unprotected area. The bounds addresses are loaded into the upper or lower bounds registers by the GATEUBDS/ or GATELBDS/ signals, respectively, which load the selected register with the contents of the multipurpose lines S300/ through S315/. This operation may be made at any time except when a CPU memory request is active.

When an absolute address is loaded into the CPU address register by the GATEAB/ signal, that address is compared against the addresses in the bounds registers. When the address is lower than the upper bounds address and higher than the lower bounds address, the location is considered to be in bounds.

On a write cycle, an in-bounds condition has exactly the same effect as if the program protect line were true. There is no effect upon a read cycle.

In page mode, the bounds area refers to a location within the memory page file rather than a physical memory location. Therefore, the protected area may be scattered throughout the physical memory. In general, a bounds area should not be established (set upper bounds to zero) if absolute and page mode addressing are to be intermixed.

Protection System Disable

The ENPRTSYS line may be brought low to cause the entire memory to be unprotected. Write requests from the CPU, DMA, or external ports are executed regardless of the state of the protect bit, except to a read-only page in page mode. When protection is disabled, a shortened write cycle is employed on full word write requests, and the protect bit is set true in each memory location referenced. There is no effect on a read operation.

If the external bank is referenced, the write operation is still executed regardless of the state of the protect bit, but the short cycle and the setting of the protect bit does not take place unless the ENPRTSYS line is also low on the external bank. In general, however, the ENPRTSYS lines to the two banks are at the same level.

ERROR DETECTION (PARITY AND ECC)

Error detection in the MOS memory is accomplished by a parity bit stored with each data word. The parity bit is set to produce an odd parity (odd number of 1s) in the 18-bit memory word. The use of a parity bit detects single bit errors, which are the most common.

An optional feature in the MOS memory is the error checking and correction (ECC) system. The ECC system uses five check bits in addition to the parity bit, and by this means can determine the source of a single error and enforce a correction. ECC theory is discussed in detail under Error Detection and Correction.

Word Parity

A word parity bit is generated for each 16-bit write data word received by the data interface to generate an odd parity. This parity bit has no effect upon memory operation, but is fed back to the requesting port so that the requesting device can determine if the data word was received correctly. Timing for the word parity output is the same as the read data output for the type of cycle requested.

Port	Word Parity Output Line
CPU	EVENPAR
DMA	DMAMPL/
External	SC/MPL

Parity Error (Without ECC)

The parity bit generated to be stored in memory bit 16 differs from the word parity bit in that the parity includes the protect bit. Therefore, the memory parity bit is the same as the word parity bit if the protect bit is false, and the complement of the word parity bit if the protect bit is true.

A parity error is detected by regenerating a word parity bit from the 16 bits in the data word read from memory. Parity is then determined by the three bits: word parity, memory parity (bit 16), and the protect bit (bit 17). An even parity among these three bits passes the test; an odd parity indicates an error.

Parity error signals are available to the requesting device on both read and normal write cycles. Timing for the various cycles is shown in the appropriate timing diagram earlier in this section.

Port	Parity Error Output Line
CPU	SET SM108/
DMA	DMAMPE/
External	CH1/$\overline{\text{PE}}$

On normal write cycles, the write portion of the cycle is aborted if a parity error is detected on the read portion unless the protect line is true or protection is otherwise disabled.

ECC Error Correction and Reporting

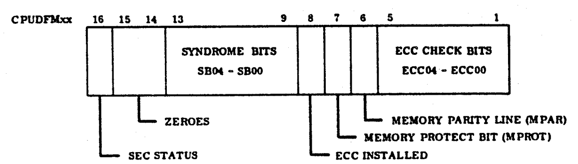
When the ECC option is installed, the ECC check bits are read on a read cycle or the read portion of a write cycle. New check bits are generated from the read data and compared against those read. Any discrepancy results in the generation of a 5-bit code known as syndrome bits, and these are decoded to determine the source of error. A full description of the theory used for ECC is given under Error Detection and Correction.

Once the source of a single-bit error is determined, the faulty bit is complemented, correcting the error. The line SEC STATUS/ is set low and stays low until the CPU issues the GATE ECC STATUS command (see below). The parity error line does not go true on a single bit error, nor is the write portion of a write cycle aborted.

Some ECC error codes indicate that more than one bit is affected. Since a single-bit error should result in a bad parity (with ECC, the parity includes the five check bits), then if parity is OK a double error has been detected. This condition is signalled to the requesting port in exactly the same manner as a parity error without ECC; i.e., the parity error line is brought true and write operations may be aborted depending upon program protect status.

ECC Status

The status of the local bank ECC signals may be referenced by the CPU at any time with a GATE ECC STATUS command (GATELBDS/ and MIR28' true). This command places status information on the CPUDFMxx outputs according to the following format:



ECC status information remains selected to the CPUDFMxx outputs until a GATEAB command is received. ECC status information is not available from the external bank. SEC STATUS is cleared after the completion of every GATE ECC STATUS command.

DUAL CPU OPERATION

A CPU may be connected to each CPU port in a dual bank system. Although both ports may operate independently, certain control lines should be tied together on the two ports and controlled by one of the two CPUs, designated as the master. These lines are:

- MC/ — Master clear; both banks should be cleared simultaneously
- ENPRTSYS — Enable protect system

ADDRESS AND CONTROL INTERFACE

GENERAL

The address and control interface board provides the timing and control for the MOS memory, the handling and decoding of memory addresses, and the priority selection of incoming memory cycle requests. Refer to the simplified block diagram of figure 4-16.

The delay line oscillator generates an on-board eight-phase timing chain that produces the primary timing signals to the control logic.

A power-on master clear/Master Clear from the CPU resets many of the latches in the control logic to provide a fresh start when necessary without disturbing memory. Data stored in memory is volatile only during power on/off without battery backup.

The control and timing logic receives control information from the CPU, DMA, and external inputs, synchronizes subsequent memory operation to the eight-phase timing chain, and transmits status control signals back to the requesting device. The control and timing logic also adjusts the memory timing to account for the response time of the memory arrays and provides for a time delay for the ECC to operate if installed.

The address and control interface also contains a refresh timer and address counter, refreshing all row addresses in the MOS memory array approximately every two milliseconds.

Priority select circuits operate on the memory request signals from the CPU, the four DMA inputs, the external memory port, and the refresh timer. The highest priority active request is determined, and the appropriate port selected to provide the memory address, data, and read/write request.

The read/write logic on the address and control interface produces the control signals for the array boards.

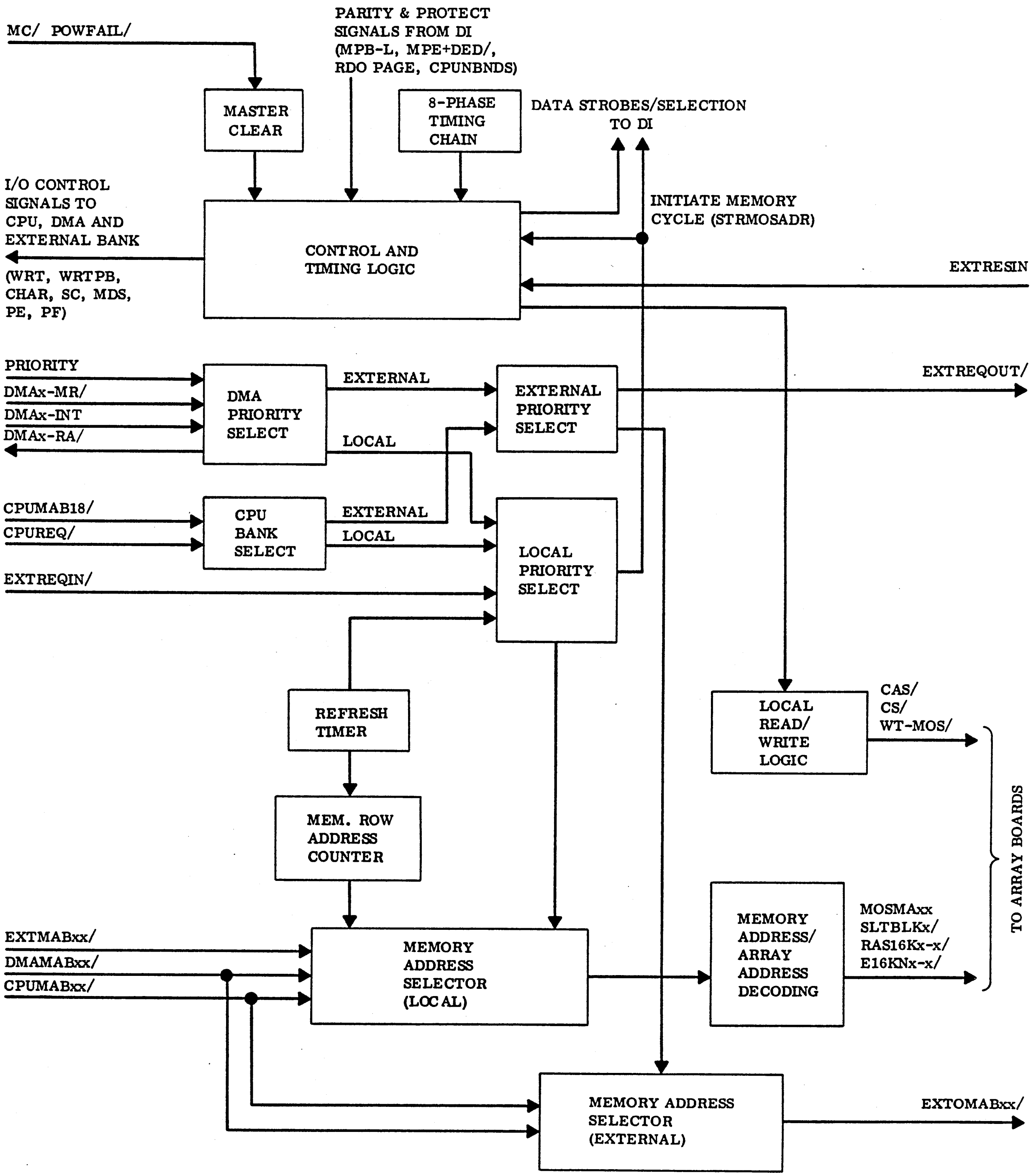


Figure 4-16. Address and Control Interface Simplified Block Diagram

Memory address signals from the three ports (DMA, external, CPU) and the refresh address counter appear at the inputs to the memory address register/selector. One of the four inputs is selected by the priority select circuits. The selected address is then fed to the local bank selector. If the external memory bank is requested by bit 18 of the CPU memory address or by a false DMA-INT signal, the priority is determined between DMA and CPU and the address is routed to the external memory bus output.

If the local bank is selected, the address is routed to the memory address /MOS array address decoding circuits. These circuits interpret the 17-bit memory address into the array board, block, row, and column information needed by the array cards.

PORT SIGNALS AND TIMING

CPU Port

Activity at the CPU port begins with the loading of the least significant 11 bits of the memory address from CPU data lines S305/ through S315/ into the CPU address register, coincident with the GATEAB/ signal from the CPU. (The most significant bits are simultaneously loaded on the data interface board and are available to the address and control interface board over lines CPUMAB12/ through CPUMAB18/.) The CPU then initiates a memory cycle request with a low level on CPUREQ. Within 25 nanoseconds following the leading (negative going) edge of this signal, these control lines from the CPU must be at their proper value for the instruction:

CPU WRITE	High for WRITE, low for READ
CHAR0 and CHAR1	Both high for word read or write
CPU-SC/	Low for split cycle operation
CPUWRTPB	High to write protect bit
CPU PROTECT/	Low for program protect

All of these lines, including CPUREQ/, must remain stable until the CPUMDS/ line goes low, signaling the CPU that all information from the CPU has been acted upon.

The CPUMDS/ line goes low for approximately 100 nanoseconds after the CPU request has been honored and the memory array addressed.

Several memory cycles may lapse between CPUREQ/ and CPUMDS/ under heavily loaded conditions due to the low priority of the CPU. If the memory address is for the external bank, both the priority selection for the CPU-external in the local MOS memory and the external priority selection in the external MOS memory must be satisfied before the requested cycle is completed.

Following the CPUMDS/ output, the results of a parity test failure (SET SM108/ low) and, on a write cycle, the protect fault indication (SET SM105/ low) appear on the appropriate lines to the CPU as approximately 100-nanosecond wide pulses. Read data and memory parity is also available from the data interface CPU port following the CPUMDS/ output.

When a CPU split cycle request has been made, the first CPUMDS/ output signals the CPU that the read portion of the cycle has been executed. The beginning of the write portion occurs when the CPU WRITE line changes from a low to a high state, after which a second CPUMDS/ signal is generated by the address and control interface to signal completion of the entire cycle.

The CPU port also includes the input lines MC/ (master clear), which resets the latches in the interface, and POWFAIL/, which holds the memory interface latches in a reset condition with the exception of the refresh control logic until power is restored to the CPU.

The line ENPRTSYS, when forced low by the CPU, overrides the usual protection methods and executes a full write cycle regardless of the state of the protect bit or DMA or CPU program protect lines.

Three clock lines from the CPU to the MOS memory (T0/, T2ODDCLOCK/, and T3-$\overline{\text{MEM}}$/) speed the CPU memory cycle by providing a resync window for the CPUREQ signal to memory logic so that a new request can be acknowledged in the shortest possible time.

DMA Ports

Up to four peripherals may have direct memory access (DMA) to the MOS memory. Each has its own memory request line, labelled DMA1-MR/ through DMA4-MR/. The cycle begins with one or more of these memory request lines going low. Coincident with the memory request, the DMA device must indicate whether the internal or external memory bank is to be selected. The appropriate bank line DMA1-INT through DMA4-INT must be high for internal, and low for selection of the external bank. If the external bank is selected but no external bank is connected, the DMA memory address error line DMA-MAE/ is forced low, and the reference is made to the same address in the local bank with write inhibited.

The request with highest priority (DMA1-MR/ is highest) is accepted and the address and control interface responds with an appropriate request accept signal (DMA1-RA/ to DMA4-RA/ low).

If the optional PRIORITY/ line is low, only the DMA input selected by switch S10 (location BC1 on the board) is recognized. All other DMA, CPU, or external requests are locked out, with only a refresh or the completion of a split cycle (read/modify/write) operation taking priority. In this manner, a priority DMA can be guaranteed a specific response time if split cycle and refresh operation are allowed for.

Within 50 nanoseconds following the DMA-RA/ leading edge, the appropriate DMA device must place the proper signal levels on the common DMA control lines to execute the desired type of memory cycle:

DMA WRITE	High for WRITE, low for READ
DMAPROT/	Low for program protect
DMAMAB01/ through DMAMAB17/	Memory address lines
DMA-SC/	Low for split cycle (read/modify/write)
DMA-CHAR0/, DMA-CHAR1/	Both high for word read or write
DMA-WRTPB/	Low to write protect bit

All of these lines must remain stable as long as the DMA-RA/ line stays low, except for the DMA WRITE line in read/modify/write operation, which goes high after the address and control interface generates the first DMA-MDS/ output to initiate the write portion of the cycle.

The DMA-MDS/ line goes low for approximately 100 nanoseconds after the DMA request has been honored and the memory array addressed. Following the DMA-MDS/ output, the results of a parity test failure (DMA-MPE/ low) and, on a write cycle, the protect fault indication (DMA-PF/ low), appear on the appropriate lines to the DMA as approximately 100-nanosecond wide pulses. Read data and memory parity is also available from the data interface DMA port following the DMA-MDS/ output.

When a DMA read/modify/write request has been made, the first DMA-MDS/ output signals the DMA device that the read portion of the cycle has been executed. The beginning of the write portion occurs when the DMA WRITE line changes from a low to a high state, after which a second DMA-MDS/ is generated. The return of the DMA-RA/ signal to a high status signals the completion of the entire cycle.

The line ENPRTSYS, when low, also affects DMA operation by overriding the usual protection method, allowing execution of a full write cycle regardless of the state of the protect bit or the DMA program protect line (DMAPROT/).

External Port

The external port is bidirectional and is used for both output and input:

- To communicate CPU or DMA read/write commands to the external memory bank (external request out)
- To receive and act upon read/write commands from the external bank when the external bank has its own DMA or CPU requests (external request in)

The two operations may be processed simultaneously.

A DMA or CPU external bank request is initiated as described above for DMA and CPU port timing. External bank selection is made by the appropriate DMA-INT line or CPUMAB18/ line in a low state. The write, memory address, split cycle, character, protect bit, and program protect lines must all meet the same requirements as for a local bank request.

After priority selection between DMA and CPU, the EXTREQOUT/ line to the external bank goes low, and the appropriate DMA or CPU memory address bus lines are gated onto the lines EXTOMAB01/ through EXTOMAB17/, as well as the following control lines:

DMA	CPU	Gated to External Output Line
DMA WRITE	CPU WRITE	EXTWRTOUT
DMA-SC/	CPU-SC/	MPL/SC
DMACHAR0, 1	CHAR0, 1	PF/CH0, $\overline{PE}$/CH1
DMAWRTPB/	CPUWRTPB/	EXTWPBOUT
DMAPROT/	CPU PROTECT/	MPB/PRF

The external bank receives the EXTREQOUT/ at its EXTREQIN/ input and, after the possible processing of a refresh request or the completion of a split cycle operation, processes the entered request based on these input lines of address and control information from the local requesting bank:

Local Bank Outputs	External Bank Inputs
EXTOMAB04/ - EXTOMAB17/	EXTIMAB01/ - EXTIMAB17/
EXTWRTOUT	EXTWRTIN
MPL/SC	SC/MPL
PF/CH0	CH0/PF
$\overline{PE}$/CH1	CH1/$\overline{PE}$
EXTWPBOUT	EXTWPBIN
MPB/PRF	PRF/MPB

Following the acceptance of the external request, the memory completes the read or write cycle and sends back to the local memory the signal EXTRESOUT/, followed by this status information:

External Bank Outputs	Local Bank Inputs
SC/MPL	MPL/SC
CH0/PF	PF/CH0
CH1/$\overline{PE}$	$\overline{PE}$/CH1
PRF/MPB	MPB/PRF

The EXTRESOUT/ signal is received by the local bank on the EXTRESIN/ line. The address and control interface in turn generates a CPUMDS/ or DMA-MDS/ signal to the requesting port, followed by the appropriate conditional parity error or protect fault signals.

REFRESH TIMER

The MOS memory circuits used in the memory arrays require a refresh signal at least every two milliseconds. In this MOS memory, the refresh oscillator is set for approximately 15.6 microseconds. At each timer cycle one count is added to a seven-stage binary counter. The output of the first stage in the refresh counter is the line REFMAB15/, and the remaining six stages form lines REFMAB01/ through REFMAB06/. Since refreshing is made an entire row at a time, the column addresses formed by MAB07 through MAB12 are not needed (see Memory Address Bus/Array Address Decoding below), nor are the block selects and transmit enables usually formed by MAB13 and MAB14 and MAB16 and MAB17.

Therefore, 1/128 of the memory is refreshed at each timer cycle, representing one row out of 64 in each memory chip on each of the two sets of row address strobes. With 128 cycles at 15.6 microseconds per cycle, an entire memory array board is refreshed each 2 milliseconds. At each cycle of the timer the refresh request latch is set, requesting a memory refresh cycle at the input to the priority logic.

PRIORITY SELECTION

Priority selection among local bank requests takes place in the following order:

1. Refresh request
2. Priority DMA request: switch-selected DMA request and PRIORITY/ line low
3. External bank request from a remote DMA or CPU
4. DMA request, with DMA 1 having highest priority and DMA 4 the lowest
5. CPU request

If a local CPU or DMA request addresses the external bank, the priority is handled separately, as discussed below.

Refresh Priority

Refresh requests are made directly from the refresh timer approximately every 15.6 microseconds. Since it is known that only one request will be made during the period the refresh can be given highest priority. As the refresh select latch is set, the request is honored immediately after the completion of the existing cycle. At that time, the eight-phase timing chain is started, the refresh address to the memory address register is selected, and the CS/ line to the memory array held high, which places the memory circuits in the refresh mode. The refresh select latch is then cleared.

External Priority

Requests from the external bank DMAs or CPU appear as an EXTREQIN/ signal and set the external request latch. At the conclusion of the current memory cycle, if neither the PRIORITY/ line is low, a refresh request is not active and a DMA or CPU read/modify/write cycle is not in process, the eight-phase timing chain is started, the EXTIMAB/ address to the memory address register is selected and the EXTREQACT/ line to the data interface is forced low so that external data will be processed.

DMA Priority

Requests from the four DMA subports appear as low levels on DMA1-MR/, DMA2-MR/, etc. The first step in DMA priority selection is to determine which of two or more simultaneous DMA requests is to be processed first. DMA1 has the highest priority, DMA4 the lowest. The one selected is sent a request accept signal (DMA1-RA/, DMA2-RA/, etc.) so that the selected DMA device can place its data, memory address, and control information on the common DMA lines. At the same time, the appropriate DMA-INT line is checked to see whether the local or external bank is being selected.

If the DMA device has chosen the external bank, the DMA external select latch is set, an EXTREQOUT/ signal is sent to the external bank assuming no CPU external request is in process, the DMA-MAB address lines to the memory address register are gated to the EXTOMAB lines to the external bank, and the ENDMWRTDO/ line (enable DMA write data out) to the data interface is pulled low to gate the DMA data to the external bank.

If the DMA chooses the internal bank, the DMA-local latch is set. At the conclusion of the current memory cycle, if there is no existing refresh or external request waiting, the eight-phase timing chain is started, the DMAMAB address to the memory address register is selected, and the DMAREQACT/ line to the data interface is pulled low so that DMA data will be processed.

An exception to the priority scheme occurs following a DMA read or full write memory cycle. If both a CPU and DMA request are waiting at that time, the CPU is processed first, its latch having been set before the DMA latch has been cleared and reset with the new request.

If the PRIORITY/ line is brought low by a DMA peripheral, only the DMA device selected by switch S10 on the address and control interface board can trigger a memory cycle. External requests, CPU requests, and all other DMA requests are all gated out. Refresh requests, however, are allowed to carry on in their normal manner.

CPU Priority

At the bottom of the priority list is the CPU memory request. Since CPU requests normally make up the vast majority of incoming requests they could easily monopolize the memory if given any higher priority.

The CPU request (CPUREQ/ low) is honored when:

- No higher priority request is active, or
- On an internal request, a DMA cycle has just been completed, no refresh or external request is active, and the PRIORITY/ line is high.

If the CPU chooses the local memory bank (CPUMAB18/ high) the eight-phase timing chain is started and the CPUMAB addresses to the memory address register are selected. The data interface interprets the lack of an EXTREQACT/ or DMAREQACT/ to mean that CPU information is to be processed.

If the CPU chooses the external memory bank, the CPU external select latch is set if no external data request is active, an EXTREQOUT/ signal is sent to the external bank, the CPUMAB address lines to the memory address register are gated to the EXTOMAB lines to the external bank, and the ENCPWRTDO/ (enable CPU write data out) line to the data interface is pulled low to gate CPU data to the external bank.

MEMORY ADDRESS BUS/ARRAY ADDRESS DECODING

Memory Address Register/Selector

The four memory address inputs from the refresh address counter, the CPU, the DMA memory address bus, and the external-in memory address bus are applied to the inputs of a one-of-four selector. In addition to the 17 memory address lines, the following control lines are selected by the same selector:

1. Split cycle
2. Program protect
3. Character 0
4. Character 1
5. Write
6. Write protect bit

Refresh Addresses

Address lines REFMAB01/ through REFMAB06/ and REFMAB15/ are supplied by the refresh address counter. The remaining inputs are unused.

CPU Addresses

The data lines S305/ through S315/, representing the 11 least significant bits of the memory address, are gated into a latch by the GATEAB/ line from the CPU. The outputs of the latch represent the lines CPUMAB11/ through CPUMAB01/, respectively. The lines CPUMAB12/ through CPUMAB17/ are supplied by the data interface. The line CPUMAB18/, also supplied by the data interface, is not fed to the selector, but to the bank selector. It selects the internal bank if high, the external bank if low.

DMA Addresses

The DMA address lines DMAMAB01/ through DMAMAB17/ are supplied by the common DMA memory address bus to the inputs of the selector.

External Addresses

The address lines from the external bank EXTIMAB01/ through EXTIMAB17/ are available to the inputs of the address selector from the external bank I/O cable.

Selection among the four inputs is determined by the decision of the priority logic.

Array Address Decoding

The array organization is explained in detail under Memory. The contents of the 17-bit memory address are shown below:

MAB	17 15	14 13	12 7	6 1
	ROW ADDRESS STROBE (RAS)	SELECT 4K BLOCK	COLUMN ADDRESS	ROW ADDRESS

The least significant six bits of the memory address (MAB01 through MAB06) are strobed into the row address register, and the next significant six bits (MAB07 through MAB12) into the column address register, by the same signal generated at the end of the priority decoding that starts the eight-phase timing chain (STRMOSADR).

The six row address bits are sent to the array along with a row address strobe (RAS) on lines MOSMA00 through MOSMA05. This address is stored in the array. Next, the six column address bits are sent along the same MOSMA00 through MOSMA05 lines with the column address strobe (CAS/). The 12 bits select a single 18-bit word from one 4K word block.

The next most significant memory address bits, MAB13 and MAB14, are decoded to select one of four 4K memory blocks, by energizing one of the lines SLTBLK0/ through SLTBLK3/.

The most significant three bits, MAB15 through MAB17, are decoded to select one of eight row address strobes, each one directed to a set of four 4K memory blocks. Thus, the memory address bus addresses eight 16K-word memory sections for a total of 131K words.

In the refresh mode, the four block select lines are all energized, and the eight row address strobes are tied together in two groups of four, the groups alternated by the level on line REFMAB15/, thus selecting a row in half the memory chips on each MOS array board on each cycle.

Bank Selection and Memory Address Error

External bank selection is made by the CPU by a low level on line CPUMAB18/ at the time of a CPU memory request. If no external bank is connected, a read request is made from the same address in the internal bank, and a write request is aborted.

DMA requests for the external bank are made by a low level on the appropriate DMA-INT line from the same device as that selected by the priority select gates. If no external bank is connected, a read request results in a read cycle from the same address in the local bank and a write request is aborted. In addition, control line DMA-MAE/ to the common DMA bus is set low as a warning to the DMA device.

CONTROL LOGIC AND TIMING

Eight-Phase Timing Chain

The eight-phase timing chain controls the timing of activities in the MOS memory. It consists of two four-bit counters driven by a delay line oscillator, that produces an eight-phase, overlapping timing chain. Timing on the oscillator is controlled by a delay line, which sets the frequency at approximatey 12.5 MHz. The timing chain diagram is shown in section 5, along with the abbreviated representation used in the read/write cycle timing diagram.

The timing chain provides complementary outputs for each clock signal.

The oscillator is started with the signal STRMOSADR after the priority logic has selected the appropriate incoming request. This in turn starts the timing chain, which normally ends with the completion of the T7 signal. In automatic split cycle write, used in character write and split cycle protected mode (ENPRTSYS enabled), the cycle is run two times, with the leading edge of the T0 pulse coincident with the trailing edge of the T6 pulse.

The clock rate is increased if fast memory arrays are used. The selection of speed, either 40 nanoseconds or 50 nanoseconds between successive timing chain pulses, is made by straps on the array boards. Any slow array board pulls the common ENMOS-250 line low, which selects a 10-nanosecond later tap on the clock timing delay line.

I/O Time Delay Selection

Time delays are incorporated in the priority select logic and read/write timing to allow for resynchronizing and differences in response time from the requesting devices. An 80-nanosecond delay is incorporated in the DMA priority select circuits to allow for resynchronizing the selected DMA device and to provide time for the selected DMA to respond to the DMA-RA/ request acceptance signal. An additional 50-nanosecond delay is incorporated after priority selection of DMA or external requests before the STRMOSADR signal is generated to allow time for the data, address, and control lines to switch from CPU selection to external, DMA, or refresh select.

If the memory is not busy, a window is generated by CPU clock signals T0/ and T3-$\overline{\text{MEM}}$/ to allow resynchronizing a CPU request with respect to a DMA, external, or refresh request, which allows for faster access to memory for CPU cycles.

Read/Write Timing

The memory cycle begins with the STRMOSADR signal generated by the priority logic. At this time the selected incoming memory address lines are clocked into the row and column address registers, the decoded block select address register, and the decoders for the row address strobe and the transmit enables. After a 30-nanosecond delay, the output of the row address strobe decoder is enabled by the $\overline{\text{ENRAS}}$ line, completing the selection of the 4K block in the memory array plus the row address.

Another 20 nanoseconds later (or 70 nanoseconds for a CPU full cycle write), the eight-phase timing chain is started and the line STRCONT is energized, which clocks on the DMAREQACT/ or EXTREACT/ lines, locks up incoming memory control lines if appropriate, and the STCP/EXD/ strobe to the data selectors on the data interface board. The determination of full or split cycle operation is made at this time. (The remainder of the section assumes full cycle operation.)

At T1 time, the column address from lines MAB07 through MAB12 are placed on the lines MOSMA00 through MOSMA05. A CPU-MDS/ signal is sent to the CPU if it is on a CPU full write cycle.

At T2 time, the column address strobe (CAS/) is sent to the array, the read/write function is determined, and either the WT-MOS/ signal is sent to the array for a write cycle, or the appropriate transmit enable line (E16KN0-1/ through E16KN1-4/) on a read cycle.

At T3 time, the signal STBCPUBKP/ is sent to the CPU on a CPU cycle to indicate that breakpoint address is available on the CPUDFMxx lines. The CPU-MDS/ signal is sent to the CPU for a CPU read or split cycle (T4 is used if an ECC board is employed).

At T4 time, the RESYNCDMA/EXT line is energized on all but a CPU cycle, resetting the input latches for refresh, DMA, and external priority selection. On external requests, the external resume signal EXTRESO/ is sent to the external bank (T5 is used if an ECC board is employed).

At T6 time (T7 if ECC is used), the DMA-MDS/ signal is sent to the DMA devices and the STBDMADFM/ signal is sent to the data interface on a DMA cycle, the STBCPUDFM/ signal is sent on a CPU cycle, or the ENEXTRDO/ is sent on an external cycle.

After a 50-nanosecond delay following T6 (or T7) the RESYNCDMA line resets the DMA priority select latches and the following conditional signals are activated as appropriate:

SET SM105/ (CPU protect fault)
DMA-PF/
DMA-MPE/
SET SM108/ (CPU parity error)

At T7, the line MEMRESYNC goes positive, resetting priority latches, and on the trailing edge of T7 the line MEMHALT goes high, turning off the oscillator and allowing the next memory request to start a new cycle.

Split Cycle Operation

Two types of split cycle operation are encountered—one is generated by a split cycle request (read/modify/write), and the second is an automatic split cycle generated by a character write request or whenever the ENPRTSYS line is true.

Read/modify/write split cycle operation is selected by the CPU-SC/, DMA-SC/, or SC/MPL (external) split cycle request lines. At T0 time, the following lines are brought low:

- $\overline{\text{CPUSC-HLD}}$ — on a CPU split cycle request, locks out DMA and higher priority requests until the split cycle is complete.
- $\overline{\text{DMASC-HLD}}$ — On a DMA split cycle request, locks out requests from other DMA devices until the split cycle is complete.
- $\overline{\text{CPU/EXT-SC}}$ — On a CPU or external split cycle request, locks out a new DMA request.
- $\overline{\text{CPDMSC/PR}}$ — On a CPU or DMA split cycle request, or a DMA priority request, locks out a new external request.
- $\overline{\text{DMA+EXT SC}}$ — On a DMA or external split cycle request, locks out a local CPU request and inhibits the window given a CPU request by the CPU clock.

At T1 time on a CPU split cycle request, the line SCCLRDMA/ clears out any DMA or higher priority request that may have already been latched in the priority circuits.

The read portion of the split cycle continues to completion. As the write line from the selected DMA or CPU port goes high, a new request is generated by the split cycle logic to begin the write cycle:

- On a CPU split cycle request, the line $\overline{\text{CPUSCREQ}}$ is brought low, starting a new cycle.
- On a DMA split cycle request, the line $\overline{\text{DMASCREQ}}$ is brought low, starting a new cycle.

- On an external split cycle request, the cycle is completed and the EXTRESOUT/ signal is returned to the external bank. The external bank then generates a new external request, beginning the second half of the split cycle.

A forced, or automatic, split cycle occurs when a character write or protect bit write is requested or the ENPRTSYS line is high during a write request. Here, the normal WT-MOS/ signal to the array is inhibited and a read cycle is made. The eight-phase timing chain is restarted after T6 time (T7 time with ECC), continuing on so that a second cycle is begun immediately. At T2 time the second time around, the WT-MOS/ line is brought low, causing a write cycle to be accomplished. The usual split cycle request inhibits are not needed, as the MEMHALT line does not go high until the second cycle.

In the character write or protect bit write mode, the purpose of the automatic split cycle is to read the contents of the selected memory location into the data interface, so that the character or word (protect bit write) that is not to be changed by the write operation is restored as the other character or protect bit is written.

In the ENPRTSYS (enable protect system) mode, the read portion of the cycle permits the reading of the protect and parity bits. The lines MPE+DED/ and MPB-L from the data interface abort the write portion of the cycle if the program protect input line is true and the protect bit is false by inhibiting the WT-MOS/ output to the array.

CPU or DMA External Bank Timing

CPU or DMA read or write requests specifying the external bank are handled asynchronously by the local address and control interface. Requests are handled without delay, except for priority selection between DMA-external and CPU-external requests. The EXTREQOUT/ is set low, the proper address gated to the EXTOMAB lines, and either the ENCPWRTDO/ (for the CPU) or ENDMWRTDO/ (for the DMA) line to the data interface set low for the gating of write data to the external bank.

As the EXTRESIN/ line goes low after the completion of the cycle by the external bank, the STRCPUBKP/ line to the CPU goes low to a CPU cycle. After a slight delay either the STBCPUDFM/ or STBDMADFM/ line goes low as well as CPU-MDS/ or DMA-MDS/, followed by the appropriate parity or protect fault conditional signals.

This completes the cycle, except for read/modify/write split cycle requests, which generate a second external bank request when the appropriate write line goes high.

ADDRESS AND CONTROL INTERFACE INTERNAL SIGNALS

Referenced signals contained entirely within the address and control interface board are described in table 4-15.

DATA INTERFACE

The data interface board provides the read and write data handling for the MOS Memory, generates and detects parity and ECC signals, and controls CPU addressing and bounds comparison. Timing for the data interface is supplied by the address and control interface. Note the simplified block diagram of figure 4-17.

Incoming CPU addresses are processed by the data interface. Page or absolute mode is determined by commands from the CPU micro instruction register, and the data interface supplies the most significant six bits of the 17-bit CPU memory address plus the bank select bit to the address and control interface. These bits are either selected from the incoming data in absolute mode or from the memory page file in page mode. The data interface also loads and stores bounds addresses used to establish unprotected areas available to the CPU and makes the comparison against those bounds with incoming CPU addresses.

TABLE 4-15. ADDRESS AND CONTROL INTERFACE INTERNAL SIGNALS

Signal	Description
$\overline{\text{CAE}}$	Column address enable. Sends MAB bits 07 through 12 to array.
$\overline{\text{CPDMSC/PR}}$	Inhibits a new external request.
CPUACT	Indicates a DMA or higher priority request is not active.
$\overline{\text{CPUACT}}$	Pulse coincident with start of CPU memory cycle. Not a complement of CPUACT.
CPUADR 18	Selects external bank for a CPU request.
CPUCHAR0	Input CHAR0 inhibited by a high CPUWRTPB input.
$\overline{\text{CPUEXSC-HLD}}$	Inhibits a new DMA external request.
$\overline{\text{CPUEXSCRQ}}$	CPU external split cycle request.
$\overline{\text{CPU/EXTSC}}$	Inhibits new DMA local request.
CPUEXTSEL	Enables CPU external control circuits.
$\overline{\text{CPUEXTSEL}}$	Resets CPU request latch. Not a complement of CPUEXTSEL.
$\overline{\text{CPUMABxx}}$	CPU memory address bits 01 through 11. Latched from CPU data lines S315/ through S305/.
$\overline{\text{CPUMAE}}$	CPU memory address error.
CPUPROT	CPU program protect line, enabled by inputs CPUPROTECT/, CPUINBNDS/, or $\overline{\text{ENPRTSYS}}$.
CPUREQ	CPU request latch set. Not a complement of input CPU-REQ/.
CPUREQ-L	CPU local request received.
CPU-SC	Complement of input CPU-SC/.
$\overline{\text{CPUSC-HLD}}$	Inhibits the RESYNDMA/EXT signal.
$\overline{\text{CPUSCREQ}}$	Initiates write portion of split cycle CPU request.
$\overline{\text{CPUWRT}}$	Input CPU WRITE inhibited by RDOPAGE/, $\overline{\text{CPUMAE}}$, or $\overline{\text{EMPF}}$.
$\overline{\text{CPUWRTHLD}}$	Delays the start of an unprotected CPU full write cycle.
DMAACT	DMA or higher priority request active.
$\overline{\text{DMAACT'}}$	Pulse just preceding start of DMA or higher priority cycle.
$\overline{\text{DMAEXSC-HLD}}$	Inhibits a new CPU external request.
$\overline{\text{DMAEXSCRQ}}$	DMA external split cycle request.

TABLE 4-15. ADDRESS AND CONTROL INTERFACE INTERNAL SIGNALS (Continued)

Signal	Description
$\overline{\text{DMA+EXTSC}}$	Inhibits new CPU local request.
DMAEXTSEL	Enables DMA external control circuits.
$\overline{\text{DMALREQ}}$	New DMA request received.
DMAPROT	Input DMAPROT/ inhibited by $\overline{\text{ENPRTSYS}}$.
DMAREQACT	Complement of output DMAREQACT/.
DMA-SC	Complement of input DMA-SC/.
$\overline{\text{DMASC-HLD}}$	Inhibits RESYNCDMA signal.
$\overline{\text{DMASCREQ}}$	Initiates write portion of split cycle DMA request.
DMAWRT	DMAWRITE inhibited by DMAMAE/.
DMAWRTPB	Complement of input DMAWRTPB/.
$\overline{\text{EMPF}}$	Complement of input EMPF.
$\overline{\text{ENCPUADR}}$	Enables CPU and refresh memory addresses.
$\overline{\text{ENDMAADR}}$	Enables DMA and external memory addresses, complement of $\overline{\text{ENCPUADR}}$.
$\overline{\text{ENEXTSTAT}}$	Enables external outputs CH0/PF andCH1/$\overline{\text{PE}}$.
$\overline{\text{ENMOS 250}}$	Complement of input ENMOS-250.
$\overline{\text{ENMOSRDD}}$	Enables output of transmit enable selector D8.
$\overline{\text{ENPRTSYS}}$	Complement of input ENPRTSYS.
$\overline{\text{ENRAS}}$	Enables outputs of row address strobe selectors.
EXTBANK	Complement of input EXTBANK/.
EXTREQACT	Complement of output EXTREQACT/.
EXTRESYNC	Resets the external request latches.
$\overline{\text{EXTRESYNDMA}}$	Brings RESYNCDMA high following a DMA external cycle.
$\overline{\text{FUL-WRT}}$	Unprotected word write (single cycle) control line.
$\overline{\text{MC/POMC}}$	Master clear/power-on master clear. Resets latches.
MEMHALT	Eight-phase clock stopped.
MEMRESYNC	Timing for DMA or higher priority start of cycle.

TABLE 4-15. ADDRESS AND CONTROL INTERFACE INTERNAL SIGNALS (Continued)

Signal	Description
MPE+DEDFF	Parity error or double error control line to abort a write operation.
$\overline{\text{MPE+DEDFF}}$	MPE+DEDFF inhibited by $\overline{\text{FUL-WRT}}$.
$\overline{\text{PO-MC}}$, $\overline{\text{PO-MC'}}$	Power on master clear control line.
PRIORITY	Complement of input PRIORITY/.
PROTFAULT	Derived from protect inputs and MPB-L line to form PF outputs.
$\overline{\text{RAE}}$	Row address enable; complement of $\overline{\text{CAE}}$.
$\overline{\text{REFMABxx}}$	Refresh memory addresses (01 through 06 and 15).
$\overline{\text{REFRESHREQ}}$	Memory cycle request from refresh timer.
RESYNCDMA, $\overline{\text{RESYNCDMA}}$	Reset DMA priority and local/external select latches.
$\overline{\text{RESYNCEXT}}$	Inhibits DMA external request.
$\overline{\text{RESYNCINT}}$	Inhibits DMA or higher priority select latch.
RESYNDMA/EXT	Resets DMA, external, and refresh priority latches.
$\overline{\text{SCCLRDMA}}$	Clears DMA or higher priority select latch during CPU split cycle.
SC-FF	Enables split cycle logic.
$\overline{\text{SELREFRESH}}$, $\overline{\text{SELREFRESH'}}$	Selects refresh memory addresses.
$\overline{\text{SETDMAMAE}}$	Sets DMA memory address error flip-flop.
$\overline{\text{STBCPUEXT}}$	Pulls output STBCPUDFM/ low following a CPU external cycle.
$\overline{\text{STBDMAEXT}}$	Pulls output STBDMADFM/ low following a DMA external cycle.
$\overline{\text{STCPUPEEXT}}$	Pulls output SET SM108/ low on CPU external parity error.
$\overline{\text{STCPUPFEXT}}$	Pulls output SET SM105/ low on CPU external protect fault.
$\overline{\text{STDMAPEEXT}}$	Pulls output DMAMPE/ low on DMA external parity error.
$\overline{\text{STDMAPFEXT}}$	Pulls output DMA-PF/ low on DMA external protect fault.
STRCONT	Clocks flip-flops producing EXTREQACT, DMAREQACT, and CPUACT outputs.
STRCPBPEXT	Pulls output STBCPUBKP/ low following a CPU external cycle.
STRMOSADR	Starts eight-phase clock and strobes memory addresses into address registers and decoders.
T2 ODDCLK	Complement of input T2 ODDCLK/.
$\overline{\text{WRITE}}$	Clears split cycle latches.
WRITE-SC	Enables automatic split cycle logic.
$\overline{\text{WRT-ABORT}}$	Inhibits WT-MOS/ output on protect fault or parity error.

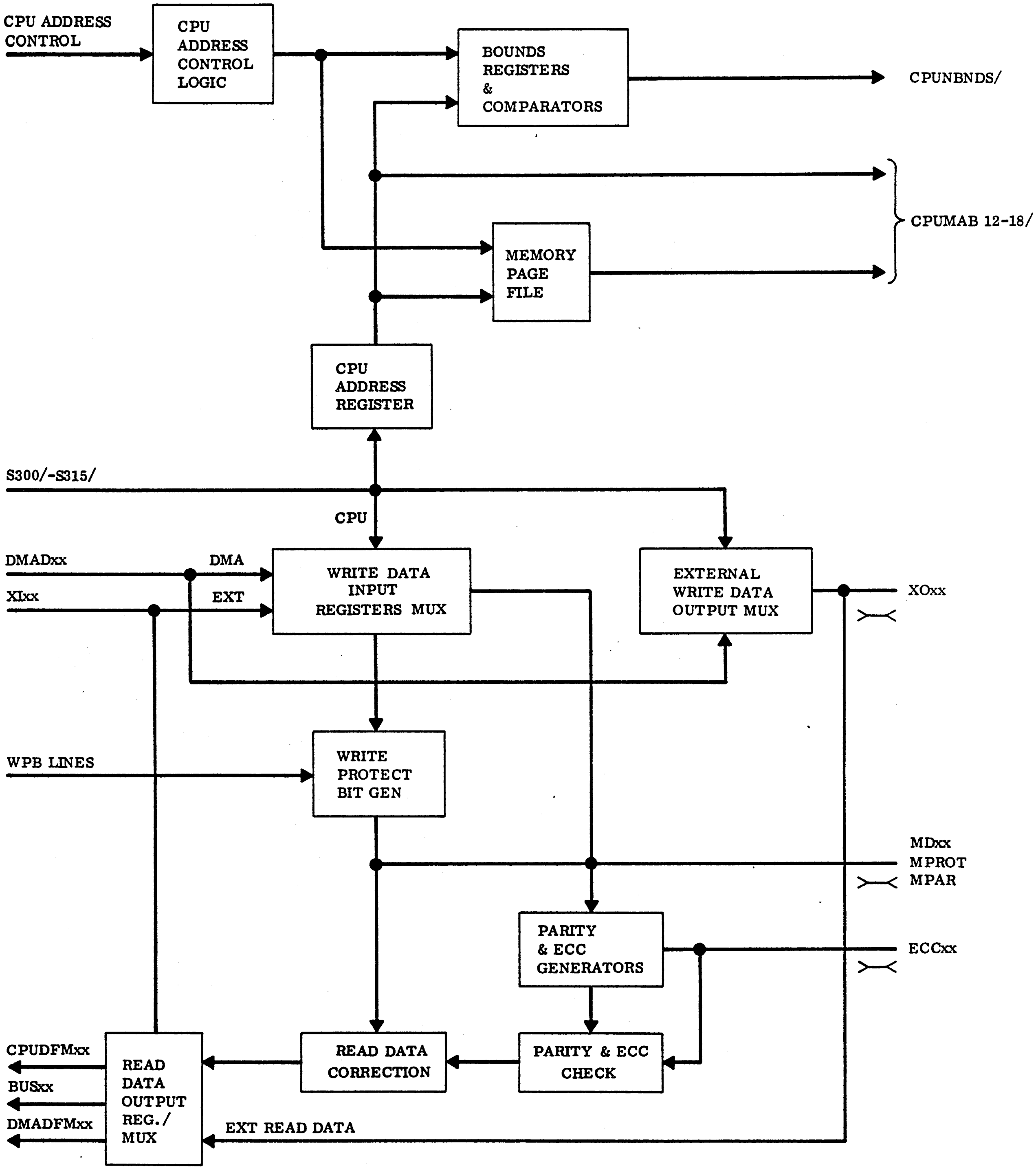


Figure 4-17. Data Interface Simplified Block Diagram

Incoming write data from the CPU or DMA devices is either directed to the external bank or stored for use in the local bank. Write data from the external bank is stored for local bank use. On command from the address and control interface priority circuits, the appropriate write data and protect bit is selected, the parity bit (and, with ECC, the five check bits) are generated, and the resulting 18-bit word is sent to the memory arrays.

On a read cycle or the read portion of a write cycle from the local bank, the data interface receives the 18-bit word from the memory arrays and the parity bit is checked. If the ECC option is installed, the check bits are also received, the five additional parity checks are made, and any single bit error in the data word is corrected. A parity error or ECC double-bit error is flagged and a signal sent to the address and control interface so that an error signal may be sent to the requesting device. The read data word (as corrected, with ECC) is directed to the three data output ports, and is also latched for use in a possible restore or character write operation.

The CPU and DMA data output registers, on command from the address and control interface, select either this local read data or read data from the external bank. The CPU output port also has provisions for providing breakpoint addresses, memory page file status, or ECC status over its two sets of output lines.

For the remainder of this section refer to the data interface block diagram in section 5.

CPU ADDRESS CONTROL

CPU address information is received by the data interface over the 16-bit multipurpose path S300/ through S315/. Operation on this data is controlled by the three address control lines from the CPU (GATEAB/, GATEUBDS/, GATELBDS/) and the condition of the four-bit micro instruction register (MIR28' through MIR31'), which is continually updated by clock pulse T0'/ from the CPU. Control is also affected by the status of the two-bit address memory register (AMR0, AMR1).

In general, the least significant 11 bits of the CPU address are used directly by the address and control interface over a parallel connection of lines S305/ through S315/. The most significant six bits of the 17-bit address, plus the bank select bit, are controlled by the data interface and sent to the address and control interface over the lines CPUMAB12/ through CPUMAB17/ plus CPUMAB18/ for the bank select bit.

The CPU address control section also includes a 16-bit CPU address register (AB register), 16-bit upper and lower bounds registers, two 16-bit comparators, a 64 by 9-bit random access memory (memory page file), and a seven-bit CPU address multiplexer.

The CPU address control commands are shown in table 4-16. Note that each of the commands loads the AB register with the data on S300/ through S315/, but this action is inhibited by a true BLKAB/ signal from the address and control interface, which occurs during a CPU read/modify/write split cycle.

AB Register

This 16-bit register is loaded with the contents of S300/ (MSB) through S315/ during any of the commands shown in table 4-16. The outputs of the register, AB00 (MSB) through AB15 are available to the CPU as a breakpoint address at the beginning of each CPU read or normal write cycle.

Bounds Registers and Comparators

Two 16-bit registers store the upper and lower bounds addresses of the unprotected memory area available to the CPU. The comparators continuously compare the AB00 through AB15 lines with the contents of the upper and lower bounds registers. When the AB00 through AB15 address is lower than the upper bounds address and higher than the lower bounds address, the line CPUNBNDS/ to the address and control interface goes low, which has the same effect as a true CPUPROTECT/ line during a CPU write operation.

TABLE 4-16. CPU ADDRESS CONTROL COMMANDS

Command	Condition	Effect
Load AB	GATEAB/ true	Loads S300/ through S315/ into AB register on leading edge. Clears load/read memory page file status and ECC status conditions.
Load Lower Bounds	GATELBDS/ true MIR28' false	Loads S300/ through S315/ into AB register on leading edge; then loads contents of AB register into lower bounds register on trailing edge.
Read ECC Status	GATELBDS/ true MIR28' true	Loads S300/ through S315/ into AB register and sets Enable ECC FF (to enable ECC status lines to CPU data output register). CPU read cycle necessary to place status levels on output lines.
Load Upper Bounds	GATEUBDS/ true MIR28' false MIR29' false	Loads S300/ through S315/ into AB register on leading edge; then loads contents of AB register into upper bounds register on trailing edge.
Load AMR	GATEUBDS/ true MIR29' true	Loads S300/ through S315/ into AB register and loads address memory register. AMR0 assumes level of MIR30', selecting page mode if true, absolute mode if false. AMR1 assumes level of MIR31', providing the most significant address bit to the memory page file on a page mode memory cycle.
Load/Read MPF	GATEUBDS/ true MIR28' true	Loads S300/ through S315/ into AB register and enables memory page file for loading or statusing. Selects memory page file status lines to CPU data output register, which are placed on the output lines on a subsequent CPU read or write cycle. A CPU write cycle loads the memory page file with a new page address, but does not affect the addressed location in memory.
Load/Read MPF/AMR	GATEUBDS/ true MIR28' true MIR29' true	Combination of load/read memory page file and load address memory register.

Memory Page File (MPF)

This 64-word by 9-bit random access memory contains a file of page addresses that form the most significant six bits of the CPU address when in page mode, plus the bank select bit. The outputs of the memory page file are (see figure 4-15):

MPF00 - MPF05:	Most significant six memory address bits
MPF06:	Bank select bit
MPF07:	Read only page protect bit
MPF08:	Unused

The five least significant memory page file address bits are provided by the lines AB00 through AB04 (LSB). The most significant bit is supplied by the AMR1 register for memory cycles, and by AB05 when the memory page file is enabled by a load/read memory page file command.

CPU Address Multiplexer

The CPU address multiplexer selects the seven most significant bits of the CPU address from either the AB register or the memory page file, depending upon the condition of AMR0. The outputs are sent to the address and control interface board.

	Source	
Output	AMR0 False (Absolute Mode)	AMR0 True (Page Mode)
CPUMAB12/ (LSB)	AB04	MPF00
—	—	—
CPUMAB16/	AB00	MPF04
CPUMAB17/	0	MPF05
CPUMAB18/ (bank select)	0	MPF06

PORT SIGNALS AND TIMING

CPU Port

Data on the multipurpose path S300/ through S315/ is considered an address when address control commands are being executed, but assumed to be write data when a CPU memory request (CPUREQ/) is received.

When a local bank CPU request is received by the address and control interface, the first activity of the data interface CPU port is a STBCPUDFM/ signal, which gates the ABxx lines from the AB register to the CPUDFMxx outputs to supply the breakpoint address to the CPU. After the request has been accepted, the STCP/EXD/ signal strobes write data from S300/ through S315/ into the CPU write data register. ENMOSWRTD/ low enables the CPU write data register to the MDxx lines to generate word parity. After ENMOSWRTD/ line goes high, read data appears on the MDxx lines, is corrected if an ECC option is installed, and is available to the CPU port. The second STBCPUDFM/ signal strobes this read data, the protect bit, and the write data word parity to the CPUDFMxx outputs. On a read cycle, a low ENMEMBUS/ line from the CPU enables these same outputs to the BUSxx lines. On a write cycle, the ENMOSWRTD/ line goes low again, and the latched write data is placed on the MDxx lines for writing into memory.

For a CPU external write cycle, write data is not latched but gated on the XOxx lines by the ENCPWRTDO/ signal to the external bank. Read data is received over the same XOxx lines and is strobed into the CPU data output register as in a local CPU cycle.

DMA Ports

After a DMA local bank request has been selected and accepted, data from the incoming lines DMAD01/ through DMAD16/ is strobed into the DMA write data register by the STCP/EXD/ signal. The low ENMOSWRTD/ and low DMAREQACT/ lines from the address and control interface place the latched DMA write data on the MDxx lines for the purpose of generating word parity After the ENMOSWRTD/ line goes high, read data appears on the MDxx lines. The data is corrected if an ECC option is installed and available to the DMA data output port. The signal STBDMADFM/ strobes this read data, the protect bit, and the write data word parity to the DMADFMxx outputs. On a write cycle, the ENMOSWRTD/ line again goes low, and the latched DMA write data is placed on the MDxx lines for writing into memory.

For a DMA external write cycle, write data is not latched but is gated to the XOxx lines by the ENDMWRTD/ signal to the external bank. Read data is received over the same XOxx lines, and strobed into the DMA data output register by the STBDMADFM/ signal as in a local DMA cycle.

External Port

After an external request has been accepted by the local bank, data from the incoming lines XI01 through XI16/ is strobed into the external write data register by the STCP/EXD/ signal. The low ENMOSWRTD/ and low EXTREQACT/ lines from the address and control interface place the latched write data on the MDxx lines for the purpose of generating word parity. After ENMOSWRTD/ goes high, read data appears on the MDxx lines, corrected if an ECC option is installed, and gated to the PRF/MPB line and write word parity is gated to the SC/MPL line by the same signal. On a write cycle, the ENMOSWRTD/ line again returns low and the latched external write data is placed on the MDxx lines for writing into memory.

PROTECT BIT GENERATION AND DETECTION

A protect bit is written into memory on each write cycle. The source of this protect bit is determined by the following truth table:

Write Protect Bit Line	EXTREQACT/	DMAREQACT/	Protect Bit Source
True	False	False	S306/(CPU)
True	False	True	DMAD10/
True	True	False	XI10
False	X	X	LSECMPB

Thus if the write protect bit line is true during a write cycle, the protect bit sent to bit 17 of the addressed memory word is the level of bit 10 of the selected write data line. If the write protect bit line is false, the protect bit previously in memory is restored. The protect bit line to the memory arrays is the bidirectional line MPROT. If only the protect bit is to be written, the requesting device must bring both character lines false, which restores the 16-bit data word during the write cycle.

If the ENPRTSYS line from the CPU is low, the protect bit is set true on every write cycle regardless of the condition of the protect bit write line or bit 10 of the incoming write data.

On a read cycle, or the read portion of a write cycle, the condition of the protect bit is received over the MPROT line from the memory arrays, corrected if necessary by the ECC circuits, and is made available to the requesting port over the lines MEMPROTBT/ to the CPU, DMAMPB/ to the DMA devices, and PRF/MPB to the external bank. The protect bit is also latched by the STBDFM/ signal, and is available as the LSECMPB line for restoration to memory and as the MPB-L line to the address and control interface for the detection of protect faults.

PARITY GENERATION AND DETECTION

As write data is strobed in on a write cycle, even parity is detected and the WORD PARITY line is latched true if an even number of 1s are present in the 16-bit write word. This latched level is available to the requesting port at the end of the read portion of a write cycle over the lines EVENPAR to the CPU, DMAMPL/ to the DMA devices, or SC/MPL to the external bank. This latched parity line has no other effect on operation.

Overall parity is generated during the read portion of a write cycle or during a read cycle from the 17-bit data word and protect bit read from memory and by the five ECC check bits if the option is installed. It is compared against the read parity bit on line MPAR from bit 16 of the addressed memory word. If the comparison is true (without ECC) then parity is correct and no error signal is sent. If the two parity signals are complementary, the MPE+DED line to the address and control interface flags a parity error. For ECC operation, see ECC Control below.

Parity is generated again from the write data word at the beginning of the write portion of a write cycle, this time including the protect bit (and the generated ECC bits). This parity level is placed on the MPAR line for writing into bit 16 of the addressed memory location.

ECC CONTROL

ECC theory is fully described under Error Detection and Correction. The ECC elements on the data interface board include the check bit generators, syndrome bit logic and bit position decoders, the error correction circuit, and the error alarm logic.

Briefly, the check bits are generated during a write cycle from five parity generators in the data interface. They are sent to the ECC array; the parity bit, and protect bit are sent to the memory arrays.

On a read cycle or the read portion of a write cycle, the five check bits are regenerated from the stored data word and protect bit. They are compared against the five check bits read from the ECC array, and any differences appear as syndrome bits SB00 through SB04. These syndrome bits are decoded to a single line output of a 5-bit to 24-line decoder, and this line is used to complement the erroneous bit in the error correction circuit. The corrected read data appears on the lines SEC00 through SEC15 and SECMPB, and is latched by the STBDFM/ signal as LSEC00 through LSEC15 plus LSECMPB to be available for a restore operation.

Three status conditions exist after a read operation with ECC:

- No error — The syndrome bits are all zero and the parity check is correct. No error signal is generated.
- Single bit error — (a) one or more of the syndrome bits is nonzero and the parity is bad. (b) The syndrome bits are zero and the parity is bad. The error is corrected and the SEC STATUS/ line is latched true. A GATE ECC STATUS command must be issued by the CPU to clear this status latch.
- Double error — One of more of the syndrome bits is nonzero but the parity checks OK. The MPE+DED/ line to the address and control interface is set true for the generation of an error signal to the CPU, DMA, or external port. Abortion

of a write operation by an unprotected port, or abortion of a write protect bit operation will result.

CHARACTER WRITE OR RESTORE CONTROL

Character write or restore operation is controlled by the CHR-0/ and CHR-1/ lines from the address and control interface, which are derived from the character 0 and 1 lines from the requesting device.

The write data multiplexer is split into two independently controlled segments, such that the most significant and least significant eight bits may be selected from one of the three write data in registers (write) or from the latched corrected read data (restore).

On a word write operation both character lines are true and both halves of the write word are derived from the data in the register selected by the lines EXTREQACT/ and DMAREQACT/ (the CPU is assumed if both are false).

On a character write operation, one of the character lines is true and the other false. If CHR-0/ is false (high), the least significant eight memory data bits are derived from the least significant eight bits of the incoming write data, while the most significant eight bits are from the corrected latched read data LSEC08 through LSEC15. If CHR-1/ is false, the least significant eight bits are from the corrected latched read data LSEC00 through LSEC07, while the most significant eight memory data bits are sourced from the most significant eight bits of the selected incoming write data. If both character lines are false, the memory data word consists entirely of the latched corrected read data.

The protect bit is unaffected by a character write or restore operation, and may be restored or changed under control of the protect bit write line. The parity bit is regenerated on each word write or character write operation.

DATA INTERFACE INTERNAL SIGNALS

Referenced signals contained entirely within the data interface board are described in table 4-17.

MEMORY ARRAYS

The MOS memory array cards contain the physical memory circuits (MOS memory chips) and the buffering for data, address and control signals to and from the interface circuits. The cards are available with 16K word by 18-bit (AT275) or 32K word by 18-bit (AT241) storage capacity with a 280-nanosecond access time.

Array cards are physically placed in slots X, Y, Z and AC of the mainframe to configure a macro memory for the system. Placement of the cards and address connectors is discussed below.

Circuit descriptions, a functional block diagram, logic diagrams, and backplane wiring notes are contained in section five.

MEMORY CONFIGURATION

Total macro memory using MOS memory arrays is 131,072 words of 18 bits each, expandable to 262,144 words by the use of an external bank. Many configurations are possible within a memory bank, and these are easily changed by the substitution or addition of array cards and the positioning of the address connectors on the backplane.

To configure memory, arrays are chosen to meet the desired total storage capacity. The arrays are placed in slots X, Y, Z and AC in the mainframe beginning with slot X.

TABLE 4-17. DATA INTERFACE INTERNAL SIGNALS

Signal	Description
ABxx	CPU address bits 00 through 15. Latched from lines S300/ through S315/.
$\overline{\text{ABxx}}$	Complements of AB07 through AB15; used to load page addresses.
$\overline{\text{BPxx}}$	Bit positions 03 through 22; decoded from the ECC syndrome bits SB00 through SB04.
CPDFMxx	Outputs 01 through 16 from CPU data output multiplexer.
$\overline{\text{CPUxx}}$	Latched CPU write data bits 00 through 15 from lines S300/ through S315/.
$\overline{\text{DMALOCAL}}$	Same as input DMAREQACT/.
ECCH	Complement of input status line ECCHERE/.
$\overline{\text{ECPUL}}$	Enables lower half of CPU write data to memory array.
$\overline{\text{ECPUU}}$	Enables upper half of CPU write data to memory array.
$\overline{\text{EDMAL}}$	Enables lower half of DMA write data to memory array.
$\overline{\text{EDMAU}}$	Enables upper half of DMA write data to memory array.
EECC	Complement of $\overline{\text{ENABLE LOCAL ECC STATUS}}$; trailing edge clears SEC status latch.
$\overline{\text{EMPF}}$	Complement of output EMPF (Enable Memory Page File).
$\overline{\text{ENABLE ECC}}$	Enables ECC check bit outputs to memory array.
$\overline{\text{ENABLE LOCAL ECC STATUS}}$	Selects ECC status inputs to CPU data output multiplexer.
$\overline{\text{ENABLE LOCAL MPF STATUS}}$	Selects MPF status inputs to CPU operand data outputs. Complement of output EMPF.
$\overline{\text{EPROT/PAR}}$	Enables protect and parity bit outputs to array. Same as input ENMOSWRTD/.
$\overline{\text{ESECL}}$	Enables lower half of read data to memory array (restore).
$\overline{\text{ESECU}}$	Enables upper half of read data to memory array (restore).
$\overline{\text{EXL}}$	Enables lower half of external write data to memory array.
$\overline{\text{EXU}}$	Enables upper half of external write data to memory array.
K0 - K4	Outputs from ECC check bit generators.
$\overline{\text{LDMAxx}}$	Latched DMA write data bits 01 through 16.
LOAD AB	Loads contents of S300/ through S315/ into CPU address register.
$\overline{\text{LOAD LBDS}}$	Trailing edge loads contents of CPU address register into lower bounds register.

TABLE 4-17. DATA INTERFACE INTERNAL SIGNALS (Continued)

Signal	Description
$\overline{\text{LOAD UBDS}}$	Trailing edge loads contents of CPU address register into upper bounds register.
LOAD WRITE DATA	Complement of input STCP/EXD/.
LSEC	Latched value of the SEC line, indicating a single bit error.
LSECxx	Latched corrected read data from memory, bits 00 through 15.
LSECMPB	Latched value of last protect bit read. Same as output MPB-L.
MPFxx	Outputs 00 through 08 from the memory page file.
MR	Same as input MC/.
$\overline{\text{MULTIND}}$	Complement of input MULTIND.
PBMUX A PBMUXB	Protect bit multiplexer select lines.
PGM FILES	Complement of output PGM FILES/. Selects upper half of memory page file.
READ ONLY PAGE ERROR	Complement of output ROPINT/.
REF+CPU	Status line active during refresh or CPU memory cycles.
SBxx	Syndrome bits 00 through 04.
SEC	Single error correction flag.
SECxx	Corrected read data bits 00 through 15.
SECMPB	Corrected read memory protect bit.
WORD PARITY	Output of parity generator.
$\overline{\text{WRITE MPF}}$	Sets memory page file to write mode.
WT-MPL	Local bank parity line; latched value of WORD PARITY.
XMPB	Protect bit from external bank.
XMPL	Parity bit from external bank.
XRDxx	Latched read data bits 01 (LSB) through 16 from external bank.
XWDxx	Latched write data bits 01 (LSB) through 16 from external bank.

Possible configurations are shown in table 4-18, along with the appropriate positions of the back plane address connector (part 96762000). The configurations adhere to these mandatory rules, necessary for proper system operation:

1. A 16K or 32K array may not be in a slot following a blank slot.

	X	Y	Z	AC
Incorrect:	16K	—	16K	—
Correct:	16K	16K	—	—

2. A 32K array may not be in a slot following a 16K array.

	X	Y	Z	AC
Incorrect:	16K	16K	32K	—
Correct:	32K	16K	16K	—

3. If an ECC array is used it must be in slot AC. An ECC array is always permitted in slot AC unless a memory data array already occupies that slot. For this reason the maximum memory capacity in a bank with ECC is 98,304 words.

Once memory is configured, array boards of the same capacity may be interchanged for troubleshooting purposes. Although physically the same size, 16K and 32K boards may not be interchanged without a reconfiguration involving the relocation of the backplane address connectors.

MEMORY ORGANIZATION AND ADDRESSING

The basic element of the MOS memory system is the 4K block, consisting of 18 MOS 4096-bit dynamic random access memory chips, organized as 4096 words by 18 bits. Control and addressing inputs are paralleled to the 18 chips within the block, while each chip receives and provides a single data chip of the 18-bit data word.

Addressing a word within the 4K block requires a 12-bit address, and in this MOS memory the address is loaded in two stages over the six address lines MOSMA00 through MOSMA05. The first stage occurs when the RAS signal (row address strobe) is received by the selected 4K block. This signal strobes the six address bits on the MOSMAxx lines into on-chip row address

TABLE 4-18. MEMORY CONFIGURATION

Memory Bank Capacity (Words)	MP Slot				Address Connector Location (Top pins — slots Y, Z, AC)
	X	Y	Z	AC	
16,384	16K	—	—	*	None required
32,768	16K	16K	—	*	10,210
32,768	32K	—	—	*	None required
49,152	16K	16K	16K	*	10,210
49,152	32K	16K	—	*	9,209
65,536	16K	16K	16K	16K	10,210
65,536	32K	16K	16K	*	9,209
65,536	32K	32K	—	*	7,207
81,920	32K	16K	16K	16K	9,209
81,920	32K	32K	16K	*	8,208
98,304	32K	32K	16K	16K	8,208
98,304	32K	32K	32K	*	7,207
114,688	32K	32K	32K	16K	7,207
131,072	32K	32K	32K	32K	7,207

*ECC always permitted in slot AC unless 16K or 32K array occupies that slot. No address connector is required at AC for an ECC array.

registers. The second six bits are then placed on the MOSMAxx lines and strobed into the column address registers in memory chips by the CAS signal (column address strobe). The terms row and column refer to the 64 by 64-bit arrangement of storage cells within each 4096-bit chip.

A 16K memory section contains four 4K blocks. A section may constitute either a complete 16K memory array card or half of a 32K card. To select a 4K block within a section, one of the four lines SLTBLK0/ through SLTBLK3/ is brought low by the address and control interface. This signal gates the incoming row address strobe RAS16Kx-x/ to provide the appropriate RAS signal to the selected block. Refer to figure 4-18.

Selection of a 16K section is made by one of the eight row address strobes from the address and control interface, RAS16K0-1/ through RAS16K1-4/. At slot X of the MP17 mainframe, the RAS16K0-1/ line is available to the array card. When low this line selects the first 16K memory section, which will be either a 16K memory located in slot X or the lower half of a 32K memory in that same location. If a 32K memory array card is located in slot X, the next sequential row address strobe select line RAS16K1-1 is picked up on the board, selecting the upper half (16K section) of the 32K card.

At slot Y, the row address strobe select line for the first 16K section of its associated board must be derived from the RAS16K1-1/ line if a 16K memory is in slot X, or the RAS16K0-2/ line if a 32K memory is in slot X. It is at this point that the address connector on slot Y must be located according to the configuration requirements shown in table 4-18. A similar condition exists for slots Z and AC. For details, refer to the backplane notes in section 5.

Read data from the memory arrays is selected in the same manner by the E16KNx-x/ lines from the address and control interface. On a read cycle, or read portion of a write cycle, one of these lines is low, enabling the read data buffers of a single 16K section to the bidirectional memory data lines MD00 through MD15, MPAR and MPROT.

MEMORY SIGNALS AND TIMING

Timing for the memory arrays is supplied by the address and control interface timing circuits, which are designed to closely match the capabilities of the MOS memory chips. The access times of 280 nanoseconds for a fast array and 330 nanoseconds for a slow array are memory system times measured from the time the row address strobe signal is generated by the address and control interface until read data is strobed into the data interface read data output register (T6 time of the eight-phase timing chain).

Activity begins at the memory array with the receipt of address and block select information on the lines MOSMAxx and SLTBLKx/, following acceptance of a memory request by the interface. The cycle begins when the selected RAS16Kx-x/ signal arrives, and is routed to the appropriate 16K memory section through the backplane wiring and address connector. There it is gated by the one low SLTBLKx/ line to form a row address strobe (RAS) to a specific 4K block, strobing the row address on the MOSMAxx lines into the on-chip registers. The chip select line (CS) to the 4K block is also brought low at this time except on refresh operations. After the row address is stored on the chip, the MOSMAxx lines contain column address information from the address and control interface and the column address strobe (CAS/) signal is received (approximately 90 nanoseconds after the row address strobe for a fast array, 150 nanoseconds for a slow array), strobing column address information into the selected chip.

At this time, on a read cycle or the read portion of a write cycle, the associated E16KNx-x/ line is brought low, which enables read data outputs from the selected block to the MDxx, MPAR and MPROT lines. However, valid data will not be present until each chip has reached its access time. At T6 time of the eight-phase timing chain, when all chips in the section should have reached access time, data will be strobed from the MDxx line to a read data register. At T7 time, the enabling E16KNx-x/ signal is removed.

On a write cycle, the write line WT-MOS/ is brought low at T2 or T2* time depending upon the type of cycle, strobing write data from the MDxx, MPAR and MPROT lines into the memory chips of the selected 4K block. The write line and row address strobe are held low for the time required by the chips (until T5 or T5* time) to achieve storage.

Approximately every 15.6 microseconds a refresh operation takes place which ensures stored data remains intact. Alternately all of the RAS16K0-x/ lines or all of the RAS16K1-x/ lines are enabled, along with all of the SLTBLKx/ lines. Thus on alternate cycles half the

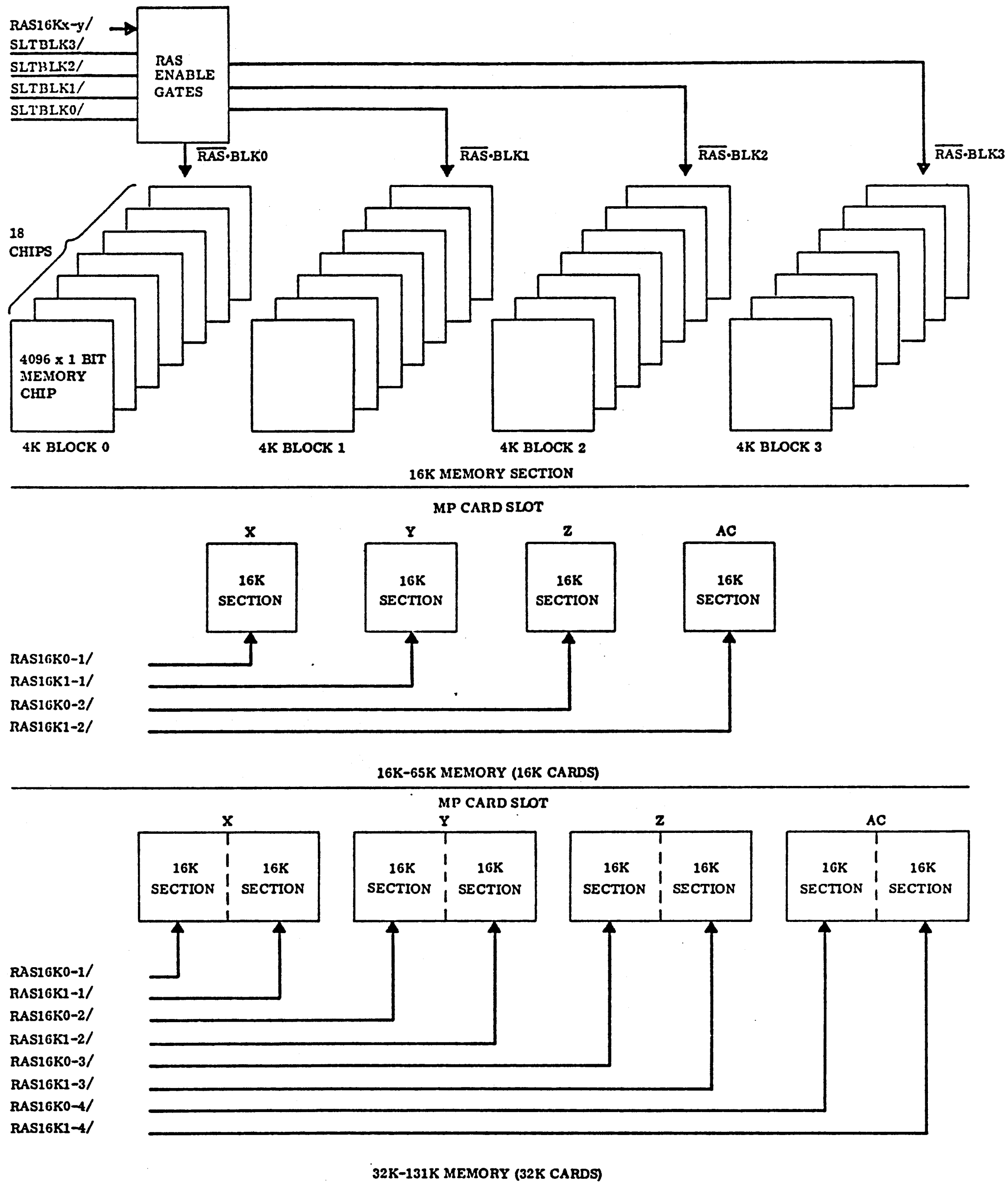


Figure 4-18. MOS Memory Organization

4K blocks are enabled. A single row address is given, however no column address is necessary as the chips are refreshed a row at a time. Sixty-four cycles are thus necessary on each set of row address strobes for a complete refresh, which will occur each two milliseconds. A refresh cycle is the same as a read cycle except that the chip select line CS/ remains high.

ERROR CHECKING AND CORRECTION (ECC)

Memory integrity may be ensured through the use of an error checking and correction option to the MOS memory. The ECC option detects and corrects single-bit errors and flags any two-bit error in a data word. If ECC is not used, only single-bit errors are flagged by a parity error, and two-bit errors will be undetected.

The option consists physically of a 98K word by five-bit ECC array board which occupies slot AC in the MP17 mainframe. Total bank memory capacity is therefore limited to 98K words. Logic for ECC operation is contained on the data interface board, and details of ECC logic will be found in the data interface sections of this manual.

ECC THEORY

ECC is a method of adding parity bits generated from portions of a binary word until a code is produced in which a single bit error can be located, not just flagged. To be single error correcting, a code must be such that at least three changes in the bit configuration are made when changing from one binary number to any other binary number. The conventional Hamming code produces this result. The data field consists of 17 bits, MD00 to MD15 (MD00 = LSB) and a word protect bit (MPROT). Five bits (ECC00 through ECC04) are added. The error correcting code bits are called the check field and extend the bit locations to 22 positions. The parity bit discussed later in this section increases the total bit locations to 23.

When the 17 bit data word is presented to memory, the ECC bits are generated to produce an even parity with the particular data bits that acted upon each. ECC00 is a result of bit positions 3, 5, 7, 9, 11, 15, 17, 19, and 21. ECC01 is a result of bit positions 3, 6, 7, 10, 11, 14, 15, 18, 19, and 22. ECC02 is a result of bit positions 5, 6, 7, 12, 13, 14, 15, 20, 21, and 22. ECC03 is a result of bit positions 9 through 15. ECC04 is a result of bit positions 17 through 22. Refer to figure 4-19.

When a data word is read from memory, the five ECC bits are regenerated and compared to the stored five. The resulting five bits from the exclusive-OR comparison are called syndrome bits. If the two ECC bit sets are equal, the syndrome bits are zero. If the overall parity check is also correct then no parity error occurred; if the overall parity check is incorrect, a single-bit error occurred in the parity bit position. If they are not equal, an error has occurred. If the overall parity check is incorrect, a single-bit error occurred and the binary value syndrome bits specify the bit position in error. If the overall parity check is correct a two-bit error occurred and the syndrome bits are meaningless. Table 4-19 shows the fault code and its meaning.

To perform a single error correction the syndrome bits are decoded to identify the incorrect bit and the bad bit is complemented.

As an example (figure 4-19), assume the data word is $2A7A_{16}$: binary 0 0010 1010 0111 1010. Generating an even parity for each ECC bit using its associated input data bit produces 00110. The composite word is also shown with odd parity generated for bit locations 1 through 22. When the data word is read from memory during a read cycle and if there is an error in bit location 9, the incorrect word becomes 0 0010 1010 0110 1010 ($2A6A_{16}$). The regenerated ECC bits become 01111. Upon comparing the two sets of ECC bits, the syndrome bits become 01001, indicating an error in bit location 9, memory data line MD04.

ECC and Parity Application

Activity begins when data is placed on the 17 memory data lines MD00 to MD15 and MPROT. WORD PARITY, generated on MD00 to MD15, goes high if the 16 input bits are even.

If the ECC option is not present, ECCHERE/ is high and K0 through K4 are forced low. During write data enable EPROT/PAR, the full odd parity (MPAR) is generated using WORD PARITY and MPROT. During read data enable, parity is checked by sampling the MPE+DED/ line. A low indicates a memory parity error.

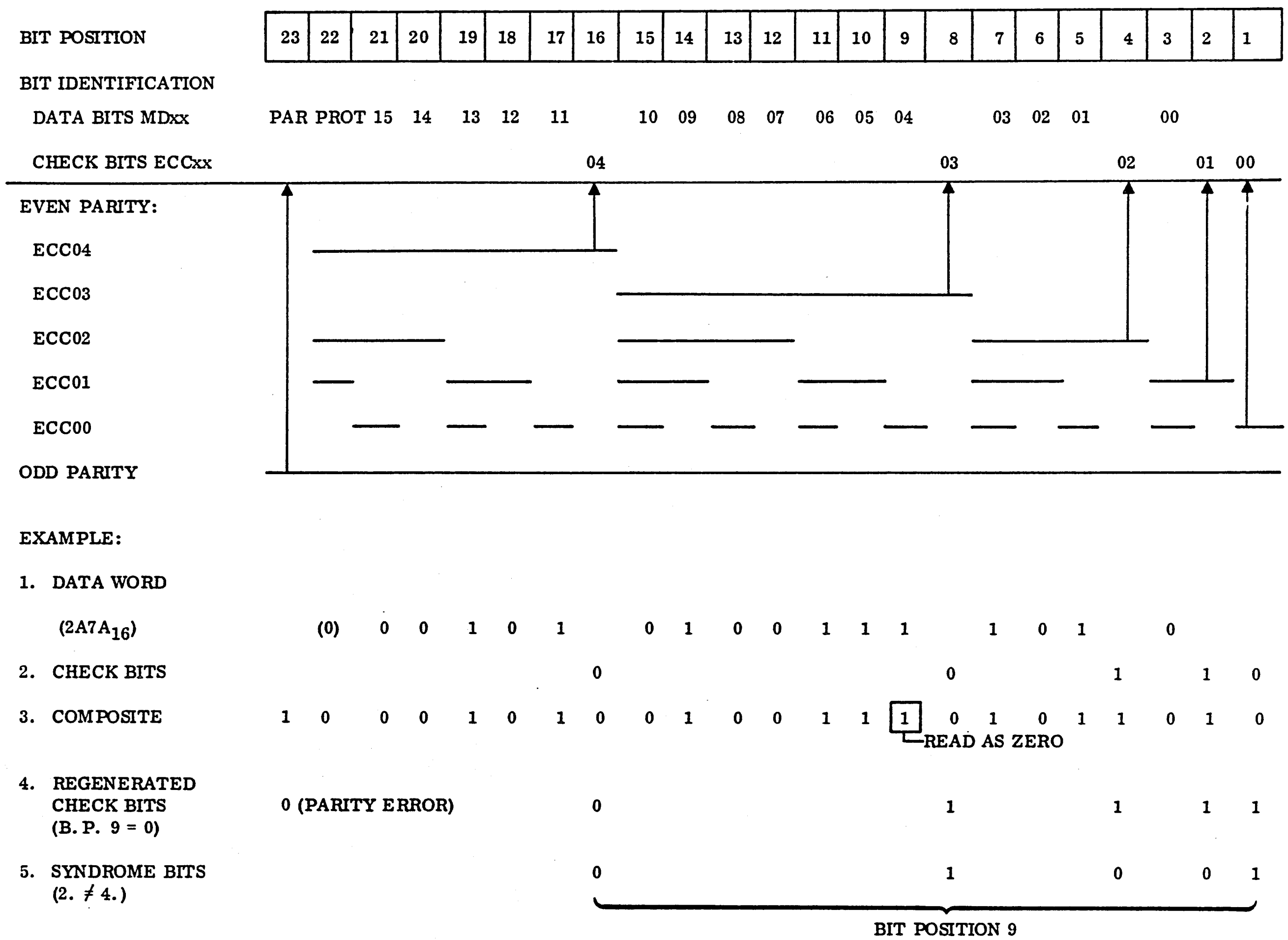


Figure 4-19. Error Correction Code

TABLE 4-19. SYNDROME CODE LISTING

Syndrome Bits (SBxx)					Fault
04	03	02	01	00	
0	0	0	0	0	No error (parity OK) or parity bit error
0	0	0	0	1	Error in bit position 1: ECC00
0	0	0	1	0	Error in bit position 2: ECC01
0	0	0	1	1	Error in bit position 3: MD00
0	0	1	0	0	Error in bit position 4: ECC02
0	0	1	0	1	Error in bit position 5: MD01
0	0	1	1	0	Error in bit position 6: MD02
0	0	1	1	1	Error in bit position 7: MD03
0	1	0	0	0	Error in bit position 8: ECC03
0	1	0	0	1	Error in bit position 9: MD04
0	1	0	1	0	Error in bit position 10: MD05
0	1	0	1	1	Error in bit position 11: MD06
0	1	1	0	0	Error in bit position 12: MD07
0	1	1	0	1	Error in bit position 13: MD08
0	1	1	1	0	Error in bit position 14: MD09
0	1	1	1	1	Error in bit position 15: MD10
1	0	0	0	0	Error in bit position 16: ECC04
1	0	0	0	1	Error in bit position 17: MD11
1	0	0	1	0	Error in bit position 18: MD12
1	0	0	1	1	Error in bit position 19: MD13
1	0	1	0	0	Error in bit position 20: MD14
1	0	1	0	1	Error in bit position 21: MD15
1	0	1	1	0	Error in bit position 22: MPROT
1	0	1	1	1	Multiple bit errors
1	1	x	x	x	Multiple bit errors

If the ECC option is present, ECCHERE/ is low and the generation of K0 through K4 occurs as described under ECC Method. During write data enable, the full odd parity (MPAR) is generated using WORD PARITY, MPROT, and K0 through K4. In addition, K0 through K4, now labeled ECC00 through ECC04 since passing through control logic are stored in the ECC MOS array board.

During read data enable, the word called from memory is placed on the memory data lines and K0 through K4 are generated for this recalled word. At the same time, the data word in question is called from memory and the original error correcting code bits ECC00 through ECC04 are called from the ECC memory array board and placed on lines ECC00 through ECC04. They are compared and produce syndrome bits SB00 through SB04, which remain low if no bit error is recognized. Should any of these bits go high, the bits in error are decoded to determine bit position, ranging from BP03 through BP22. MD00 through MD15 and MPROT (the data information bits) are then passed through exclusive-OR gates for complementing if single bit errors are detected. The single-error-corrected outputs are SEC00 through SEC15 and SECMPB. The SEC bits are finally latched by the STBDFM/ signal, become LSEC00 through LSEC15 and LSECMPB, and await control logic to pick their destination. During this time parity is also checked. If ECC is correct and parity is correct, everything is correct and nothing is corrected. If parity is in error, a single bit error has occurred and it is corrected if the syndrome bits are nonzero (ECC bit errors need not be corrected). If ECC is incorrect and parity is good, a double bit error is detected and flagged as nonrecoverable by MPE+DED/ low.

ECC MEMORY ARRAY

The ECC MOS memory array board is a special-purpose memory board designed to store the error correcting code bits ECC00 through ECC04. The board's location is slot AC. It has a five-bit bidirectional bus and has the same timing and control found on the memory data board. Signals EN16KN0-1/, EN16KN1-1/, EN16KN0-1/, EN16KN1-2/, EN16KN0-3/, and EN16KN1-3/ are enable read data lines and select which bank of 16K memory is to be used. SLTBLK0/, SLTBLK1/, SLTBLK2/, and SLTBLK3/ are select block signals and select a 4K section of memory to be used with the 16K of memory previously selected. RAS16K0-1/, RAS16K1-1/, RAS16K0-2/, RAS16K1-2/, RAS16K0-3/, and RAS16K1-3/ are the row address strobes for the memory chips. MA00 through MA05 are the shared row and column address bits for the memory address chips.

This section contains block diagrams, circuit descriptions, and logic diagrams. The block diagrams are related to the theory of operation in section 4. The circuit descriptions are related to the block diagrams in this section and to the logic diagrams at the end of this section.

INTERCONNECTING DIAGRAM

Figures 5-1 thru 5-4 show all connections between data interface, address and control interface, memory arrays, ECC array, and other system components. All data and address paths are highlighted. Signal names and logic board pin-numbers are included. The diagrams should be useful for troubleshooting to the board level.

FUNCTIONAL BLOCK DIAGRAMS

Figures 5-5 thru 5-8 show data flow, address paths and major control signals in the array and interface boards. All data and address paths are highlighted. Each block of the diagrams contains a number in the upper right corner that corresponds to the logic diagram sheet number. These block diagrams supplement the logic diagrams and are also intended to be used for training maintenance personnel.

ADDRESS AND CONTROL INTERFACE BOARD CIRCUITS

DMA PRIORITY AND BANK SELECT CIRCUITS

The highest priority DMA request is determined by this circuit, and a DMA local or DMA external request is produced.

The four incoming DMA request lines, DMA1-MR/ through DMA4-MR/, are input through selector B1 to the four DMA request latches at B2 and B3. However, only the one input selected by switch S10 (at location BC1) is available through the selector to the latches when the PRIORITY/ input line is low. Later DMA requests are locked out as soon as the first latch is set.

Resync timing for the DMA priority select circuit is provided by the flip-flops at L1 and L2, plus the delay circuit J1.

After a 40-nanosecond delay, to assure that the local/ external bank select line DMAx-INT has stabilized, the highest priority request is selected through the gates at D1, D2, and C2 and the resulting request accept signal (DMAx-RA/ low) is sent to the DMA port. This request accept signal informs the selected DMA device to place its data and control signals on the data, address and control lines which are common to all DMA devices. As the DMAx-RA/ line goes low, the associated flip-flop at F1 or G1 corresponding to the selected DMA device will be clocked low only if the incoming line DMAx-INT is high, indicating an internal bank request.

After an additional 30-nanosecond resync delay, the gates at D1 and A2 generate either a DMA local or DMA external request that is sent to the appropriate local or external priority select circuit. If an external bank is not connected (EXTBANK/ high) a local bank request is generated even if the external bank was requested, but the DMA memory address error flag is set via line $\overline{\text{SETDMAMAE}}$. A local DMA request can also be generated by the line $\overline{\text{DMASCREQ}}$, which starts the write portion of a DMA read/modify/write cycle.

The internal/external request gates are disabled after the DMA request has been selected by either the local or external bank priority select circuits, and the incoming DMA request latches are reset after the completion of the requested DMA memory cycle by the lines RESYNCDMA and $\overline{\text{RESYNCDMA}}$.

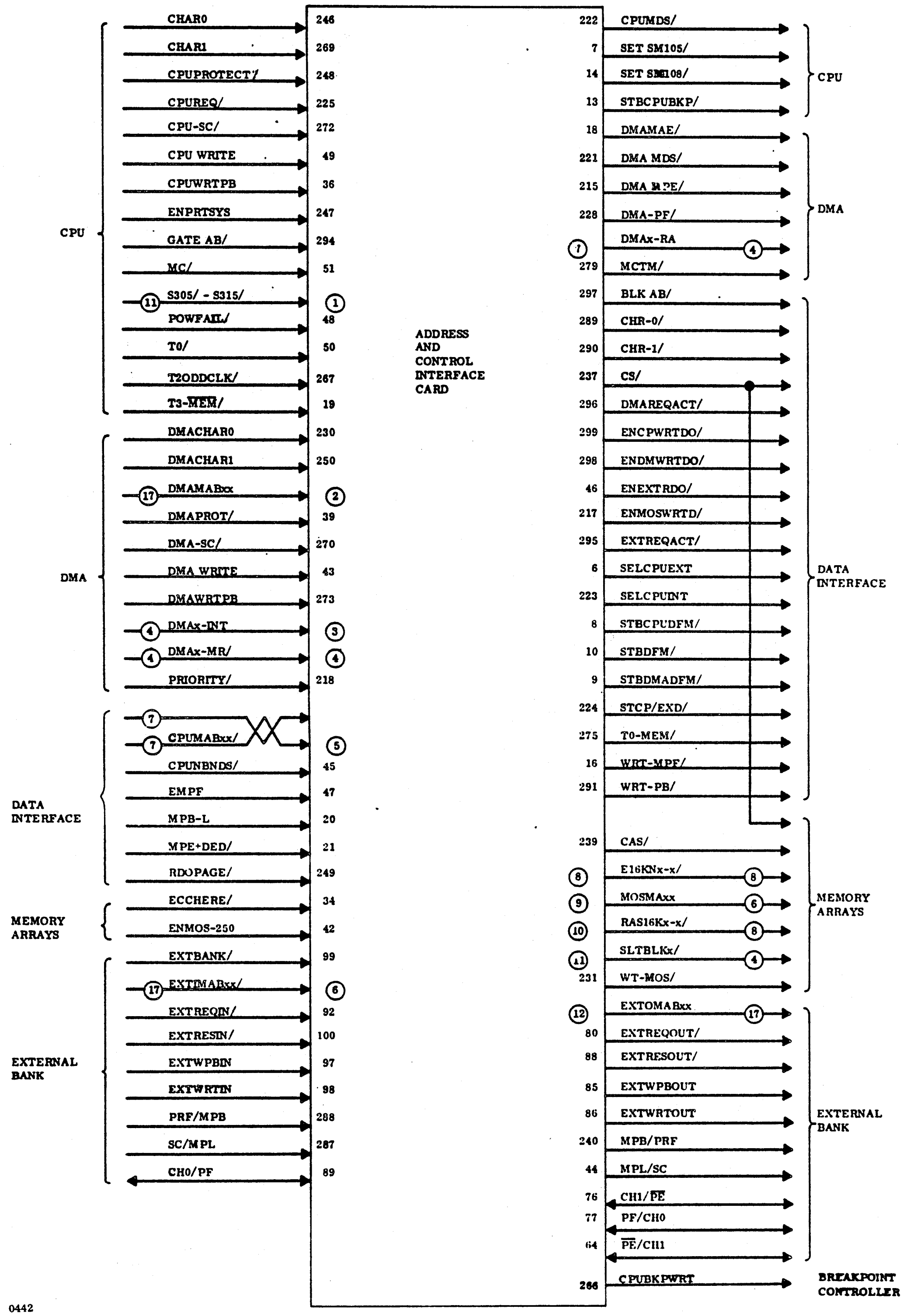


Figure 5-1. Address and Control Interface Signals (Sheet 1 of 2)

(1)

S305/ - S315/	
S305/	41
S306/	40
S307/	38
S308/	23
S309/	28
S310/	24
S311/	22
S312/	29
S313/	12
S314/	15
S315/	5

(2)

DMAMABxx	
DMAMAB01	37
DMAMAB02	253
DMAMAB03	255
DMAMAB04	256
DMAMAB05	263
DMAMAB06	35
DMAMAB07	277
DMAMAB08	52
DMAMAB09	252
DMAMAB10	261
DMAMAB11	262
DMAMAB12	274
DMAMAB13	292
DMAMAB14	281
DMAMAB15	282
DMAMAB16	271
DMAMAB17	284

(3)

DMAx-INT	
DMA1-INT	210
DMA2-INT	205
DMA3-INT	248
DMA4-INT	211

(4)

DMAx-MR/	
DMA1-MR/	11
DMA2-MR/	214
DMA3-MR/	212
DMA4-MR/	213

(5)

CPUMABxx/	SIG SLW	GND STRIP WX†
CPUMAB12/	268	68
CPUMAB13/	286	86
CPUMAB14/	280	80
CPUMAB15/	293	93
CPUMAB16/	285	85
CPUMAB17/	283	83
CPUMAB18/	17	17

(6)

EXTIMABxx	
EXTIMAB01	65
EXTIMAB02	66
EXTIMAB03	67
EXTIMAB04	68
EXTIMAB05	69
EXTIMAB06	70
EXTIMAB07	71
EXTIMAB08	72
EXTIMAB09	73
EXTIMAB10	74
EXTIMAB11	75
EXTIMAB12	90
EXTIMAB13	91
EXTIMAB14	93
EXTIMAB15	94
EXTIMAB16	95
EXTIMAB17	96

(7)

DMAx-RA/	
DMA1-RA/	227
DMA2-RA/	219
DMA3-RA/	220
DMA4-RA/	216

(8)

E16KNx-x /	
E16KN0-1/	208
E16KN1-1/	226
E16KN0-2/	207
E16KN1-2/	26
E16KN0-3/	206
E16KN1-3/	25
E16KN0-4/	209
E16KN1-4/	27

(9)

MOSMAxx	
MOSMA00	258
MOSMA01	257
MOSMA02	260
MOSMA03	259
MOSMA04	265
MOSMA05	264

(10)

RAS16Kx-x/	
RAS16K0-1/	236
RAS16K1-1/	244
RAS16K0-2/	32
RAS16K1-2/	30
RAS16K0-3/	33
RAS16K1-3/	233
RAS16K0-4/	232
RAS16K1-4/	31

(11)

SLTBLKx /	
SLTBLK0/	238
SLTBLK1/	235
SLTBLK2/	241
SLTBLK3/	242

(2)

EXTOMABxx/	
EXTOMAB01/	53
EXTOMAB02/	54
EXTOMAB03/	55
EXTOMAB04/	56
EXTOMAB05/	57
EXTOMAB06/	58
EXTOMAB07/	59
EXTOMAB08/	60
EXTOMAB09/	61
EXTOMAB10/	62
EXTOMAB11/	63
EXTOMAB12/	78
EXTOMAB13/	79
EXTOMAB14/	81
EXTOMAB15/	82
EXTOMAB16/	83
EXTOMAB17/	84

† TWISTED PAIR, BLUE WIRE TO GROUND. POSITION WX REFERS TO GROUND STRIP LOCATED BETWEEN SLOTS W AND X. PIN DESIGNATION NUMBERS ARE 4-50 AND 53-102.

Figure 5-1. Address and Control Interface Signals (Sheet 2 of 2)

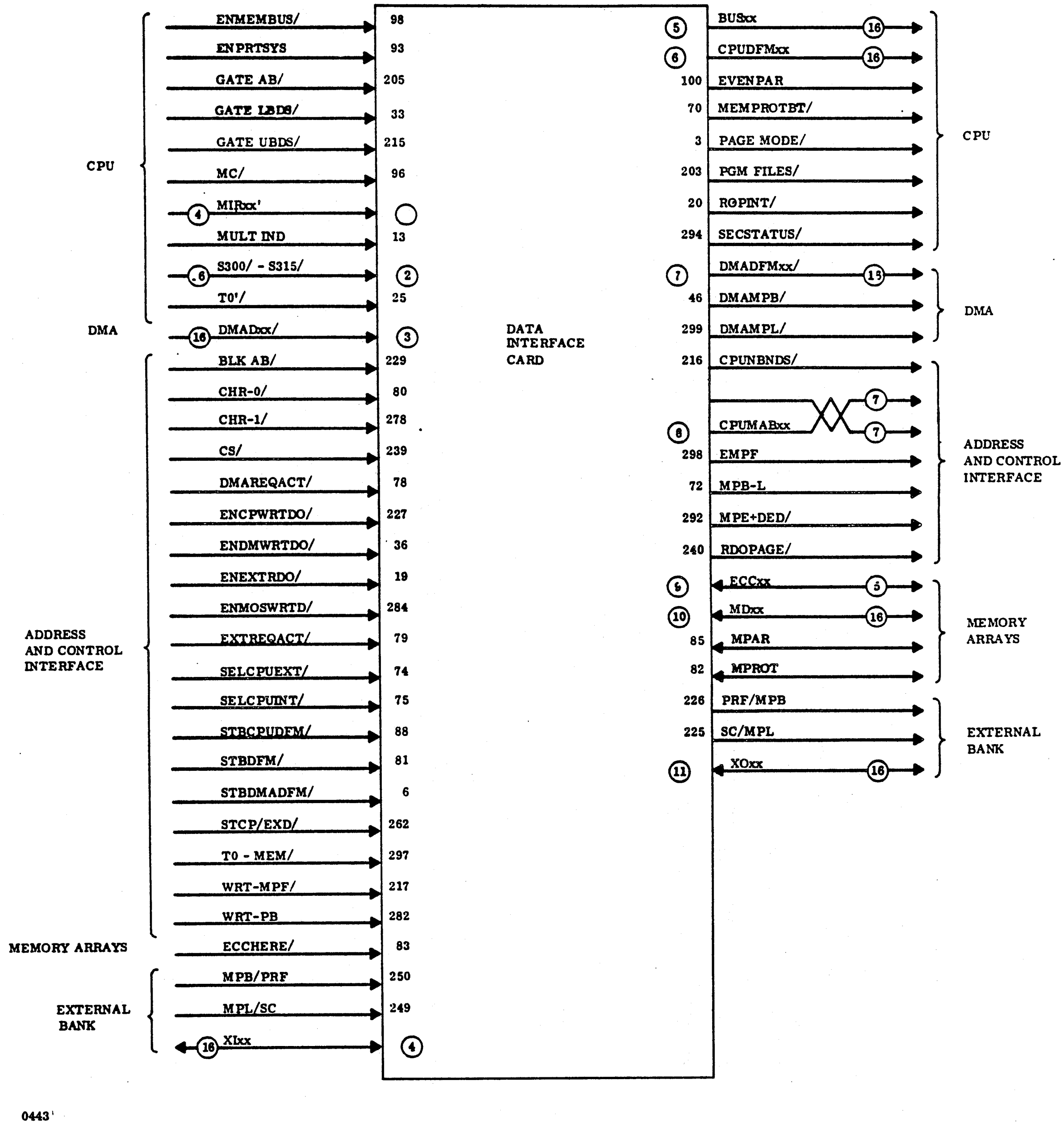


Figure 5-2. Data Interface Signals (Sheet 1 of 2)

(1)

MIRxx	
MIR28'	9
MIR29'	300
MIR30'	7
MIR31'	11

(2)

S300/ - S315/	
S300/	54
S301/	56
S302/	55
S303/	53
S304/	39
S305/	41
S306/	40
S307/	38
S308/	23
S309	28
S310/	24
S311/	22
S312/	29
S313/	35
S314/	15
S315/	27

(3)

DMADxx/	
DMAD01/	76
DMAD02/	261
DMAD03/	31
DMAD04/	228
DMAD05/	253
DMAD06/	252
DMAD07/	42
DMAD08/	258
DMAD09/	257
DMAD10/	37
DMAD11/	45
DMAD12/	60
DMAD13/	62
DMAD14/	61
DMAD15/	59
DMAD16/	52

(4)

XIxx	
XI01	209
XI02	208
XI03	207
XI04	206
XI05	211
XI06	213
XI07	218
XI08	214
XI09	212
XI10	210
XI11	220
XI12	222
XI13	224
XI14	223
XI15	221
XI16	219

(5)

BUSxx	
BUS00	92
BUS01	94
BUS02	95
BUS03	91
BUS04	295
BUS05	43
BUS06	44
BUS07	57
BUS08	84
BUS09	97
BUS10	64
BUS11	296
BUS12	89
BUS13	99
BUS14	10
BUS15	283

(6)

CPUDFMxx	
CPUDFM01	71
CPUDFM02	73
CPUDFM03	66
CPUDFM04	77
CPUDFM05	63
CPUDFM06	65
CPUDFM07	267
CPUDFM08	69
CPUDFM09	86
CPUDFM10	291
CPUDFM11	260
CPUDFM12	58
CPUDFM13	259
CPUDFM14	266
CPUDFM15	275
CPUDFM16	276

(7)

DMADFMxx	
DMADFM01	264
DMADFM02	241
DMADFM03	5
DMADFM04	47
DMADFM05	14
DMADFM06	32
DMADFM07	17
DMADFM08	30
DMADFM09	16
DMADFM10	8
DMADFM11	18
DMADFM12	265
DMADFM13	12
DMADFM14	67
DMADFM15	21
DMADFM16	34

(8)

CPUMABxx	SIG SLV	GND STRIP VW†
CPUMAB12/	50	50
CPUMAB13/	48	48
CPUMAB14/	49	49
CPUMAB15/	51	50
CPUMAB16/	270	70
CPUMAB17/	26	26
CPUMAB18/	68	68

(9)

ECCxx	
ECC00	87
ECC01	285
ECC02	288
ECC03	90
ECC04	289

(10)

MDxx	
MD00	255
MD01	268
MD02	269
MD03	256
MD04	280
MD05	277
MD06	271
MD07	263
MD08	272
MD09	274
MD10	281
MD11	273
MD12	293
MD13	290
MD14	286
MD15	287

(11)

XOxx	
XO01	233
XO02	232
XO03	231
XO04	230
XO05	235
XO06	237
XO07	242
XO08	238
XO09	236
XO10	234
XO11	244
XO12	246
XO13	248
XO14	247
XO15	245
XO16	243

† TWISTED PAIR, BLUE WIRE TO GROUND. POSITION VW REFERS TO STRIP LOCATED BETWEEN SLOTS V AND W. PIN DESIGN NUMBERS ARE 4-50 AND 53-102.

Figure 5-2. Data Interface Signals (Sheet 2 of 2)

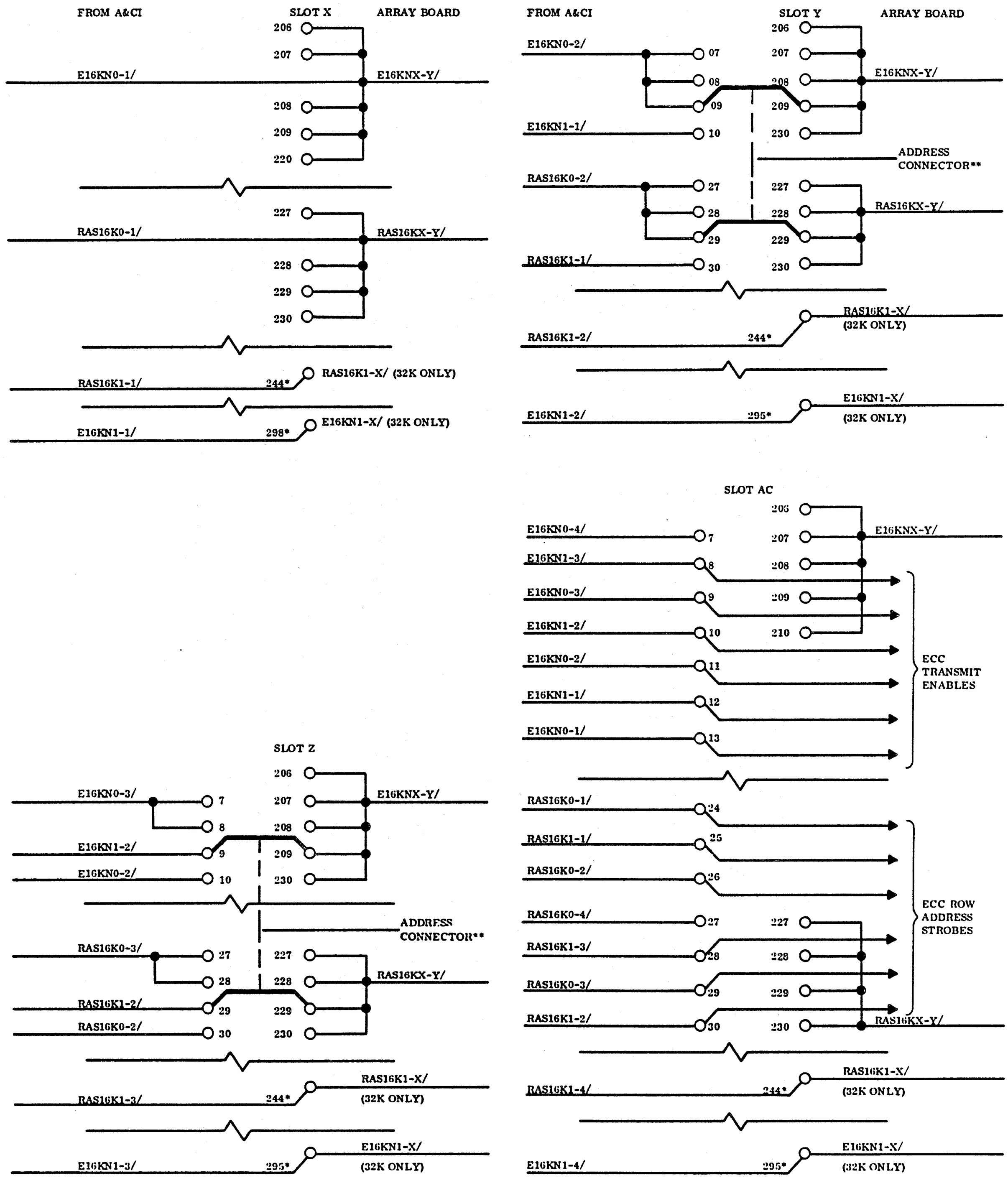
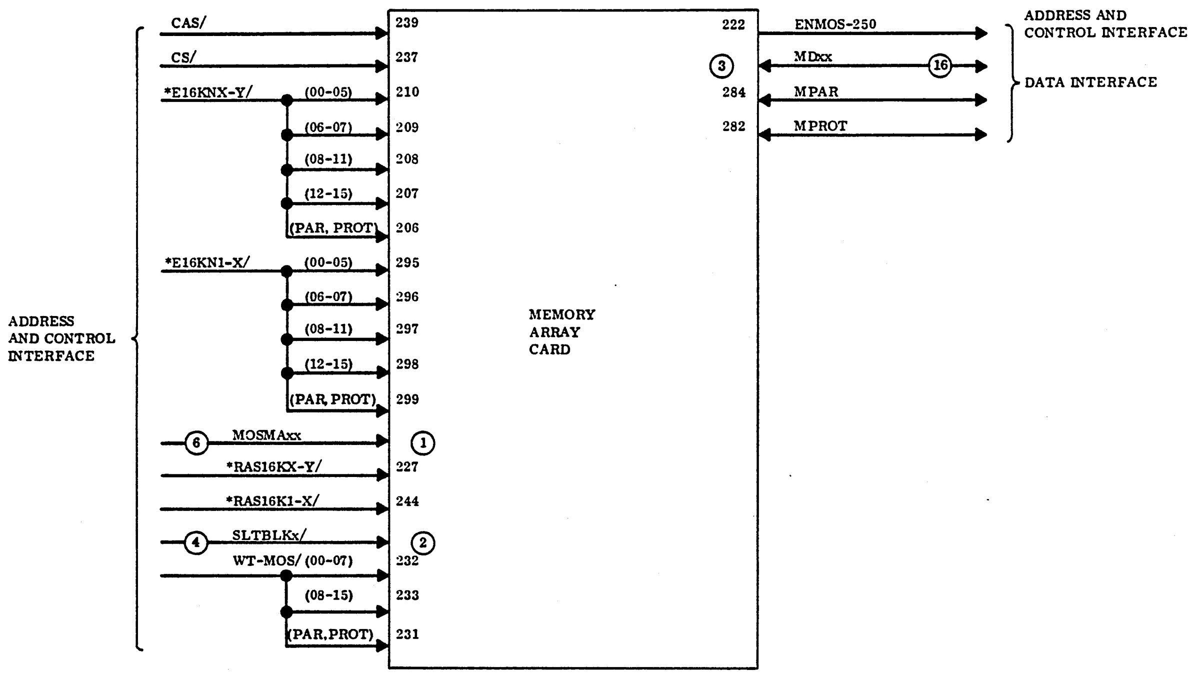


Figure 5-3. MOS Memory Array Signals (Sheet 1 of 2)



① MOSMAxx

MOSMAxx	
MOSMA00	258
MOSMA01	257
MOSMA02	260
MOSMA03	259
MOSMA04	265
MOSMA05	264

② SLTBLKx/

SLTBLKx/	
SLTBLK0	238
SLTBLK1	235
SLTBLK2	241
SLTBLK3	242

③ MDxx

MDxx	
MD00	255
MD01	268
MD02	269
MD03	256
MD04	280
MD05	277
MD06	271
MD07	263
MD08	272
MD09	274
MD10	281
MD11	273
MD12	293
MD13	290
MD14	286
MD15	287

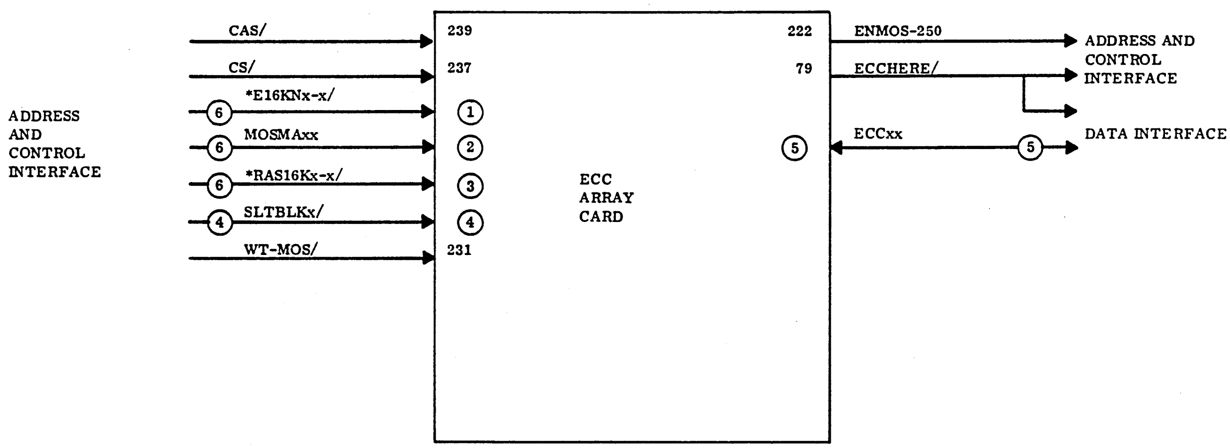
*THE FOLLOWING PINS ARE STRAPPED TOGETHER ON THE BACK PLANE:

E16KNX-Y/: 206, 207, 208, 209, 210
E16KN1-X/: 295, 296, 297, 298, 299
RAS16KX-Y/: 227, 228, 229, 230
WT-MOS/: 231, 232, 233

**ADDRESS CONNECTOR (NO. 96762000) SHOWN IN POSITION (TOP PINS 9, 209) FOR THE FOLLOWING MEMORY CONFIGURATION:

SLOT X: 32K
SLOT Y: 16K
SLOT Z: 16K
SLOT AC: ECC

Figure 5-3. MOS Memory Array Signals (Sheet 2 of 2)



1

E16KNx-x/	
E16KN0-1/	13
E16KN1-1/	12
E16KN0-2/	11
E16KN1-2/	10
E16KN0-3/	9
E16KN1-3/	8

3

RAS16Kx-x/	
RAS16K0-1/	24
RAS16K1-1/	25
RAS16K0-2/	26
RAS16K1-2/	30
RAS16K0-3/	29
RAS16K1-3	28

4

SLTBLKx/	
SLTBLK0/	238
SLTBLK1/	235
SLTBLK2/	241
SLTBLK3/	242

2

MOS MAxx	
MOS MA00	258
MOS MA01	257
MOS MA02	260
MOS MA03	259
MOS MA04	265
MOS MA05	264

5

ECCxx	
ECC00	83
ECC01	85
ECC02	88
ECC03	91
ECC04	89

*SEE ALSO BACKPLANE NOTES FOR SLOT AC IN FIGURE 5-3.

Figure 5-4. ECC Array Signals

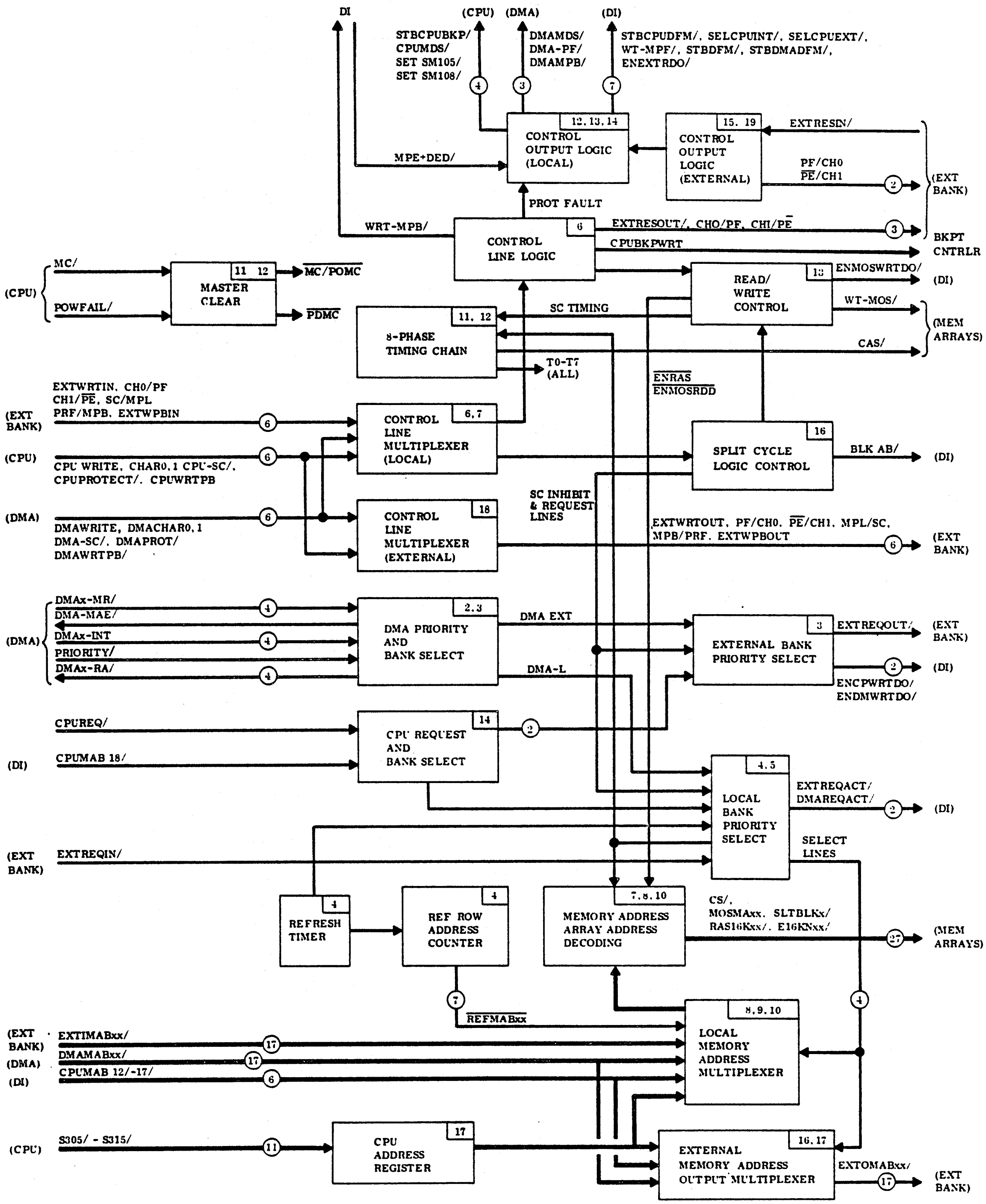


Figure 5-5. Address and Control Interface Block Diagram

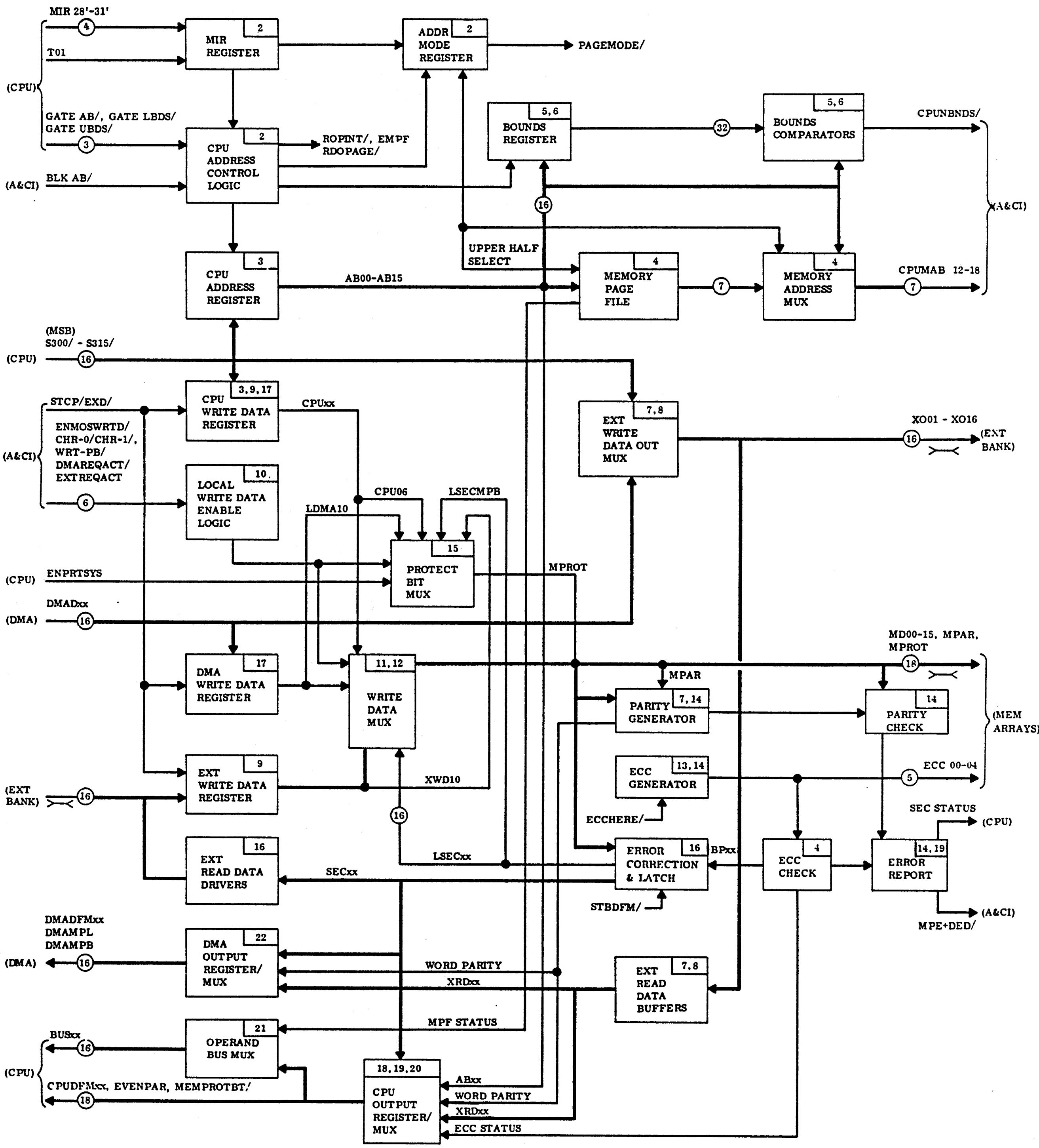


Figure 5-6. Data Interface Block Diagram

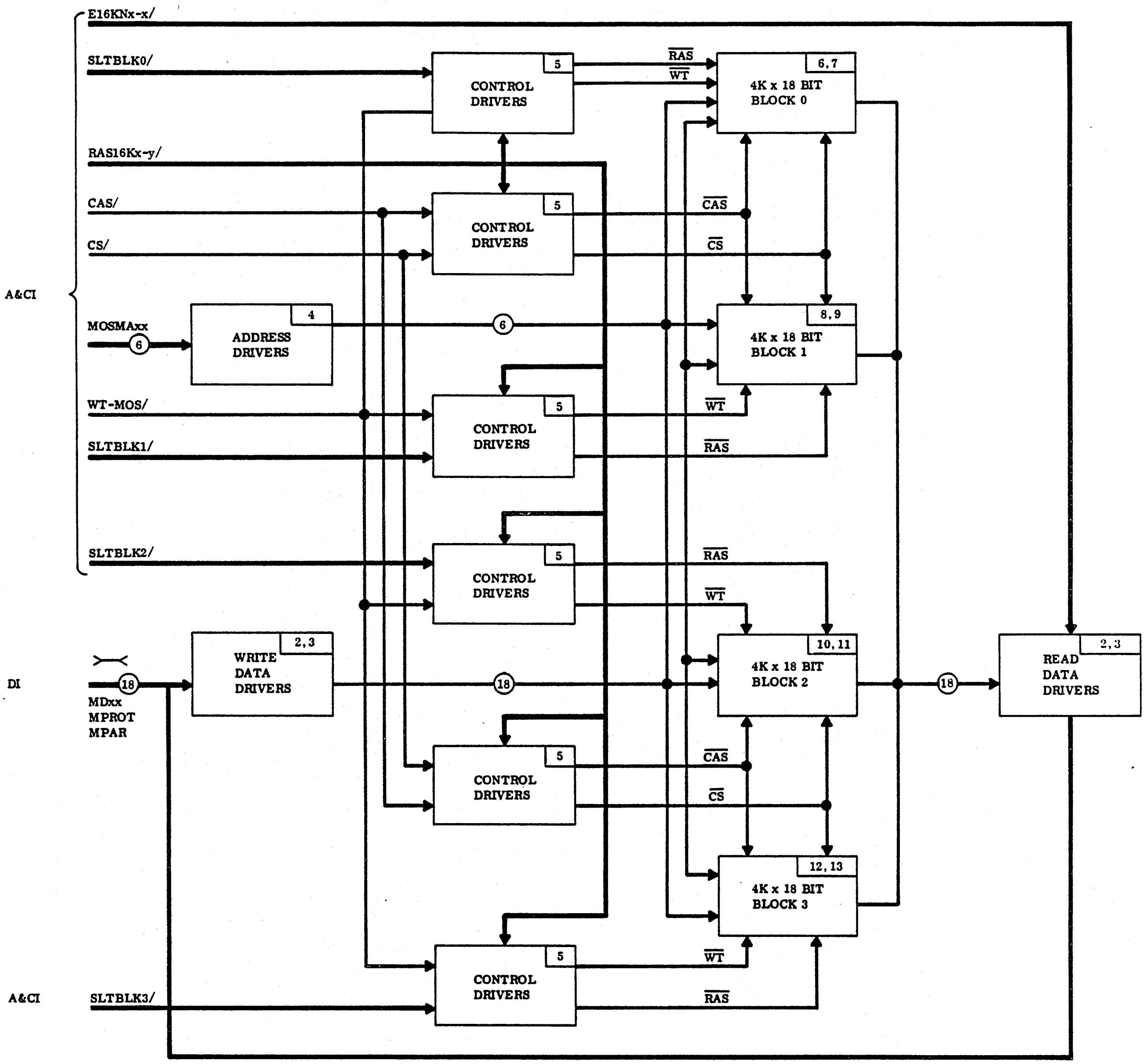


Figure 5-7. Memory Array Block Diagram

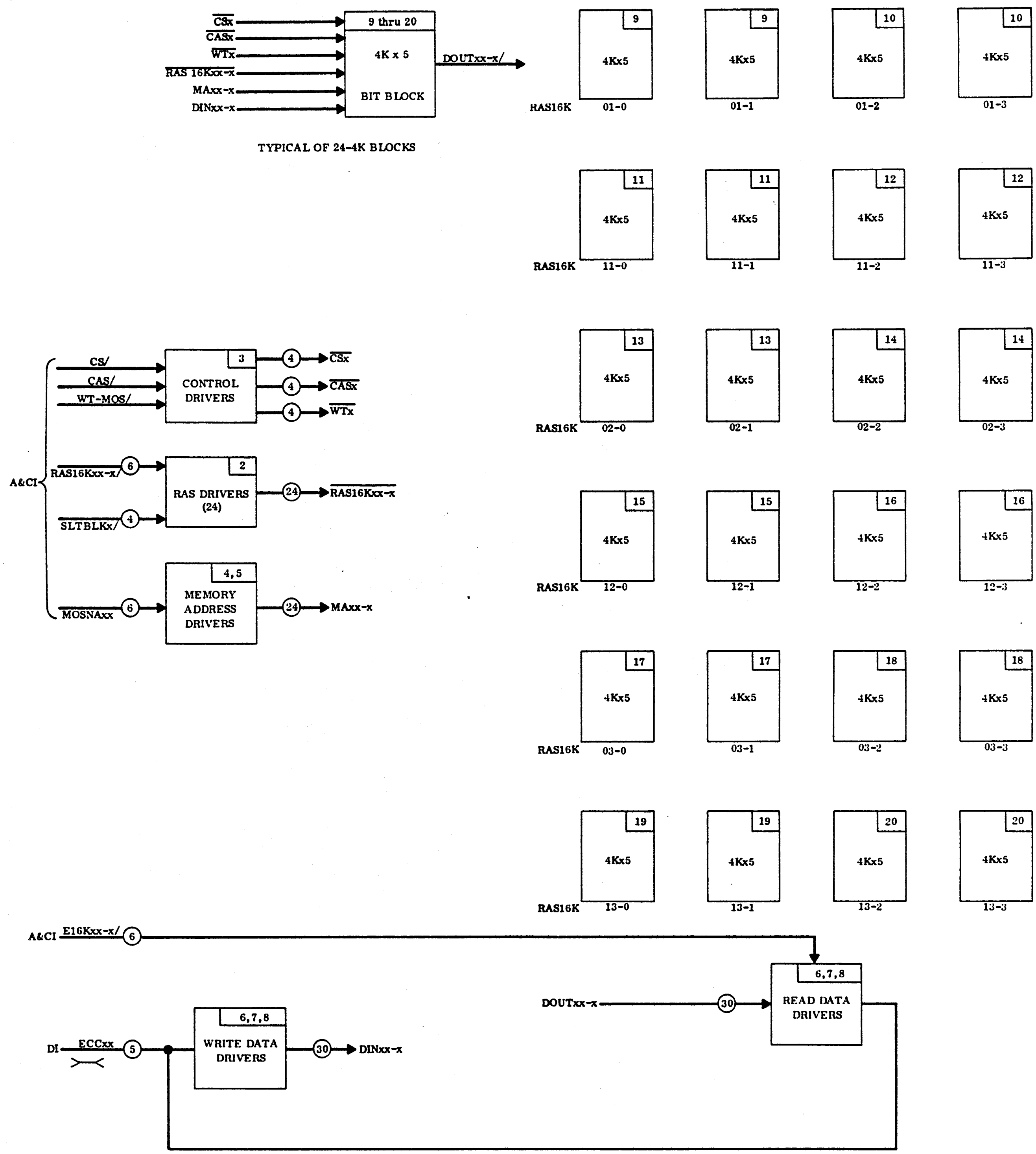


Figure 5-8. ECC Array Block Diagram

CPU REQUEST AND BANK SELECT CIRCUITS

The memory request input from the CPU is received on the CPUREQ/ line and latched in a flip-flop at B4. The flip-flop output, CPUREQ:

1. Generates the first STBCPUDFM/ signal through the gates at H1 and A9. This signal strobes the CPU address into the CPU data register for breakpoint compare on the CPU panel interface.

2. On a local bank request, (CPUMAB18/ false), generates the CPU local request CPUREQ-L to the local bank priority circuits through the gate at J4. This signal may be inhibited if a DMA or external read/modify/write cycle is in progress, or when the DMA PRIORITY/ line is true from the DMA.

   If DMA priority is selected the flip-flop at HJ1 is clocked low, inhibiting the CPU request until the DMA priority line is dropped. At this time, the flip-flop is set such that the next CPU request will be resynced properly.

3. On an external bank request (CPUMAB18/ true), generates the enabling CPUADR18 signal to the external bank priority select circuit through the gate at HJ2. This signal is inhibited if an external bank is not connected (EXTBANK/ false), the CPU memory address error flip-flop at B6 is set bringing the line $\overline{\text{CPUMAE}}$ true, which inhibits a write operation, thus forcing a local bank read cycle from the same address. A true EMPF/ line from the address and control interface also forces a local read cycle to provide the timing for the loading or statusing of the memory page file.

A CPUREQ signal is also generated internally for the write portion of a read/modify/write cycle, by a $\overline{\text{CPUSCREQ}}$ or $\overline{\text{CPUEXSCRQ}}$ signal from the read/modify/write cycle logic.

REFRESH TIMER/ADDRESS COUNTER

Timer N5 is set for a 15.6 microsecond period and feeds the clock input of the refresh row address counter at L6 and M5. The counting provides every combination of the 64 row addresses through the outputs $\overline{\text{REFMAB01}}$ through $\overline{\text{REFMAB16}}$, selecting half of each MOS memory array board for refresh on alternate cycles by the $\overline{\text{REFMAB15}}$ output. Thus, the entire local memory bank is refreshed every 128 cycles, or two milliseconds. The counter clock also serves as a refresh request to the local bank priority select circuits.

LOCAL BANK PRIORITY SELECT CIRCUITS

Priority is determined first among the three higher priority request inputs—DMA local requests, external requests and refresh requests. Then, priority is determined between the highest priority among these three requests and a CPU request. The highest priority request determines the source of data, address, and control information for the completion of the memory cycle.

Requests from the refresh timer are latched in the flip-flop at M4, and external requests from the EXTREQIN/ line in the flip-flop at J6. A latched DMA-local request is available from the DMA priority select circuit at gate A2 pin 12.

The latched refresh, external, and DMA-local requests are received through the gates at L3 and are latched by the request priority flip-flops at M3 (DMA-local, external) and M4 (refresh). If one or more of the flip-flops is set, further requests are blocked out by the L3 gates, as are requests made during a read/modify/write split cycle.

Once one or more of the request priority flip-flops are set, the flip-flop at K3 is clocked low, and the output DMAREQ (representing a DMA or higher priority request) is available to the DMA active latch. After a 40-nanosecond resync delay through the delay circuit at S1 the flip-flop at L2 is set, which enables the priority select gates at N3, P2 and P4.

The DMA active flip-flop at L4 is set directly by the DMAREQ signal if no CPU local request is in progress and the $\overline{\text{RESYNCINT}}$ line is false ($\overline{\text{RESYNCINT}}$ is a CPU request resync signal generated by the flip-flop at H3 from the CPU timing signals). Otherwise, the DMA active flip-flop is set at T6 time or when the $\overline{\text{RESYNCINT}}$ line returns false. After the present cycle is complete (MEMHALT true) an STRMOSADR signal is generated at gate N4 pin 12 through the gates at P3 and R4 plus the delay circuit at S3, which allows the selected address and control lines to stabilize. The address and control lines are selected by the outputs of the priority select gates and consist of the lines $\overline{\mathrm{ENDMAADR}}$, $\overline{\mathrm{ENCPUADR}}$, $\overline{\mathrm{SELREFRESH}}$, and $\overline{\mathrm{EXTSEL}}$. On external or DMA requests, either the EXTSEL2 or DMASEL2 flip-flop at L5 is clocked true by the STRCONT timing signal, which provides the data select signals EXTREQACT/ or DMAREQACT/ to the data interface, and EXTREQACT or DMAREQACT to the local bank control output logic.

The request priority flip-flops at M3 and M4 are cleared at T4 time by the RESYNDMA/EXT resync signal, and waiting priority requests may be accepted at that time unless a read/modify/write cycle is in progress, when one or both of the inhibit lines $\overline{\mathrm{CPDMSC/PR}}$ or $\overline{\mathrm{CPU/EXTSC}}$ are true.

The CPU active flip-flop at L4 is set directly by the CPUREQ-L signal if no memory cycle is in progress (MEMHALT true) and the DMA active flip-flop is not set; an immediate STRMOSADR signal is generated at gate N4 pin 2 to start a CPU memory cycle. If a DMA or higher priority memory cycle is in progress, the CPU active flip-flop is clocked true at T6 time, and the STRMOSADR signal is generated through the gates at N4 at the conclusion of the cycle.

EXTERNAL BANK PRIORITY SELECT CIRCUITS

A DMA external bank request is made by the DMA priority and bank select circuit and is made available to the external bank priority select circuit at gate A2 pin 8. A CPU external request requires the two signals CPUREQ and CPUADR 18 from the CPU request and bank select circuit. Write portions of read/modify/write cycles are requested via the lines $\overline{\mathrm{DMAEXSCRQ}}$ for a DMA cycle, and the same CPUREQ and CPUADR18 lines for a CPU cycle.

An incoming request is latched by either the DMAEXTREQ or CPUEXTREQ flip-flop at E1. A DMA request also sets the flip-flop at K1, which enables the DMA address to the external bank via the line DMAEXTSEL, and generates an external bank request EXTREQOUT/ through the gate at K2 and driver at R3. A CPU request also generates an EXTREQOUT/ signal through the same gate and driver and enables the CPU address to the external bank via the line CPUEXTSEL to the CPU and DMA select flip-flops at NP1. These flip-flops provide the select lines to the external address and control multiplexer, and to the external write data out multiplexer in the data interface via the lines ENCPWRTDO/ or ENDMWRTDO/.

The CPU and DMA external request latches are reset at the end of the external cycle by the EXTRESYNC signal, which allows the next external bank request to be processed.

CPU ADDRESS REGISTER

The least significant 11 CPU address bits from lines S305/ through S315/ (LSB) are clocked into the CPU address register at J7 and K7 by the GATE AB/ signal from the CPU. The register output lines are $\overline{\mathrm{CPUMAB01}}$ through $\overline{\mathrm{CPUMAB11}}$. The most significant bits CPUMAB12/ through CPUMAB17/ are supplied by the data interface.

LOCAL MEMORY ADDRESS MULTIPLEXER

Memory addresses from the CPU address register, DMA port, external port, and refresh address counter are available to the local memory address multiplexer, consisting of three-state two-input multiplexers located at L7, L8, L9, M7, M8, M9, R8, R9, and part of S8 and S9. Addresses are selected according to the following truth table:

CPU ($\overline{\mathrm{CPUMAB01}}$ through $\overline{\mathrm{CPUMAB11}}$, CPUMAB12/ through CPUMAB17/	$\overline{\mathrm{ENCPUADR}}$ true, $\overline{\mathrm{SELREFRESH'}}$ false
DMA (DMAMAB01/ through DMAMAB17/)	$\overline{\mathrm{ENDMAADR}}$ true, $\overline{\mathrm{EXTSEL'}}$ false
External (EXTIMAB01/ through EXTIMAB17/)	$\overline{\mathrm{ENDMAADR}}$ true, $\overline{\mathrm{EXTSEL'}}$ true
Refresh ($\overline{\mathrm{REFMAB01}}$ through $\overline{\mathrm{REFMAB06}}$, $\overline{\mathrm{REFMAB15}}$)	$\overline{\mathrm{ENCPUADR}}$ true, $\overline{\mathrm{SELREFRESH'}}$ true

MEMORY ADDRESS/ARRAY ADDRESS DECODING

The 12 least significant memory address bits, as selected by M8, L8, L9, L7, M9, and M7 are strobed into registers M6 and N7 by the STRMOSADR signal; the least significant six bits in N7, the next most significant in M6.

The line $\overline{\text{RAE}}$, when low, gates the six bits in N7 through selector P7 to the lines MOSMA00 through MOSMA05, forming the row address to the memory array boards. Later, the line $\overline{\text{CAE}}$ gates the six bits in M6 through selector N6 to the same lines to the memory arrays, forming the column address.

The two least significant bits from selectors R8 or R9, representing memory address bits 13 and 14, are routed through gates at F6 to a two to four-line decoder, the NAND gates F7, and strobed into the block select register F8 by the STRMOSADR line. The one low line of the four outputs is one of the 4K block select lines SLTBLK0/ through SLTBLK3/, to the memory array.

Into the same F8 register are strobed the memory address bit 15, from R8 or R9, and the level on the $\overline{\text{SELREFRESH}}$ line. When low, the $\overline{\text{SELREFRESH}}$ line also forces both gates at F6 high, thus selecting all four block select lines simultaneously, and the line CS/ to the memory array high to support a refresh cycle.

Memory address bits 16 and 17 from R8 or R9 and S8 or S9 are strobed into register S6 by the STRMOSADR line. These two lines plus bit 15 from F8 are decoded by the three-to-eight-line decoders D7 and D8. The output from D7 selects one of the eight row address strobes RAS16K0-1/ to RAS16K1-4/ when selectors E7 and E8 are enabled by the $\overline{\text{ENRAS}}$ line. When $\overline{\text{SELREFRESH}}$ is low all the inputs to selector E7 and the inputs to E8 are tied through the inverter at H6 to bit 15. Thus, half the row address strobes are selected on a refresh cycle, alternating with the level on bit 15. The outputs of decoder D8 select one of the eight transmit enables E16KN0-1/ to E16KN1-4/, to the memory array boards. The outputs are enabled during a read cycle by the $\overline{\text{ENMOSRDD}}$ line from the write logic.

EXTERNAL MEMORY ADDRESS OUTPUT MULTIPLEXER

Memory addresses from the CPU address register and DMA port are available to the external memory address output multiplexer, consisting of three-state, two-input multiplexers located at J8, J9, K8, K9, P8, and P9. The inputs $\overline{\text{CPUMAB01}}$ through $\overline{\text{CPUMAB11}}$ and CPUMAB12/ through CPUMAB17/ or DMAMAB01/ through DMAMAB17/ are selected by the active CPU or DMA external select latch at NP1 to the external memory address outputs EXTOMAB01/ through EXTOMAB17/.

CONTROL LINE MULTIPLEXERS

Incoming control line information from the CPU, DMA, and external ports is selected by the same select line as memory address information. Some incoming lines are modified by control line logic before selection:

- CPUWRITE, CPUWRT — The CPUWRITE input is inhibited at the gate H7 by (1) the RDOPAGE/ input from the data interface, indicating a read-only page has been accessed in page mode, (2) $\overline{\text{CPUMAE}}$, indicating the external bank was requested but none is connected, and (3) the EMPF line from the data interface, indicating a load or read MPF instruction is in process. The inhibited line CPUWRT is fed to the control logic multiplexers.

- CPUPROTECT/, CPUPROT — A gate at G7 allows the CPUPROTECT/ line, the CPUNBNDS/ line, or a low ENPRTSYS line to set the CPU program protect line to the control line multiplexers (CPUPROT) true.

- CHAR0, CPUCHAR0 — A gate at G9 allows the CPU write protect bit line CPUWRTPB to inhibit the CHAR0 input, thus forcing a restore operation on the most significant eight data bits. The inhibited line CPUCHAR0 is fed to the control line multiplexers.

- DMA WRITE, DMAWRT — A gate at G9 allows the DMAMAE/ addressing error signal to inhibit the DMA WRITE line, indicating the external bank was requested but none is connected. The inhibited write line DMAWRT is fed to the control line multiplexers.

- DMAPROT/, DMAPROT — A gate at G9 allows either the DMAPROT/ input or a low ENPRTSYS line to set the DMA program protect line to the control line multiplexers (DMAPROT) true.

The control line multiplexers for the local bank are the three-state, two-input multiplexers at R7, S7, and parts of S8 and S9. The multiplexer outputs feed the control line registers at R6 and S6. The external bank control line multiplexers are at H8 and H9. Table 5-1 shows the multiplexer inputs and outputs.

EIGHT-PHASE TIMING CHAIN

The STRMOSADR signal from the local priority select circuit starts a memory cycle by clocking the flip-flop at J6 low. After a 30-nanosecond delay by the delay circuit at J6, the $\overline{\text{ENRAS}}$ line goes low, enabling the row address strobe to the selected MOS memory array. After a 50-nanosecond delay, the flip-flop at H5 is set through the gates at D6 and G6 (100 nanoseconds through the gates at F6 and G6 for a full word write cycle with protection disabled), and the STRCONT signal is generated. This flip-flop controls the operation of the timing chain. When set by the delayed STRMOSADR signal, the line MEMHALT goes false, terminating the STRMOSADR signal.

The eight-phase timing chain consists of the clock gates at J4 and J5, the four-bit counter circuits at G5 (even clock) and F5 (odd clock), the delay circuit at G2, the timing selector at G3, and the restart gate at H7. The clock gates are enabled by the setting of the flip-flop at H5, causing the counter at G5 to be clocked and the first, or T0, output to appear. At the same time the gate output of J5 pin 8 sends a clock signal to the delay circuit at G2. The time delay selected (20 or 30 nanoseconds) is determined by the ENMOS-250 input from the arrays. If one or more of the arrays is a slow array, causing ENMOS-250 to be low, the 30 nanosecond time is selected by the three-state drivers at G3. With circuit propagation delays, the time between clocking of the G5 and F5 counters is either 40 or 50 nanoseconds.

Alternate clocking of the G5 and F5 timing registers produces an eight-phase, overlapping timing chain with outputs T0 through T7 and the complements $\overline{\text{T0}}$ through $\overline{\text{T7}}$. At T7 time the flip-flop at H5 is clocked back low on single cycles, stopping the clocking of the timing chain. Single cycles are read cycles or full word write cycles with protection disabled. On a normal write operation the WRT-SC flip-flop at K3 inhibits the first T7 reset signal through the gate at F4, allowing the timing chain to start again after T6 time through the gates at D2 and D3 if ECC is not installed, or after T7 time with ECC. The timing chain output is shown in figure 5-9, along with the abbreviated representation used in the read/write cycle timing diagrams.

The three-state timing multiplexer at E5 receives the $\overline{\text{T3}}$, $\overline{\text{T4}}$, and $\overline{\text{T6}}$ timing signals at one set of inputs; $\overline{\text{T4}}$, $\overline{\text{T5}}$, and $\overline{\text{T7}}$ at the other. When the ECC option is installed, the later timing signals are used to provide the additional delay needed for the ECC check bits to be decoded and single bit errors corrected. The affected circuits are described in this section showing both times (e.g., T6 (T7) indicates the T6 time is used without ECC, T7 time with ECC). A delay circuit at A5 provides the additional timing signals of T6 (T7)+50 nanoseconds and T6 (T7)+100 nanoseconds. The outputs of this E5 multiplexer are disabled through the gates at D5 during the write portion of a protected write cycle.

Additional timing signals are generated for other parts of the system. The memory resync flip-flop at H5 generates a resync signal to the local priority select circuits, MEMRESYNC, which is low from time T4 to T7. The STCP/EXD/ signal from gate D4 pin 11 is a double pulse at T0 and T2 times which strobes write data into registers in the data interface. The $\overline{\text{RAE}}$ and $\overline{\text{CAE}}$ outputs from the flip-flop at E3 select row address or column address to the MOSMAxx lines, with $\overline{\text{CAE}}$ true from T1 to T5 time and $\overline{\text{RAE}}$ true at all other times. The column address strobe $\overline{\text{CAS}}$ from the other flip-flop at E3 is sent at T1 time (delayed somewhat by device delays).

CONTROL LINE LOGIC AND READ/WRITE CONTROL

The control line information latched in the registers at R6 and S6 determine the action taken during a memory cycle. When the write line is true, three gates at S5 and P5 determine whether a single cycle write or read/write split cycle will be executed.

TABLE 5-1. CONTROL LINES

Control Function	Multiplexer Input	Local Bank		External Bank	
		Multiplexer	Register	Multiplexer	Output Line
Write	CPU WRT	S8	R6	H8	
	DMAWRT	S9		H9	EXTWRTOUT
	EXTWRTIN	S9		—	
Character 0	CPUCHAR0	R7		H8	
	DMACHAR0	S7		H9	PF/CH0
	CH0/PF	S7		—	
Character 1	CHAR1	R7		H8	
	DMACHAR1	S7		H9	$\overline{\text{PE}}$/CH1
	CH1/$\overline{\text{PE}}$	S7		—	
Split Cycle	CPU-SC/	R7		H8	
	DMA-SC/	S7		H9	MPL/SC
	SC/MPL	S7		—	
Program Protect	CPUPROT	R7	S6	H8	
	DMAPROT	S7		H9	MPB/PRF
	PRF/MPB	S7		—	
Write Protect Bit	CPUWRTPB	S8		H8	
	DMAWRTPB/	S9		H9	EXTWPBOUT
	EXTWPBIN	S9		—	

The $\overline{\text{FUL-WRT}}$ line is brought low to initiate a single cycle write operation when the ENPRTSYS line is false and both the character 0 and character 1 lines are true. In all other conditions when the write line is high a read/write split cycle is initiated by the line WRITE-SC, which conditions the WRT-SC flip-flop at K3 to be clocked low at T2 time, and clocked back high at the second T2 time (T2*).

When $\overline{\text{FUL-WRT}}$ is true, the write flip-flop at F2 is clocked high at T2 time, bringing the WT-MOS/ write control line to the memory arrays true until T6 time, when the flip-flop is cleared through the gate at D6. The read/write data select flip-flop also at F2 is preset by the STRMOSADR signal, bringing the ENMOSWRTD/ line true, enabling write data to the memory data lines from the data interface.

On a normal write cycle the flip-flops at F2 are clocked low at T2 time for the read portion of the cycle, bringing $\overline{\text{ENMOSRDD}}$ true, which enables the selected transmit enable line to the memory arrays. At T6 (T7)+50 nanoseconds the read/write data select flip-flop is clocked high, and at the second T2 time the write flip-flop is clocked high for the write portion of the cycle and cleared at the second T6 time.

On a read cycle, both flip-flops are clocked low at T2 time and remain low for the duration of the cycle.

Three conditions cause the write flip-flop to be held clear (WT-MOS/ held false) by the $\overline{\text{WRT-ABORT}}$ signal through the gate at D6:

- Protect parity error — When a parity error is detected from read data (or double error with

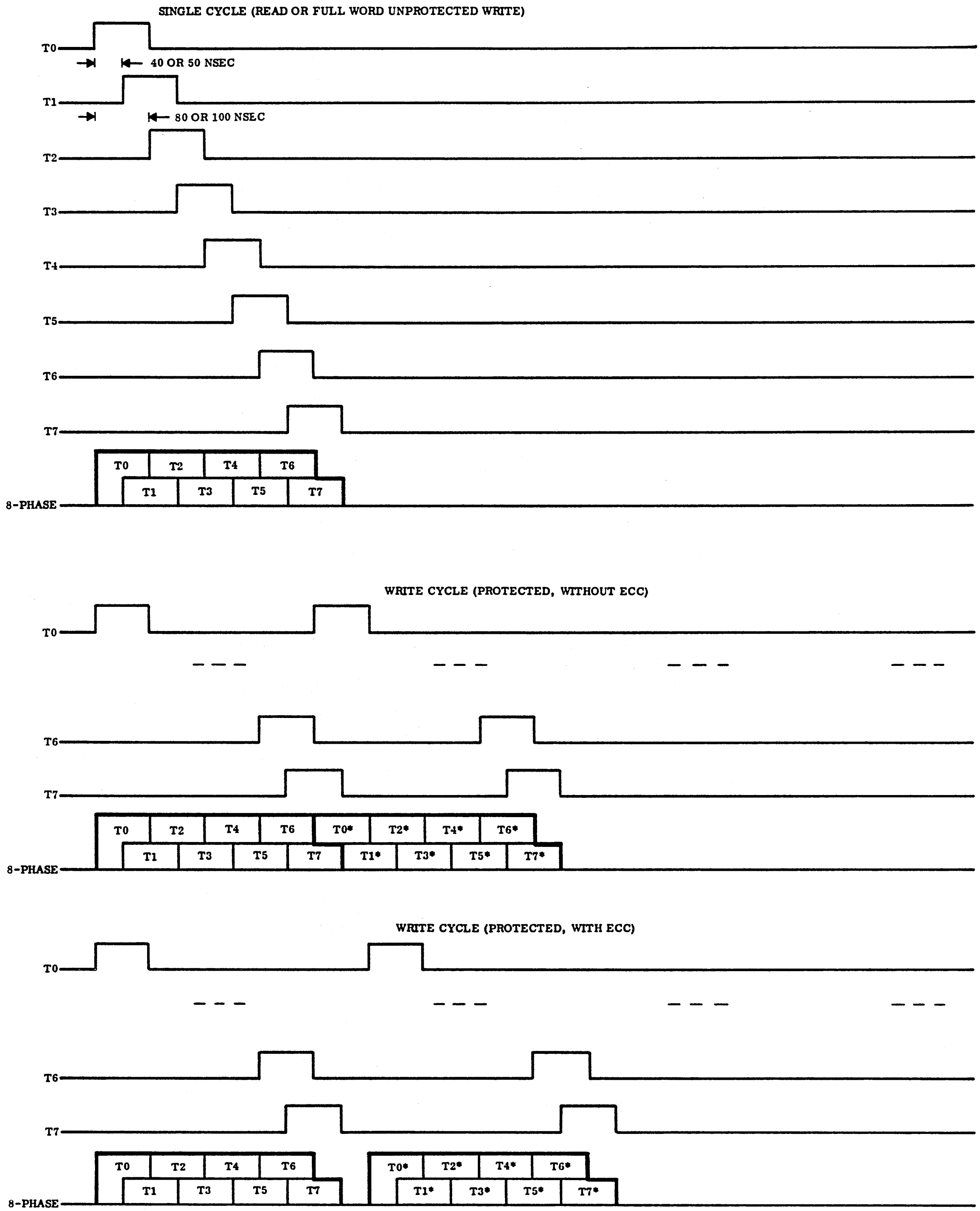


Figure 5-9. Eight-Phase Timing Chain

ECC) the line MPE+DED/ from the data interface goes true, and the MPE+DED flip-flop at C9 is clocked low. The true MPE+DEDFF line from the flip-flop and a true program protect line produce the WRT-ABORT signal through two gates at P5.

- Write protect bit parity error — When a parity error is detected (MPE+DEDFF true) and the write protect bit control line is true, the WRT-ABORT signal is produced through the gates at S5 and P5.

- Protect fault — When the protect bit from read data is true (MPB-L from the data interface) and the program protect line is false, the WRT-ABORT signal is produced through the gates at C7 and P5.

- CPUBKPWRT - When CPU-SC/ is low or CPUWRT is low, a CPUBKPWRT signal is applied to the breakpoint controller. This enables the breakpoint compare OPERAND.

On an aborted write operation, a normal write cycle is executed except that existing memory data is retained.

SPLIT CYCLE CONTROL LOGIC

The local split cycle control line latched in register R6 clocks the levels on ENDMAADR, ENCPUADR, and EXTSEL into the register at R2 at T0 time.

On a CPU local split cycle request, the request inhibit lines to the priority select circuits CPUSC-HLD, CPU/EXTSC, and CPDMSC/PR are brought true through gates at N2, and the resync line SCCLRDMA is brought true during T1 time to clear any waiting higher priority request. When the CPUWRT line goes high, the CPUSCREQ signal is generated through the gate at F4 to begin the write cycle.

On a DMA local split cycle request, the request inhibit lines to the priority select circuits DMASC-HLD and CPDMSC/PR are brought true through gates at S2 and N2, and DMA+EXTSC is also brought true. When the DMAWRT line goes high, the DMASCREQ signal is generated through the gate at P2 to begin the write cycle.

On an external split cycle request, the request inhibit lines to priority select circuits DMA+EXTSC and CPU/EXTSC are brought true, the latter through the gates at S2 and N2. The request for the write cycle is regenerated at the external bank and received over the EXTREQIN/ line.

On DMA- or CPU-external requests the incoming split cycle line DMA-SC/ or CPU-SC/ establishes a true or false level at the inputs to the external SC flip-flops at PR1. On a CPU-external split cycle request, one of the flip-flops at PR1 is clocked high by the CPU external select latch at NP1, bringing the inhibit line CPUEXSC-HLD true to the external bank priority select circuit, and the BLK AB/ line low to prohibit any CPU address change until the cycle is complete. When the CPUWRT line goes true, the second request signal CPUEXSCRQ line to the external bank priority select circuit is brought true, resulting in a second EXTREQOUT/ signal to the external bank to begin the write cycle. A DMA-external split cycle request is handled in a similar manner by the other flip-flop at PR1, producing the inhibit signal DMAEXSC-HLD and the second requestsignal DMAEXSCRQ.

CONTROL OUTPUT LOGIC—LOCAL BANK CYCLES

CPU Read/Write Cycles

On a CPU read or write request the output STBCPUDFM/ is sent to the data interface through the gates at H1 and A9, loading the CPU read data output register with the breakpoint address (current CPU memory address). After the request has been accepted and the memory cycle begins, the STRCONT line clocks the DMAACT flip-flop at B7 low, enabling the CPU control output gates. At T3 (T4) time the STBCPUBKP/ signal is sent to the CPU through gates at D5 and B5, informing the CPU that the CPU address is available on the data interface CPUDFMxx output lines; and at the same time the read data output select flip-flop at B4 is set, enabling the SELCPUINT/ line to the data interface through the gate at D4, selecting the local CPU read data to the CPU read data output register inputs. At T6 (T7) time the STBDFM/ signal is sent to the data interface to strobe read data into the restore registers, and the second STBCPUDFM/ signal sent through the gates at A7 and A9 to strobe read data into the CPU read data output register. The read data output select flip-flop at B4 is clocked back low to reselect the CPU address on the trailing edge of T6 (T7).

On a CPU read or normal write request the CPUMDS flip-flop at B7 is clocked low at T3 (T4) time, producing the WRT-MPF/ signal to the data interface through the gates at D5 and C5 if the CPUWRITE line is true; and, after a slight delay by the RC network R50/C52, the CPUMDS/ memory resume signal is sent to the CPU through the gate at C6. At T6 (T7)+50 nanoseconds time the parity error signal SET SM108/ is sent to the CPU through the gates at B8 and B9 if a parity error has been detected in the read data; and, on a normal write cycle, the protect fault signal SET SM105/ is sent if a protect fault is detected by the gate at C7 in the control line logic circuits. The control output logic is disabled at the E5 selector during the write portion of a normal write cycle.

On a CPU full word write cycle with protection disabled (single cycle), the CPUMDS/ signal is sent at T1 time through gates at C5 and C6, and the WRT-MPF/ signal is sent at the same time through gates at D5 and C5. Parity error and protect fault signals are not generated on this cycle.

DMA Read/Write Cycles

On a DMA read or write cycle the input DMAREQACT from the DMASEL2 flip-flop enables the DMA control output gates. At T6 (T7) time the STBDFM/ signal is sent to the data interface to strobe read data into the restore registers, the STBDMADFM/ signal is generated through the gates at A7 and A9 to strobe read data into the DMA read data output register, and the DMAMDS/ memory resume signal is sent to the requesting DMA device. At T6 (T7)+50 nanoseconds time the complementary signals RESYNCDMA and $\overline{\text{RESYNCDMA}}$ are generated through the gates at A8 and C6 to clear the DMA priority flip-flops so a new request can be processed.

On a read or normal write cycle the parity error signal DMAMPE/ is sent at T6 (T7)+50 nanoseconds time through gates at B8 and B9 if a parity error has been detected in the read data, and, on a normal write cycle, the protect fault signal DMA-PF/ is sent if a protect fault is detected. There are no DMA control line outputs during the write portion of a normal write cycle.

External Read/Write Cycles

On an external read or write cycle the input EXTREQACT from the EXTSEL2 flip-flop enables the first flip-flop at C8 to be clocked high at T4 (T5) time. The output of the flip-flop produces the memory resume signal EXTRESOUT/ to the external bank until T6 (T7) time when the flip-flop is cleared, and the second flip-flop at C8 is clocked low. This flip-flop produces the outputs ENEXTRDO/ to the data interface, which enables read data on to the XIxx lines to the external bank; and $\overline{\text{ENEXTSTAT}}$, which enables any detected parity error or protect fault to the CH1/PE or CH0/PF lines, respectively, to the external bank. There are no external control outputs during the write portion of a normal write cycle.

CONTROL OUTPUT LOGIC—EXTERNAL BANK CYCLES

CPU-External Read/Write Cycles

On a CPU-external read or write request, the output STBCPUDFM/ is sent to the data interface through the gates at H1 and A9, loading the CPU read data output register with the breakpoint address (current CPU memory address). No further control output logic activity takes place until the memory resume signal is received from the external bank.

When the memory resume signal EXTRESIN/ is received, the following occurs:

1. The external select latches at NP1 are set, disabling memory address and control line information to the external bank.

2. The $\overline{\text{STRCPBPEXT}}$ signal is set true through the gate at M2.

3. This signal sets the DMAACT flip-flop at B7 and the read data output select flip-flop at B4, bringing the line SELCPUEXT/ to the data interface true to select external read data as the input to the CPU read data output multiplexer, sends the STBCPUBKP/ signal through the gate at B5 to inform the CPU that the breakpoint address is available over the CPUDFMxx lines, and clocks the CPUMDS flip-flop at B7 low to send out the CPUMDS/ memory resume signal and, on a write cycle, the WRT-MPF/ signal.

At the trailing edge of the EXTRESIN/ input, the flip-flop at K6 is clocked low, driving delay circuit N1, which provides the timing for the remaining control line outputs. The $\overline{\text{STBCPUEXT}}$ signal generated through the gate at M2 in turn generates the STBCPUDFM/ signal through the gate at A9, strobing the external read data into the CPU read data output register. Next, the parity error and protect fault information from the external bank over lines PE/CH1 and PF/CH0 are clocked into the register at G4. Finally, the $\overline{\text{STCPUPEEXT}}$ and $\overline{\text{STCPUPFEXT}}$ signals are generated from the G4 register outputs, which in turn generate the parity error output SET SM108/ and/or the protect fault signal SET SM105/ through the gates at B9 and A9. Also at this time the EXTRESYNC signal through the gate at M2 clears the external priority select flip-flops.

DMA-External Read/Write Cycles

No control logic output activity occurs on a DMA-external read or write cycle until memory resume signal EXTRESIN/ is received from the external bank, at which time the external select latches at NP1 are set, disabling memory address and control line information to the external bank.

At the trailing edge of the EXTRESIN/ input, the flip-flop at K6 is clocked low, driving delay circuit N1, which provides the timing for the remaining control line outputs. First, the $\overline{\text{STBDAMEXT}}$ signal generated through the gate at M2 in turn generates the STBDMADFM/ signal through the gate at A9, strobing the external read data into the DMA read data output register. The memory resume signal DMAMDS/ is also sent at this time. Next, the parity error and protect fault information from the external bank over lines PE/CH1 and PF/CH0 are clocked into the register at G4. Finally, the $\overline{\text{STDMAPEEXT}}$ and $\overline{\text{STDMAPFEXT}}$ signals are generated from the G4 register outputs, which in turn generate the parity error output DMAMPE/ and/or the protect fault signal DMA-PF/ through the gates at B9. At the same time, the EXTRESYNC signal through the gate at M2 clears the external priority select flip-flops, and the $\overline{\text{EXTRESYNDMA}}$ signal through the gate at A3 generates the RESYNCDMA and $\overline{\text{RESYNCDMA}}$ signals to clear the DMA priority flip-flops.

MASTER CLEAR CIRCUITS

The master clear input from the CPU, the line MC/, sets the flip-flop at K6 through the gate at J5, producing the $\overline{\text{MC/POMC}}$ signal at the termination of the current read or write cycle. When the $\overline{\text{MC/POMC}}$ signal is false, the request and split cycle latches are cleared, and DMA and external resync signals generated. While MC/ remains false, only refresh cycles are executed. After MC/ returns true and the refresh master clear flip-flop H3-9 resets, $\overline{\text{POMC}}$ inhibits the power fail. The K-6 flip-flop is clocked back low to inhibit a master clear at power on. Memory operation returns to normal.

On systems with battery backup, a low POWFAIL/ signal from the CPU prohibits the reclocking of the K6 flip-flop until proper CPU operation is restored after a power interruption. The flip-flop is only clocked low after the POWFAIL/ line returns true.

POWER SUPPLY AND BATTERY BACKUP

The +5vdc power supply to the address and control interface is derived from two sources: the power supply from the CPU mainframe, and the optional battery backup supply. Circuits on the logic diagrams marked with a $\triangle$4 (96752174) or a $\triangle$1 (96890851) are powered by this optional supply and allow refresh cycles to continue in the event of a power shutdown. The refresh counter, priority select circuits, the timing chain, and other circuits necessary to provide refresh signals to the memory arrays remain powered from this optional supply to prevent loss of memory data.

DATA INTERFACE BOARD CIRCUITS

CPU ADDRESS CONTROL AND REGISTERS

Four CPU micro instruction register lines, MIR28' through MIR31', are clocked into the register A4 by the CPU clock input T0'/. The A4 outputs remain stable during CPU clock time T4 when the CPU address control signals GATEUBDS/, GATELBDS/, and GATEAB/ are active. The affect of these three control lines is shown in the CPU address control commands table in section 4.

If any of the three control lines is in the active low state and BLKAB/ is high, the line LOAD AB is enabled at gate B4. LOAD AB clocks the CPU address on lines S300/ through S315/ into the 16-bit AB register at C7, D7, E7, and F7. BLKAB/ is true only during a CPU read/modify/write cycle, to inhibit the loading of a new address before the split cycle is complete. The AB register outputs, AB00 (MSB) through AB15 and AB07 through AB15 are stable until a new address is clocked in by the LOAD AB signal.

Control line GATELBDS/ produces the $\overline{\mathrm{LOADLBDS}}$ signal through the gate at B1 if the latched level of MIR28' is low. The trailing edge of $\overline{\mathrm{LOADLBDS}}$ clocks the AB00 through AB15 outputs from the AB register into the lower bounds register at C4, E4, and F4. If the latched level of MIR28' is high, GATELBDS/ through the gate at B6 sets the ECC status flip-flop at A5. The output of this flip-flop, $\overline{\mathrm{ENABLE\ LOCAL\ ECC\ STATUS}}$, selects ECC status information at the CPU read data multiplexer (see below).

Control line GATEUBDS/ produces the $\overline{\mathrm{LOADUBDS}}$ signal through the gate at B4 if the latched levels of both MIR28' and MIR29' are low. The trailing edge of $\overline{\mathrm{LOADUBDS}}$ clocks the AB00 through AB15 data from the AB register into the upper bounds register at C2, E2, and F2. If MIR29' is high, the GATEUBDS/ signal through the gate at B3 clocks the two-bit address mode register at A2 to the latched levels of MIR30' and MIR31'. MIR30' determines the condition of the AMR0 register, which selects page mode operation; MIR31' determines the condition of the AMR1 register, which selects the upper or lower half of the memory page file.

If the latched level of MIR18' is high, then the GATEUBDS/ signal sets the enable memory page file flip-flop at A3 true through the gate at B1. When this flip-flop is set, the line EMPF is true, directing the address and control interface to interpret a subsequent write request from the CPU as a command to write a page address to the memory page file. The EMPF line also enables memory page file status signals to the CPU read data multiplexer, and enables AB05 as the most significant memory page file address bit.

Control line GATEAB/ has the primary purpose of loading the AB register, but also resets the enable memory page file flip-flop and the ECC status flip-flop. The resetting of the ECC flip-flop clears the SEC status flip-flop.

MEMORY PAGE FILE (MPF)

The memory page file is a 64 word by 9 bit random access memory at location CD6. The inputs to the memory page file are the nine least significant bits of the AB register, $\overline{\mathrm{AB07}}$ through $\overline{\mathrm{AB15}}$ (LSB). The outputs are the lines MPF00 through MPF08. The least significant four bits of the five-bit memory page file address are AB00 through AB04. The most significant bit is supplied by the AMR1 register under normal memory read/write operation, or by AB05 when the enable memory page file flip-flop is set during a load or read memory page file condition.

The memory page file write mode (load MPF) is selected when the WRT-MPF/ signal from the address and control interface is received at T3 (memory) time during a write cycle (T4 with ECC), and when the enable MPF flip-flop is set, through the gate at B1 ($\overline{\mathrm{WRITE\ MPF}}$).

If the read-only page bit MPF07 is true, AMR0 is set (page mode), and the enable memory page file flip-flop is not set, the signal RDOPAGE/ to the address and control interface is brought low through the gate at B3 to inhibit a write operation. If a write operation is attempted, the WRT-MPF/ signal sets the read-only page error flip-flop at A5 through the gate at B1, which sets the interrupt line ROPINT/ true to the CPU. This flip-flop stays set until it is cleared by a GATEAB/ signal following a read memory page file status.

CPU ADDRESS MULTIPLEXER

The seven-bit multiplexer at C5 and F5 selects the source for the most significant six bits of the CPU memory address plus the bank select bit, CPUMAB12/ through CPUMAB17/ and CPUMAB18/. If the AMR0 register is clear (absolute mode), CPUMAB12/ through CPUMAB16/ are sourced from AB05 through AB00, respectively, and CPUMAB17/ and CPUMAB18/ are false, restricting the memory address to the first 65K of the local bank. If the AMR0 register is set (page mode), CPUMAB12/ through CPUMAB18/ are sourced from MPF00 through MPF06, respectively. The least significant 11 bits of the CPU memory address are stored on the address and control interface.

BOUNDS COMPARATORS

The bounds comparison is made by two sets of four 4-bit comparators connected in cascade. The lower bounds comparator at C3, D3, E3, and F3 compares the outputs of the lower bounds register with the AB00 through AB15 lines. If the binary number formed by the ABxx terms is greater than the lower bounds register value, the comparator output ABOVE LOWER

BOUNDS is true. The upper bounds comparator at C1, D1, E1, and F1 operates in an identical fashion, and if the ABxx terms have a lower value than the upper bounds register, the comparator output BELOW UPPER BOUNDS is true. When both comparator outputs are true, the line CPUNBNDS/ goes true through the gate K1, indicating that the CPU 16-bit address ABxx is within the unprotected bounds area of memory.

When operating in the 15-bit addressing mode (MULTIND/ low) the most significant bit of the AB register (AB00) and both bounds registers are forced false by the gates at D2. This mode restricts addressing (in absolute mode) to the first 32K of memory and forces the unprotected area within that range.

CPU WRITE DATA INPUT

On a local bank memory cycle the data on lines S300/ through S315/ (LSB) are strobed into the CPU write data register (D8, F8, and parts of A12 and G8) by the LOAD WRITE DATA signal, which is the complement of the STCP/EXD/ signal from the address and control interface. The latched outputs $\overline{\text{CPU00}}$ through $\overline{\text{CPU15}}$ (LSB) feed the write data multiplexer.

On an external bank CPU memory request the lines S300/ through S315/ are gated to the external bank write data output lines XO01 through XO16. The ENCPWRTDO/ signal from the address and control interface enables the CPU external write data output three-state drivers at D9, E9 and F9.

DMA WRITE DATA INPUT

On a local bank memory cycle the data on the lines DMAD01/ through DMAD16/ are strobed into the DMA write data register (G8, G11, and FG12) by the LOAD WRITE DATA signal. The latched outputs $\overline{\text{LDMA01}}$ through $\overline{\text{LDMA16}}$ feed the write data multiplexer.

On an external bank DMA memory request the lines DMAD01/ through DMAD16/ are gated to the external bank write data output lines XO01 through XO16. The ENDMWRTDO/ signal from the address and control interface enables the DMA external write data output three-state drivers at D12, E12, and F12.

EXTERNAL WRITE DATA INPUT

On a local bank memory cycle the data on the external write data input/read data output lines XI01 through XI16 are strobed into the external write data register (A12, B12, and C12) by the LOAD WRITE DATA signal. The latched outputs XWD01 through XWD16 feed the write data multiplexer.

LOCAL WRITE DATA MULTIPLEXER AND ENABLE CIRCUITS

The write data multiplexer consists of four 8-bit three-state drivers feeding the lines MD00 through MD07 (least significant eight bits) to the MOS memory, plus another four 8-bit three-state drivers feeding the lines MD08 through MD15. The independent control is required on the upper and lower half of the write data word for character write operation.

The drivers are selected by the lines CHR-0/, CHR-1/, EXTREQACT/, and DMAREQACT/ from the address and control interface, through the logic gates at K2, J13, K13, and L13. See table 5-2 for the truth table, enable lines and driver locations. Data is enabled to the MDxx lines when ENMOSWRTD/ is low.

PROTECT BIT MULTIPLEXER

The source of the protect bit to be written into memory during a write cycle is determined by the lines WRT-PB/, EXTREQACT/, and DMAREQACT/ from the address and control interface. The gates at K13 produce the select lines PBMUXA and PBMUXB to the four-input multiplexer J4, according to the truth table shown in table 5-2.

When the WRT-PB/ line is true, due to a true write protect bit line from the requesting port, the protect bit source is from bit 10 (on a scale of 01 through 16, with 01 LSB) of the latched write data. When WRT-PB/ is false, the source is LSECMPB, or the latched protect bit from the read portion of the cycle, and thus the protect bit is restored. The output of the protect bit multiplexer is enabled to the MPROT line to the memory arrays by the $\overline{\text{EPROT/PAR}}$ signal, which is coincident with the ENMOSWRTD/ signal from the address and control interface.

TABLE 5-2. WRITE DATA MULTIPLEXER ENABLES LINES

CHR-0/	EXTREQACT/	DMAREQACT/	Enable Line		Source	Driver Location
Upper half select (MD08 - MD15)						
H	X	X	ESECU		LSEC08 - LSEC15	K10, K11
L	H	H	ECPUU		CPU00 (MSB) - CPU07	J10, J11
L	H	L	EDMAU		LDMA09 - LDMA16	G10, G12
L	L	H	EXU		XWD09 - XWD16	H10, H12
CHR-1/	**EXTREQACT/**	**DMAREQACT/**	**Enable Line**		**Source**	**Driver Location**
Lower half select (MD00 - MD07)						
H	X	X	ESECL		LSEC00 - LSEC07	J9, K10
L	H	H	ECPUL		CPU08 - CPU15 (LSB)	D9, G9, J10
L	H	L	EDMAL		LDMA01 - LDMA08	G9, G10
L	L	H	EXL		XWD01 - XWD08	H9, H10
			Enable Lines			
WRT-PB/	**EXTREQACT/**	**DMAREQACT/**	**PBMUXA**	**PBMUXB**	**Source**	
Protect bit select (MPROT)						
H	X	X	H	H	LSECMPB	
L	H	H	L	L	CPU06	
L	H	L	H	L	LDMA10	
L	L	H	L	H	XWD10	

When the ENPRTSYS line is false, the output of the multiplexer is disabled and a pull-up resistor forces the line high; thus the protect bit is set true on every write cycle regardless of the source.

PARITY GENERATOR/DETECTOR

Parity generators L10 and M10 receive the 16-bit memory data inputs MDxx, whether incoming write data from the requesting port or read data from the arrays. If the number of 1 bits is even, the output (WORD PARITY) is true.

On the trailing edge of the timing input T0-MEM/ from the address and control interface, the flip-flop at A3 is clocked to the level of WORD PARITY. The WT-MPL output then represents the word parity of the incoming write data, and is available to the data output ports as a word parity status line.

As read data appears on the MDxx lines, the L10 and M10 parity generators again produce a WORD PARITY level for this data. This read word parity signal is combined with the read protect bit from MPROT, the read parity bit from MPAR, and the five read ECC check bits from ECC00 through ECC04 in the parity generator at M5. An odd parity from these eight inputs indicates that parity is OK if ECC is not installed (ECC00 through ECC04 are all high); an even parity output indicates a parity error, and the error flag MPE+DED/ to the address and control interface is brought low through gate K3. If ECC is installed, an even parity output from M5 indicates no error if all the syndrome bits are zero (see the paragraphs below); or a double error if one or more syndrome bits are nonzero, in which case the error flag MPE+DED/ is set low through the gate at K3.

An odd parity output from M5 with ECC installed indicates a single bit error, and the odd parity output line SEC is strobed into the register at H8 by the STBDFM/ signal. The latched output, LSEC, allows the SEC status flip-flop at L2 to be clocked low by the next STBDFM/ signal, bringing the SEC STATUS/ line low to the CPU. This flip-flop remains low until the completion of a read ECC status operation, where it is reset by the second flip-flop at L2 on the trailing edge of the ECC signal.

The outputs from M5 are disabled during a local refresh cycle or MPF status operation through the gates at K1.

As the ENMOSWRTD/ line returns low during the write portion of a write cycle, WORD PARITY is again generated from the write data now on the MDxx lines. This level is then combined with the protect bit (MPROT) and the five ECC check bits K0 through K4 in parity generator L4 to generate an overall odd parity among the 18 bits (23 bits with ECC) in the memory word. The output of L4 is then enabled to the MPAR line by the $\overline{\text{EPROT/PAR}}$ signal for writing into memory.

ECC ENCODING AND DECODING

When an ECC array is installed, the line ECCHERE/ is low, due to connections on the ECC array board.

The five ECC check bits are generated by five parity generators. According to the error correcting code scheme outlined under Error Checking and Correction, the parity inputs and outputs are as follows:

Parity Gen.	Output Line	Inputs
L8	K0 (LSB)	MD00, 01, 03, 04, 06, 08, 10, 11, 13, 15 (10)
M8	K1	MD00, 02, 03, 05, 06, 09, 10, 12, 13; MPROT (10)
L9	K2	MD01, 02, 03, 07, 08, 09, 10, 14, 15; MPROT (10)
M11	K3	MD04, 05, 06, 07, 08, 09, 10 (7)
L11	K4	MD11, 12, 13, 14, 15; MPROT (6)

Outputs K0 through K4 are high if their respective memory data inputs have an odd number of high levels; low, for an even number.

During a local read cycle or read portion of a write cycle, the generated ECC data, K0 through K4, is compared with the ECC00 through ECC04 inputs read from the ECC array by the exclusive-OR gates at K4 and part of J7. The results appear at theoutputs SB00 through SB04, called the syndrome bits. If the syndrome bits are all zero, no error is detected; if the syndrome bits are nonzero, their binary value specifies the single bit position that is in error. They are decoded by the binary decoders at J5, K5, and L5, and the decoded output lines BPxx correspond to the bit position discussed under Error Checking and Correction.

The BPxx lines representing memory data bit positions feed the error correction circuits for all data read from the local MOS memory. Bit position errors representing ECC check bits require no correction.

During the write portion of a write cycle, the generated ECC data K0 through K4 is enabled to the ECC00 through ECC04 lines to the ECC array by the $\overline{\text{ENABLE ECC}}$ line, which is synchronous to the ENMOSWRTD/ signal when an ECC option is installed.

ERROR CORRECTION CIRCUITS

Data on the bidirectional MOS memory data lines MD00 through MD15 and MPROT are inverted and each is applied to one input of an exclusive-OR gate contained in circuits L6, K6, M6, J6, and part of J7.

The error correction signals $\overline{\text{BPxx}}$ are applied to the remaining inputs of the exclusive-OR gates. If one of these inputs is low, the complement of the MDxx input signal appears at the output SECxx. The error correcting signals are applied as follows:

Input/Output	Error Correction Signal
MD00/SEC00	$\overline{\text{BP03}}$
MD01/SEC01	$\overline{\text{BP05}}$
MD02/SEC02	$\overline{\text{BP06}}$
MD03/SEC03	$\overline{\text{BP07}}$
MD04/SEC04	$\overline{\text{BP09}}$
MD05/SEC05	$\overline{\text{BP10}}$
MD06/SEC06	$\overline{\text{BP11}}$
MD07/SEC07	$\overline{\text{BP12}}$

MD08/SEC08	$\overline{\text{BP13}}$
MD09/SEC09	$\overline{\text{BP14}}$
MD10/SEC10	$\overline{\text{BP15}}$
MD11/SEC11	$\overline{\text{BP17}}$
MD12/SEC12	$\overline{\text{BP18}}$
MD13/SEC13	$\overline{\text{BP19}}$
MD14/SEC14	$\overline{\text{BP20}}$
MD15/SEC15	$\overline{\text{BP21}}$
MPROT/SECMPB	$\overline{\text{BP22}}$

Single error corrected outputs SEC00 through SEC15 and SECMPB are the read data outputs that are available to the read data output ports. When an ECC option is not installed, these lines contain the same data as the MD00 through MD15 and MPROT lines from the arrays. The SEC lines are also latched by the STBDFM/ signal in the register at H8, J8, and K8. Register outputs are LSEC00 through LSEC15 and LSECMPB, used to restore read data during character write or protect bit write operations, and to restore the protect bit in a normal write cycle.

CPU READ DATA MULTIPLEXER

Four data sources are available to the CPU read data multiplexer: local read data, external bank read data, breakpoint addresses, and local ECC status. The four-input multiplexers are located at G4, G5, G6, H4, H5, H6, and H7. Gates at K3 provide the select inputs to the multiplexers, according to the following truth table:

Select Inputs	Active Select Line	Source
0 0	—	CPU address
0 1	SELCPUEXT/	External read data
1 0	SELCPUINT/	Local read data
1 1	$\overline{\text{ENABLE LOCAL ECC STATUS}}$	ECC status

The multiplexer inputs and outputs are as follows:

Inputs	Outputs
Breakpoint Address (0):	
AB15 - AB00	CPDFM01 - CPDFM16
External read data (1):	
XRD01 - XRD16	CPDFM01 - CPDFM16
Local read data (2):	
SEC00 - SEC15	CPDFM01 - CPDFM16
ECC status (3):	
ECC00 - ECC04	CPDFM01 - CPDFM05
MPAR	CPDFM06
MPROT	CPDFM07
ECCH	CPDFM08
SB00 - SB04	CPDFM09 - CPDFM13
Low (ground)	CPDFM14 - CPDFM15
SEC STATUS	CPDFM16

The outputs of the multiplexer are clocked into the CPU read data register at G3, H3, and J3 by the STBCPUDFM/ signal from the address and control interface. The register output lines, CPUDFM01 through CPUDFM16, provide breakpoint address and instruction information to the CPU via the output pins.

The parity and protect inputs to the CPU read data register are from multiplexer H1. When local read data is selected for the CPU read data multiplexer, the parity bit source is the latched word parity level WT-MPL and the protect bit source is the (corrected) protect bit from the local MOS memory SECMPB. When external read data is selected, the parity and protect bit source is from the external bank (XMPL and XMPB). Note that the CPU protect bit output is forced false if the memory address is in bounds (CPUNBNDS/ low).

CPU OPERAND BUS MULTIPLEXER

Either the CPU read data multiplexer or the memory page file status signals may be enabled onto the CPU operand bus, BUS00 (MSB) through BUS15. The multiplexer inputs are selected as follows:

Inputs	Output
$\overline{\text{ENABLE LOCAL MPF STATUS}}$ false:	
CPUDFM01 - CPUDFM16	BUS15 - BUS00
$\overline{\text{ENABLE LOCAL MPF STATUS}}$ true:	
MPF00 - MPF08	BUS15 - BUS07
Low (ground)	BUS06 - BUS03
PGM FILES (AMR 1)	BUS02
PAGE MODE (AMR 0)	BUS01
READ ONLY PAGE ERROR	BUS00

The three-state multiplexer outputs are enabled onto the BUSxx lines by a low input line ENMEMBUS/ from the CPU.

DMA READ DATA MULTIPLEXER

Local and external read data are available to the DMA devices through the multiplexer at A9, B9, B7, C9, and A6.

If the line $\overline{\text{DMA LOCAL}}$ (DMAREQACT/) is low, the lines SEC00 through SEC15, SECMPB, and WT-MPL from the local bank are selected. If high, the input lines XRD01 through XRD16, XMPB, and XMPL from the external bank are selected. The multiplexer outputs are fed to the output registers at A8, A7, and B8.

The output registers are clocked by the STBDMADFM/ signal and form the outputs DMADFM01 through DMADFM16, DMAMPB/, and DMAMPL/.

MEMORY ARRAY CIRCUITS

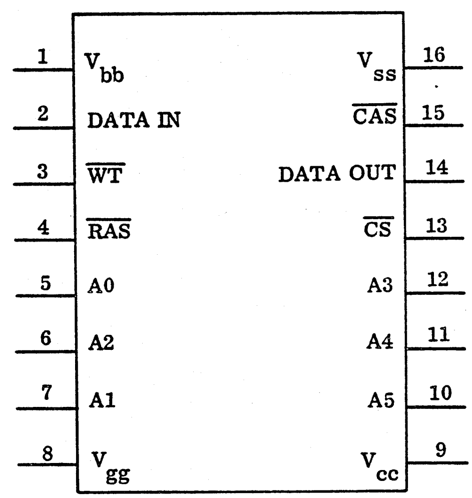
MEMORY CHIP

The memory circuit used in the array is a MOS memory organized as 4096 words by one bit. Each chip contains a six-bit address input, shared to provide row and column addresses for the 64 by 64 bit arrangement of storage cells within the chip. Each circuit has a single write data input and three-state read data output. Power supply inputs are +12, +5, and -5 vdc.

Each circuit has four control inputs:

- Chip select ($\overline{CS}$) — Usually true in the MOS memory during the time the row address strobe is true. The $\overline{CS}$ line is high during a refresh cycle.
- Row address strobe ($\overline{RAS}$) — Leading (negative-going) edge strobes the six-bit row address into the on-chip row register.
- Column address strobe ($\overline{CAS}$) — Leading (negative-going) edge strobes the six-bit column address into the on-chip column register.
- Write line ($\overline{WT}$) — When true, replaces the previously stored bit addressed with the level on the data input line.

Pin connections for the MOS memory chip are shown in figure 5-10. The inputs A0 through A5 are the address inputs.



V_{gg}: +12V V_{ss}: GROUND

V_{cc}: +5V V_{bb}: -5V

Figure 5-10. Memory Chip Pin Assignments (Top View)

ARRAY ORGANIZATION

Each memory chip represents one bit of an 18-bit by 4096-word memory block; thus 18 chips are used to form a 4K block. Four 4K memory blocks make up a memory section of 16,384 words. The four blocks may comprise an entire card (16K card) or two sections may be on a card (32K card). Each section is selected by one of the eight row address strobes (RAS16Kx-x/) from the address and control interface, and the blocks within each section are selected by one of four block select inputs (SLTBLKx/). Table 5-3 shows the array component location.

The proper row address strobe is selected by positioning the address connector (see figure 5-3).

DATA DRIVERS

Incoming write data from lines MD00 through MD15, MPAR, and MPROT are fed to the inputs of drivers at J9, F9, and C9 on a 16K memory array and on the lower 16K of a 32K memory. The upper 16K drivers of a 32K memory array are located at P9, T9, and W9. Each driver feeds write data to four 4K memory blocks.

Read data from the memory chip outputs is fed to three-state drivers at G9, D9, and A9 on a 16K memory array and on the lower 16K of a 32K memory. The upper 16K read data drivers of a 32K memory are located at S9, V9, and Y9. The outputs are enabled to the MD00 through MD15, MPAR, and MPROT lines to the data interface by the EN16KNx-y/ (E16KN1-x/ for 32K upper half) desired from an E16KNx-x/ line.

TABLE 5-3. MEMORY ARRAY COMPONENT LOCATION

0-16K					16K-32K				
Bit	Blk 0	Blk 1	Blk 2	Blk 3	Bit	Blk 0	Blk 1	Blk 2	Blk 3
0	J4	J3	J8	J7	0	P4	P3	P8	P7
1	J2	J1	J6	J5	1	P2	P1	P6	P5
2	H4	H3	H8	H7	2	R4	R3	R8	R7
3	H2	H1	H6	H5	3	R2	R1	R6	R5
4	G4	G3	G8	G7	4	S4	S3	S8	S7
5	G2	G1	G6	G5	5	S2	S1	S6	S5
6	F4	F3	F8	F7	6	T4	T3	T8	T7
7	F2	F1	F6	F5	7	T2	T1	T6	T5
8	E4	E3	E8	E7	8	U4	U3	U8	U7
9	E2	E1	E6	E5	9	U2	U1	U6	U5
10	D4	D3	D8	D7	10	V4	V3	V8	V7
11	D2	D1	D6	D5	11	V2	V1	V6	V5
12	C4	C3	C8	C7	12	W4	W3	W8	W7
13	C2	C1	C6	C5	13	W2	W1	W6	W5
14	B4	B3	B8	B7	14	X4	X3	X8	X7
15	B2	B1	B6	B5	15	X2	X1	X6	X5
16†	A4	A3	A8	A7	16	Y4	Y3	Y8	Y7
17††	A2	A1	A6	A5	17	Y2	Y1	Y6	Y5

† (MPAR)
†† (MPROT)

ADDRESS DRIVERS

Memory address data from the lines MOSMA00 through MOSMA05 is fed to the inputs of drivers L6 and L8 on a 16K memory array and on the lower half of a 32K memory. The upper 16K drivers of a 32K memory array are located at M6 and M8. Each driver feeds memory address data to two 4K memory blocks.

CONTROL DRIVERS

Control lines from the address and control interface are enabled to the memory circuits by the RAS16Kx-y/ (RAS16K1-x/ for 32K upper half) line through three-state drivers K6 and K8 for a 16K memory or the lower half of a 32K memory and at N6 and N8 for the upper half of a 32K memory. The $\overline{RAS}$ and $\overline{WT}$ drivers each feeds a single 4K memory block; the $\overline{CAS}$ and $\overline{CS}$ drivers each feeds two 4K memory blocks.

Array Input	Chip Input (enabled by RAS16Kx-y)	Function
SLTBLKx/	$\overline{RAS}$	Row address strobe
CAS/	$\overline{CAS}$	Column address strobe
WT-MOS/	$\overline{WT}$	Write enable
CS/	$\overline{CS}$	Chip select

POWER DISTRIBUTION

The +5v bus has been split to minimize the power drain for battery backup operation. Some of the +5v circuits (namely the data paths) can be allowed to lose power whereas others (i.e., clocks and addresses required for refresh) must be maintained to preserve memory contents during power failures. Without battery backup both +5v buses are jumpered and powered from the same supply.

ECC ARRAY CIRCUITS

The ECC array is similar to the MOS memory array, except that it is arranged as 98K by 5 bits. The card includes six 16K memory sections, each containint four 4K memory blocks. Table 5-4 shows memory chip component location.

DATA DRIVERS

Incoming write data from the data interface over the lines ECC00 through ECC04 are fed to the inputs of drivers at D6, H6, M6, R6, V6 and Z6. Each driver feeds write data to four 4K memory blocks.

Read data from the memory chip outputs are fed to three-state drivers at B6, F6, K6, P6, T6 and X6. The outputs are enabled to the ECC00 through ECC04 outputs by the appropriate E16KNx-x/ line from the address and control interface.

ADDRESS DRIVERS

Memory address data from MOSMA00 through MOSMA05 are fed to the inputs of drivers at F7, H7, V7, and X7. Each driver feeds memory address data to six 4K memory blocks.

CONTROL DRIVERS

The $\overline{RAS}$ row address strobe inputs to the memory chips are formed by the SLTBLKx/ inputs as enabled by the RAS16Kx-x/ inputs. The three-state drivers are located at D7, K7, T7, and Z7, and each feeds a single 4K memory block.

The $\overline{CAS}$, $\overline{CS}$, and $\overline{WT}$ drivers are located at M7 and R7. Each feeds six 4K memory blocks.

TABLE 5-4. ECC ARRAY MEMORY COMPONENT LOCATION

Block Select Lines	Bit 0	1	2	3	4
RAS16K0-1					
SLTBLK0	A5	A4	A3	A2	A1
SLTBLK1	B5	B4	B3	B2	B1
SLTBLK2	C5	C4	C3	C2	C1
SLTBLK3	D5	D4	D3	D2	D1
RAS16K1-1					
SLTBLK0	E5	E4	E3	E2	E1
SLTBLK1	F5	F4	F3	F2	F1
SLTBLK2	G5	G4	G3	G2	G1
SLTBLK3	H5	H4	H3	H2	H1
RAS16K0-2					
SLTBLK0	J5	J4	J3	J2	J1
SLTBLK1	K5	K4	K3	K2	K1
SLTBLK2	L5	L4	L3	L2	L1
SLTBLK3	M5	M4	M3	M2	M1
RAS16K1-2					
SLTBLK0	N5	N4	N3	N2	N1
SLTBLK1	P5	P4	P3	P2	P1
SLTBLK2	Q5	Q4	Q3	Q2	Q1
SLTBLK3	R5	R4	R3	R2	R1
RAS16K0-3					
SLTBLK0	S5	S4	S3	S2	S1
SLTBLK1	T5	T4	T3	T2	T1
SLTBLK2	U5	U4	U3	U2	U1
SLTBLK3	V5	V4	V3	V2	V1
RAS16K1-3					
SLTBLK0	W5	W4	W3	W2	W1
SLTBLK1	X5	X4	X3	X2	X1
SLTBLK2	Y5	Y4	Y3	Y2	Y1
SLTBLK3	Z5	Z4	Z3	Z2	Z1

SIGNAL	PIN	CROSS REF NO
BLKAB/	297	0118
CAS/	239	0110
CHAR0	246	0117
CHAR1	269	0108
CHR-0/	289	0108
CHR-1/	290	0105
CH0/PF	89	0114
CH1/PE/	76	0114
CPUMAB12/	268	0108
CPUMAB13/	286	0107
CPUMAB14/	280	0107
CPUMAB15/	293	0107
CPUMAB16/	285	0107
CPUMAB17/	283	0106
CPUMAB18/	17	0113
CPUMDS/	222	0113
CPUNBDS/	45	0117
CPUPRØTECT/	248	0117
CPUREQ/	225	0113
CPUWRITE	49	0117
CPUWRTPB	36	0106
CPU-SC/	272	0105
CS/	237	0107
CPUBKPWRT	266	0105
DMACHAR0	230	0105
DMACHAR1	250	0105
DMAMAB01/	37	0109
DMAMAB02/	253	0109
DMAMAB03/	255	0109
DMAMAB04/	256	0109
DMAMAB05/	263	0108
DMAMAB06/	35	0108
DMAMAB07/	277	0108
DMAMAB08/	52	0108
DMAMAB09/	252	0108
DMAMAB10/	261	0108
DMAMAB11/	262	0108
DMAMAB12/	274	0108
DMAMAB13/	292	0107
DMAMAB14/	281	0107
DMAMAB15/	282	0107

SIGNAL	PIN	CROSS REF NO
DMAMAB16/	271	0107
DMAMAB17/	284	0106
DMAMAE/	18	0113
DMAMDS/	221	0112
DMAMPE/	215	0112
DMAPRØT/	39	0117
DMAREQACT/	296	0104
DMAWRITE	43	0117
DMAWRTPB/	273	0106
DMA1-INT	210	0101
DMA1-MR/	11	0101
DMA1-RA/	227	0101
DMA2-INT	205	0101
DMA2-MR/	214	0101
DMA2-RA/	219	0101
DMA3-INT	243	0101
DMA3-MR/	212	0101
DMA3-RA/	220	0101
DMA4-INT	211	0101
DMA4-MR/	213	0101
DMA4-RA/	216	0101
DMA-PF/	228	0112
DMA-SC/	270	0105
ECCHERE/	34	0112
EMPF	47	0117
ENCPWRTDØ/	299	0118
ENDMWRTDØ/	298	0118
ENEXTRDØ/	46	0114
ENMØSWRTD/	217	0112
ENMØS-250	42	0111
ENPRTSYS	247	0105
EXTBANK/	99	0113
EXTIMAB01/	65	0109
EXTIMAB02/	66	0109
EXTIMAB03/	67	0109
EXTIMAB04/	68	0109
EXTIMAB05/	69	0108
EXTIMAB06/	70	0108
EXTIMAB07/	71	0108
EXTIMAB08/	72	0108
EXTIMAB09/	73	0108

SIGNAL	PIN	CROSS REF NO
EXTIMAB10/	74	0108
EXTIMAB11/	75	0108
EXTIMAB12/	90	0108
EXTIMAB13/	91	0107
EXTIMAB14/	93	0107
EXTIMAB15/	94	0107
EXTIMAB16/	95	0107
EXTIMAB17/	96	0106
EXTØMAB01/	53	0116
EXTØMAB02/	54	0116
EXTØMAB03/	55	0116
EXTØMAB04/	56	0116
EXTØMAB05/	57	0116
EXTØMAB06/	58	0116
EXTØMAB07/	59	0116
EXTØMAB08/	60	0116
EXTØMAB09/	61	0116
EXTØMAB10/	62	0116
EXTØMAB11/	63	0116
EXTØMAB12/	78	0115
EXTØMAB13/	79	0115
EXTØMAB14/	81	0115
EXTØMAB15/	82	0115
EXTØMAB16/	83	0115
EXTØMAB17/	84	0115
EXTREQACT/	295	0104
EXTREQIN/	92	0103
EXTREQØUT/	80	0114
EXTRESIN/	100	0118
EXTRESØUT/	88	0114
EXTWPBIN	97	0106
EXTWPBØUT	85	0117
EXTWRTIN	98	0106
EXTWRTØUT	86	0117
E16KN0-1/	208	0106
E16KN0-2/	207	0106
E16KN0-3/	206	0106
E16KN0-4/	209	0106
E16KN1-1/	226	0106
E16KN1-2/	26	0106
E16KN1-3/	25	0106
E16KN1-4/	27	0106

SIGNAL	PIN	CROSS REF NO
GATEAB/	294	0116
GND	4	0117
GND	101	0117
GND	102	0117
GND	204	0117
GND	234	0117
GND	245	0117
GND	251	0117
GND	254	0117
GND	301	0117
GND	302	0117
GND	87	0117
MCTM/	279	0102
MC/	51	0111
MØSMA00	258	0109
MØSMA01	257	0109
MØSMA02	260	0109
MØSMA03	259	0109
MØSMA04	265	0109
MØSMA05	264	0109
MPB-L	20	0105
MPB/PRF	240	0117
MPE+DED/	21	0113
MP /SC	44	0117
PE//CH1	64	0117
PF/CH0	77	0117
PØWERFAIL/	48	0110
PRF/MPB	288	0105
PRIØRITY	218	0101
RAS16K0-1/	236	0106
RAS16K0-2/	32	0106
RAS16K0-3/	33	0106
RAS16K0-4/	232	0106
RAS16K1-1/	244	0106
RAS16K1-2/	30	0106
RAS16K1-3/	233	0106
RAS16K1-4/	31	0106
RDØPAGE/	249	0117

SIGNAL	PIN	CROSS REF NO
SC/MPL	287	0105
SELCPUEXT/	6	0111
SELCPUINT/	223	0111
SETSM105/	7	0112
SETSM108/	14	0112
SLTBLK0/	238	0107
SLTBLK1/	235	0107
SLTBLK2/	241	0107
SLTBLK3/	242	0107
STBCPUBKP/	13	0113
STBCPUDFM/	8	0112
STBDFM/	10	0112
STBDMADFM/	9	0112
STCP/EXD/	224	0110
S305/	41	0116
S306/	40	0116
S307/	38	0116
S308/	23	0116
S309/	28	0116
S310/	24	0116
S311/	22	0116
S312/	29	0116
S313/	12	0116
S314/	15	0116
S315/	5	0116
T0/	50	0114
T0-MEM/	275	0110
T2-ØDDCLK	267	0114
T3-MEM/	19	0114
WRT-MPF/	16	0113
WRT-PB/	291	0106
WT-MØS/	231	0112
+5V	1	0117
+5V	2	0117
+5V	201	0117
+5V	202	0117
+5V BB	3	0117
+5V BB	203	0117

6. 8T98 IS SIMILAR TO 939
5. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S138
4. IC TO BE CONNECTED TO +5VBB
3. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S257
2. NO ELEMENT IDENTIFIER AVAILABLE FOR 100 NS DELAY
1. 8T97 IS SIMILAR TO 939

NOTES UNLESS OTHERWISE SPECIFIED

INACTIVE

INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DR 96752171 DETACHED LIST

LOGIC TITLE

LOGIC DWG NO — REV

PWA NO 96752170 — PWB NO 96754582

CONTROL DATA — SMALL COMPUTER DEVELOPMENT DIVISION

DR B L Johnson 2-3-78

CHK 2-16-78

ENGR 2-24-78

MPI7 MØS MEMØRY I/F
ADDRESS / CØNTRØL

CARD POS

LOGIC TYPE 8GVT

C — CODE IDENT NO 09132 — DRAWING NUMBER 96752171 — REV B

SHEET 1 OF 19

Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 1 of 20)

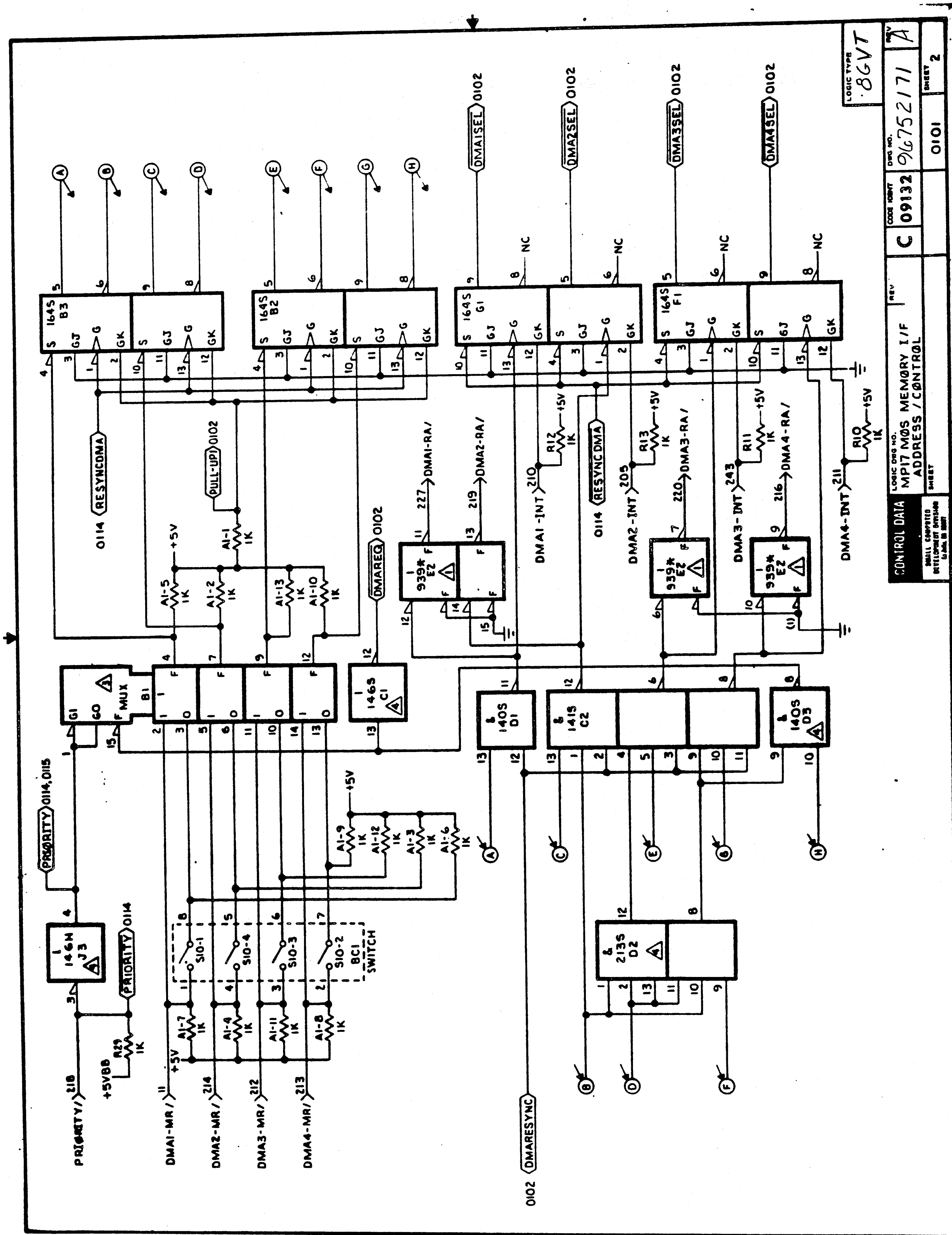


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 2 of 20)

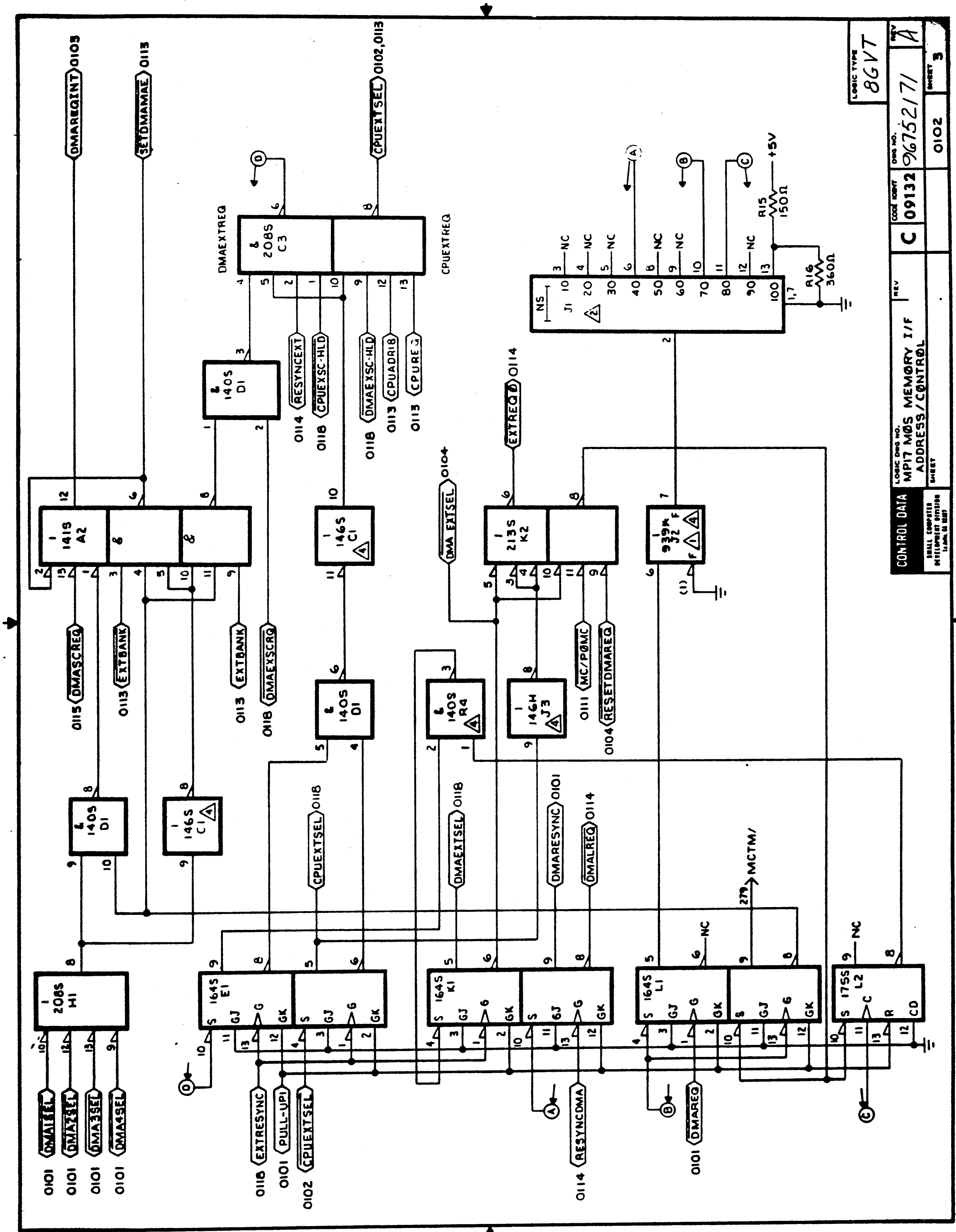


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 3 of 20)

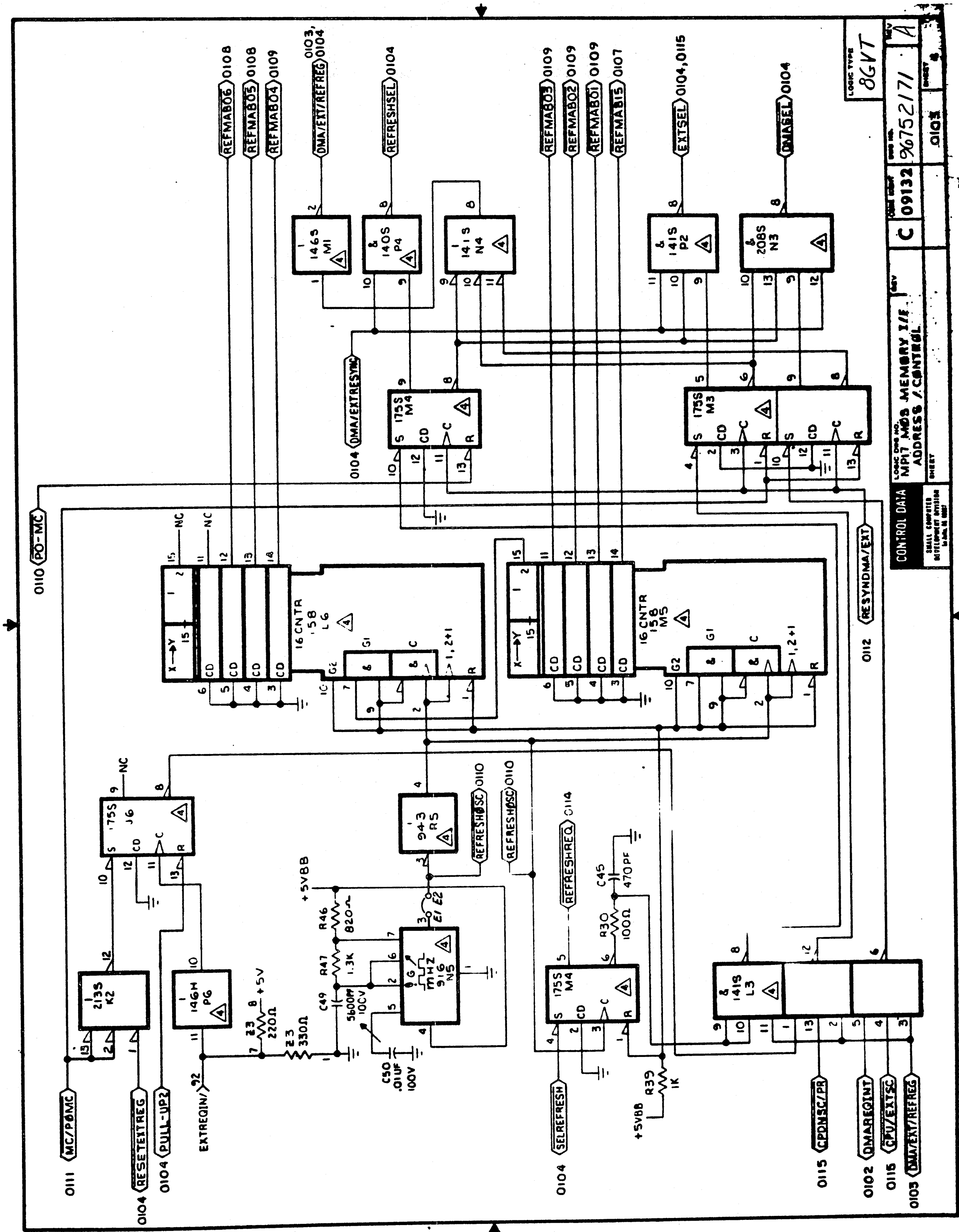


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 4 of 20)

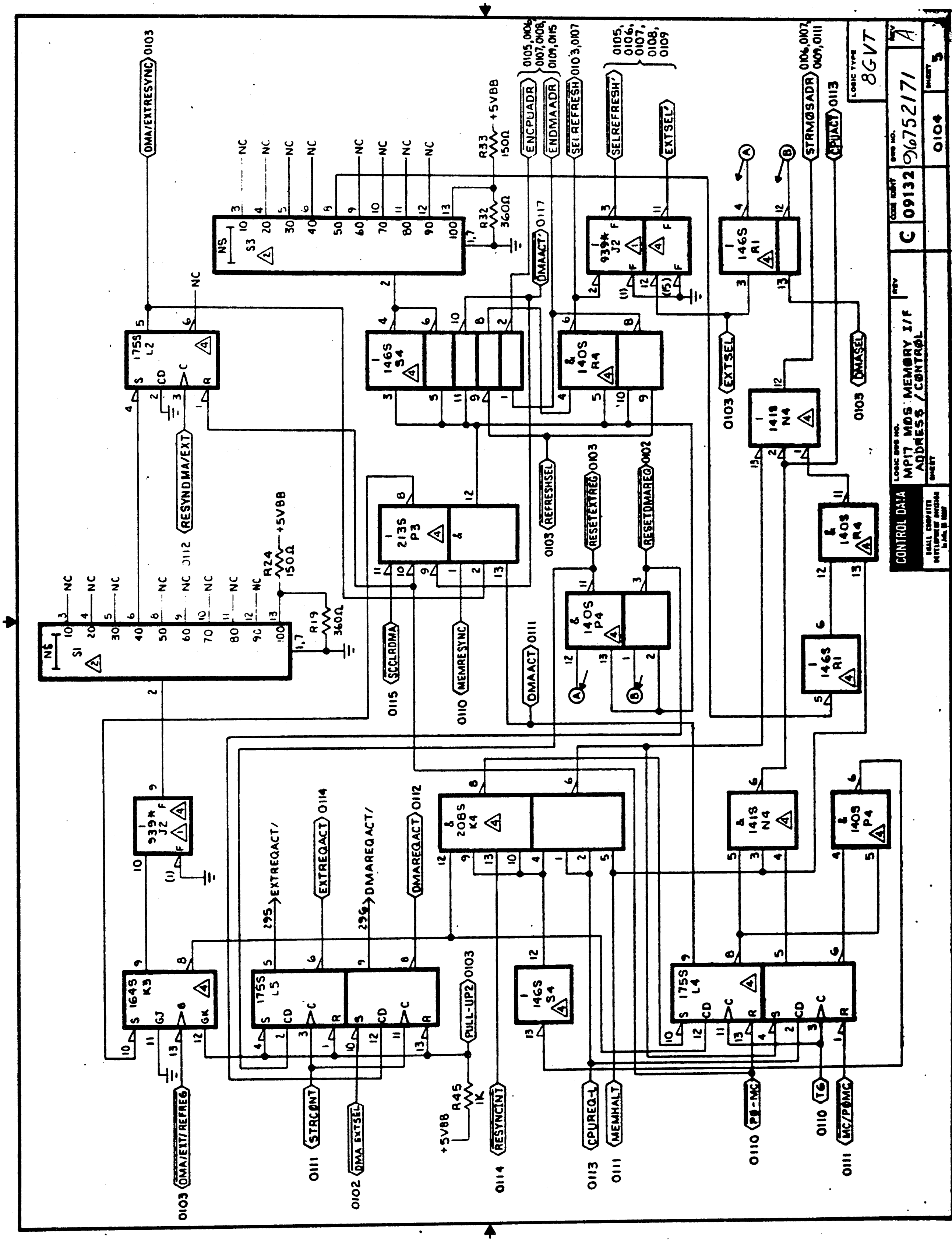


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 5 of 20)

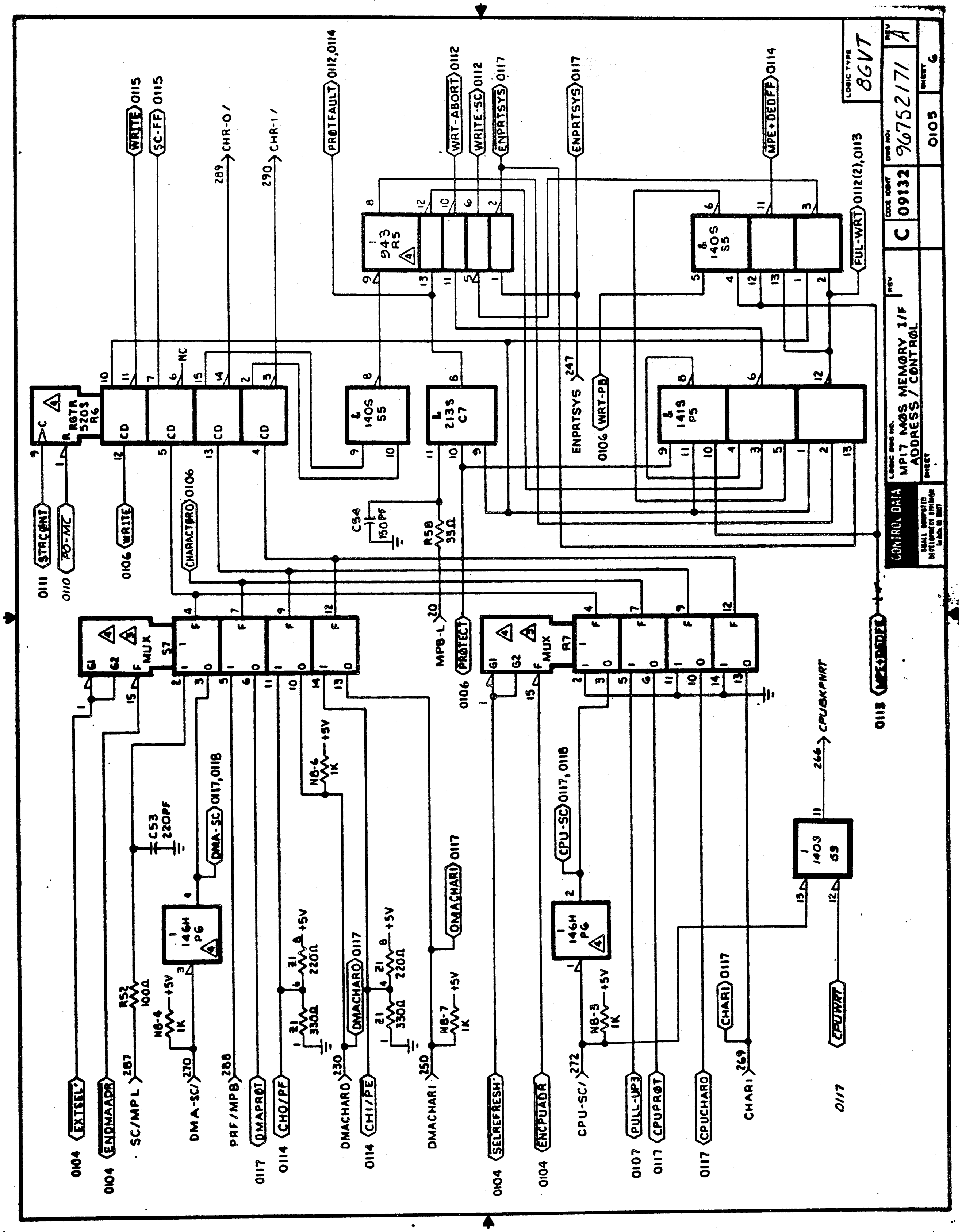


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 6 of 20)

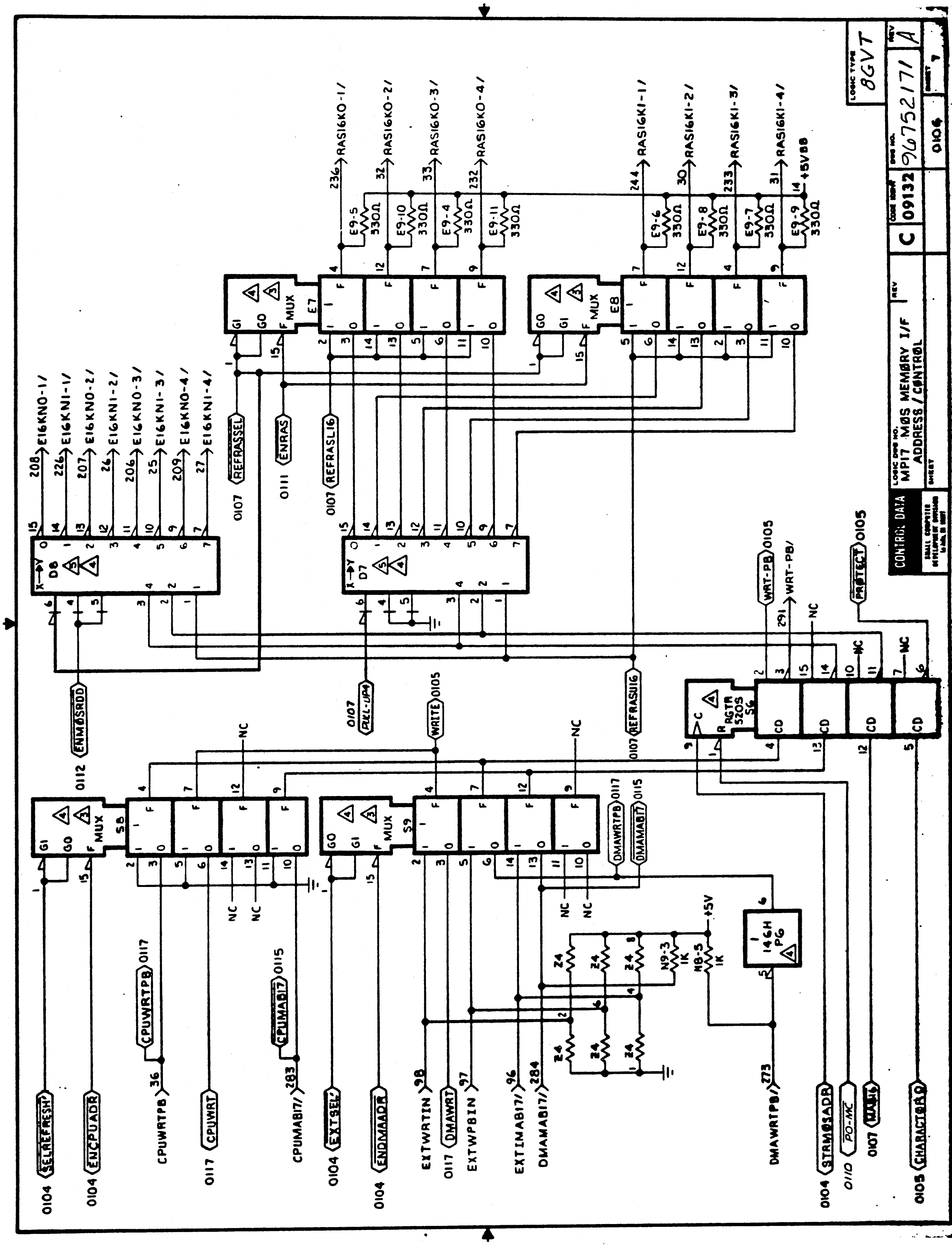


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 7 of 20)

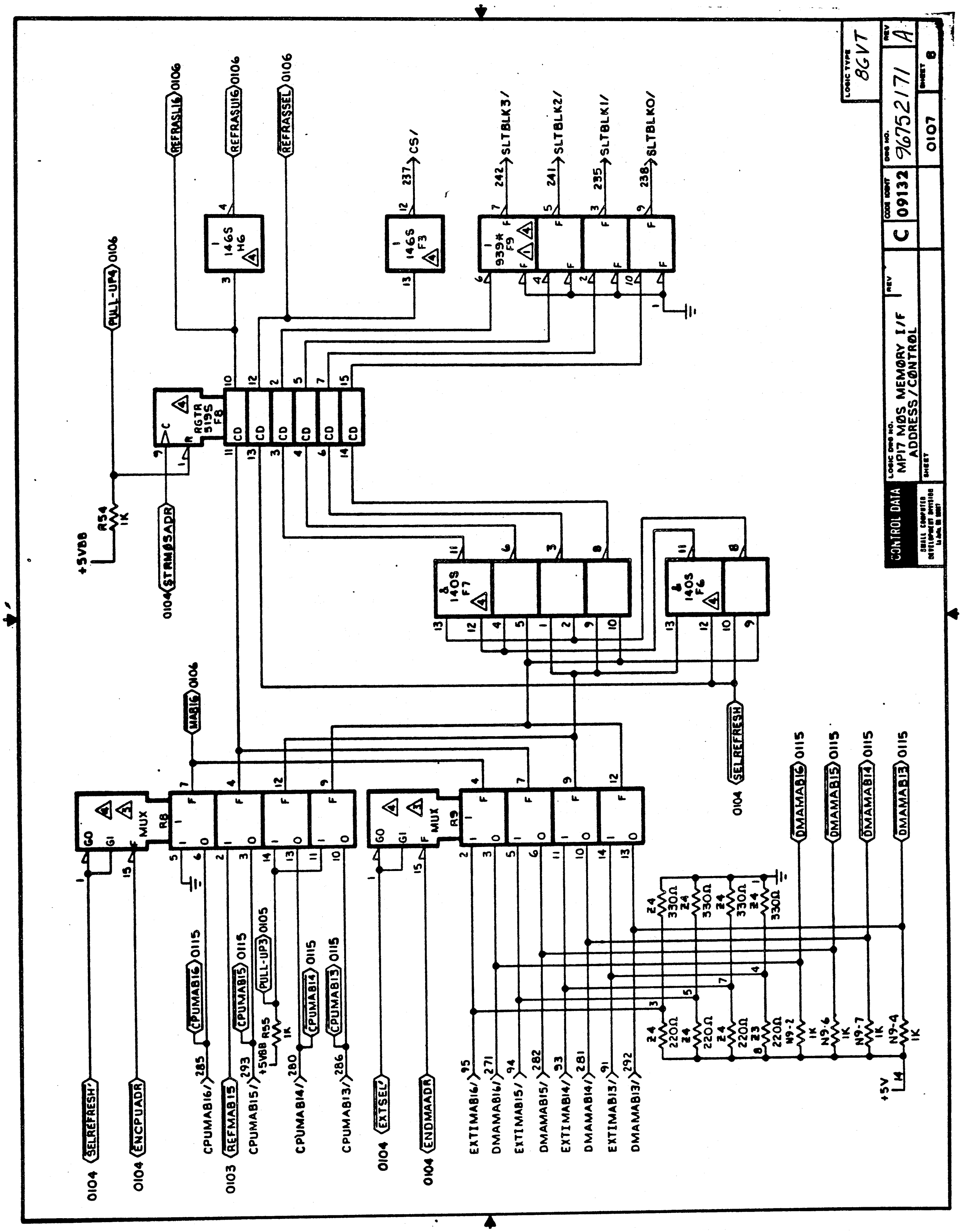


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 8 of 20)

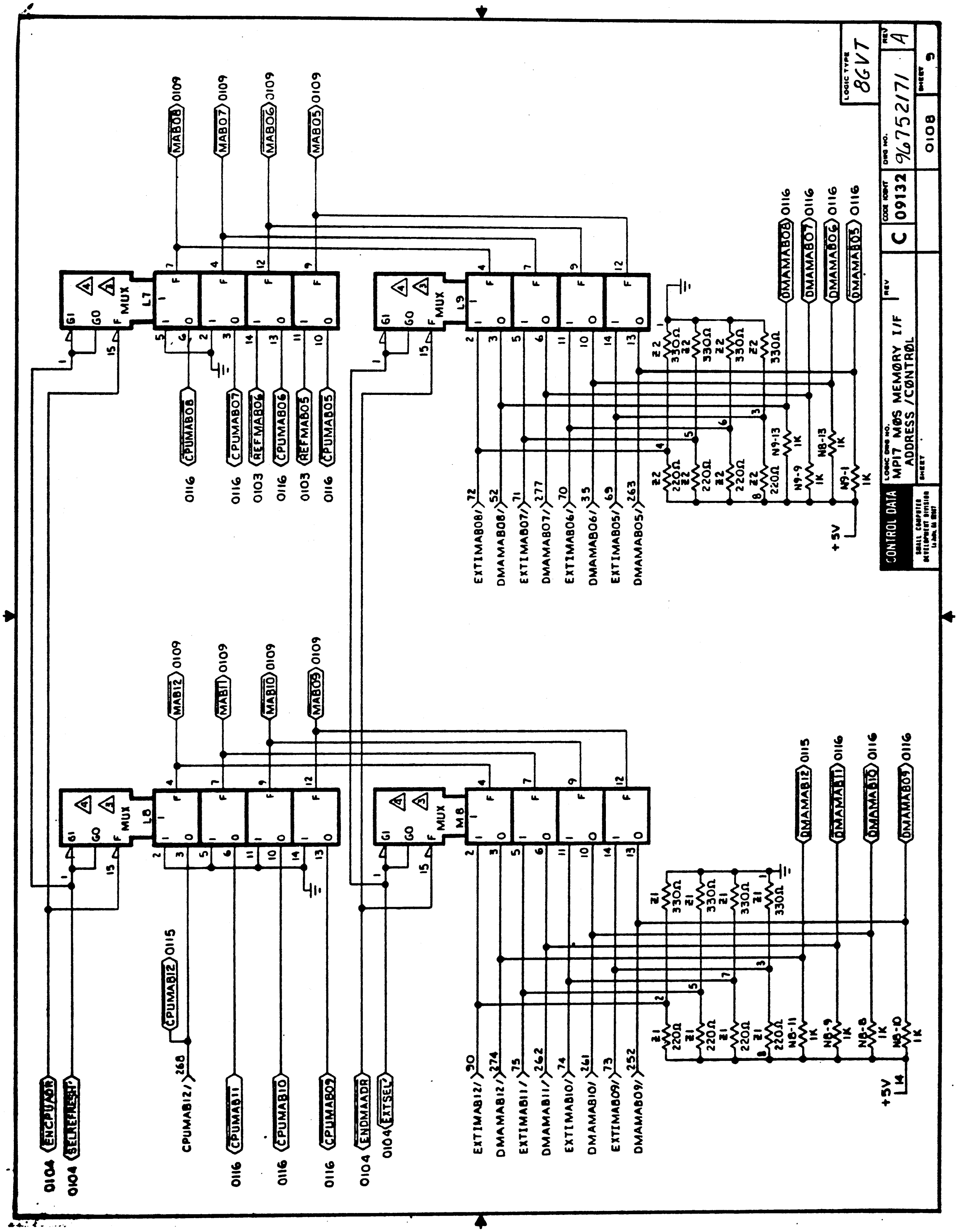


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 9 of 20)

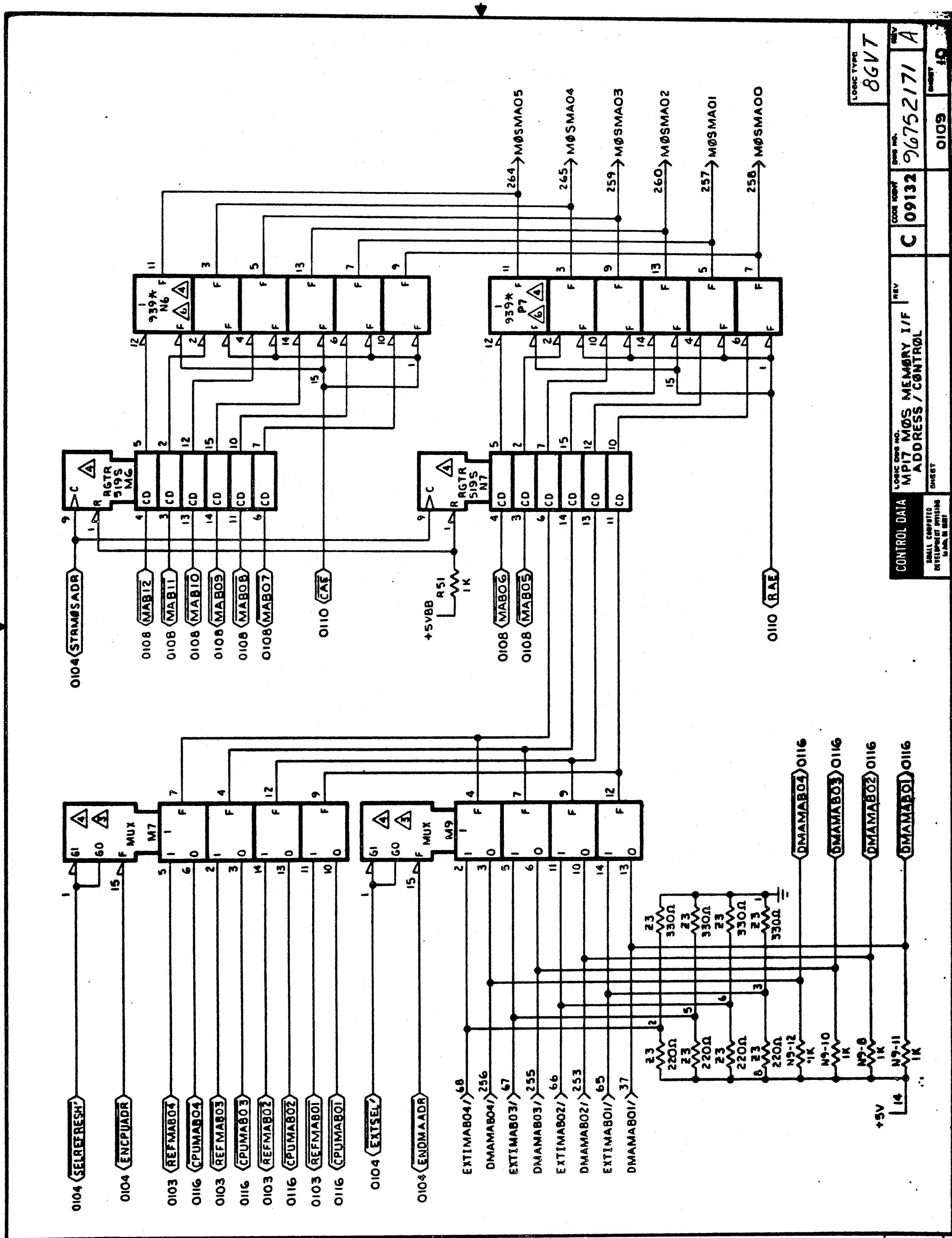


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 10 of 20)

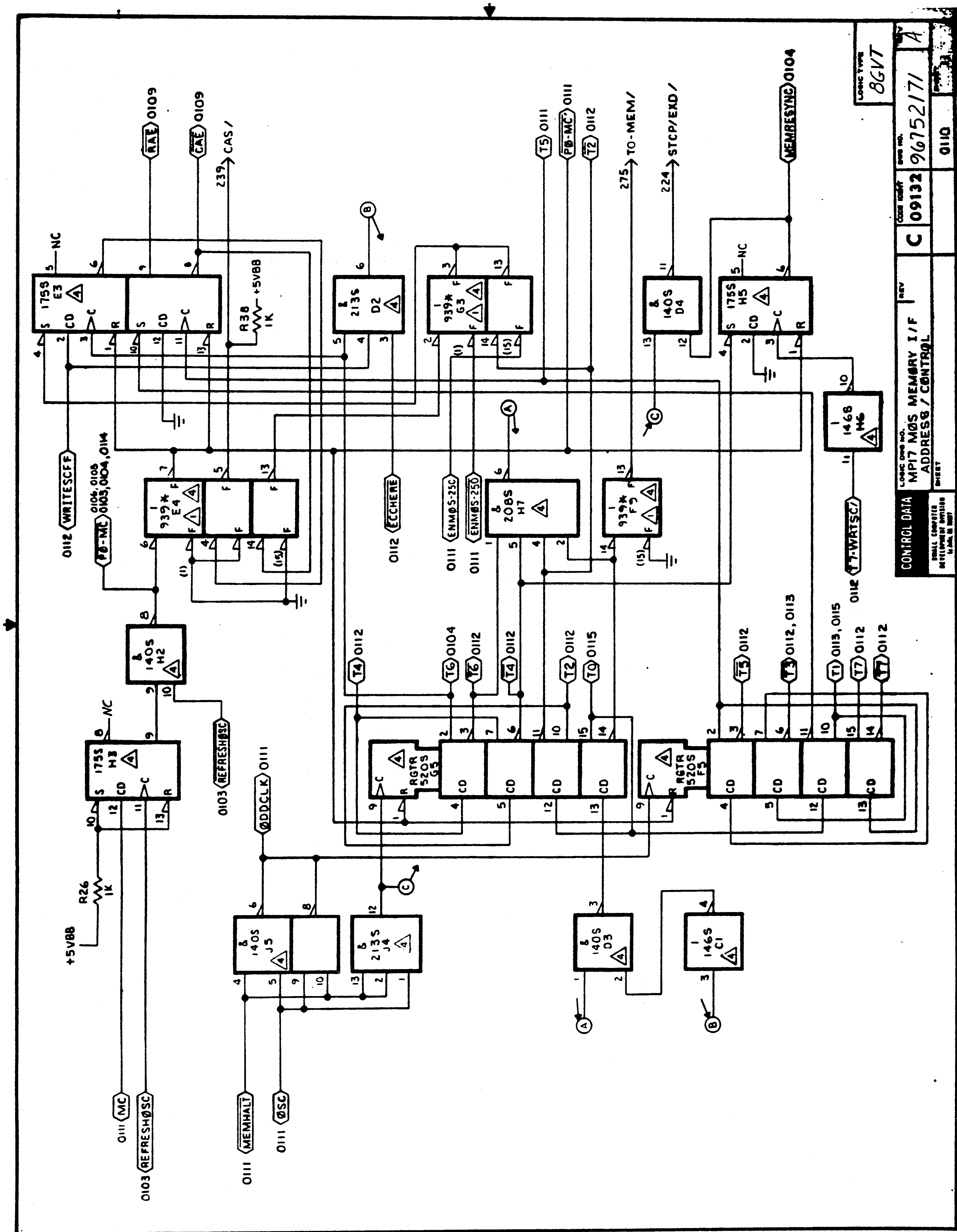


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 11 of 20)

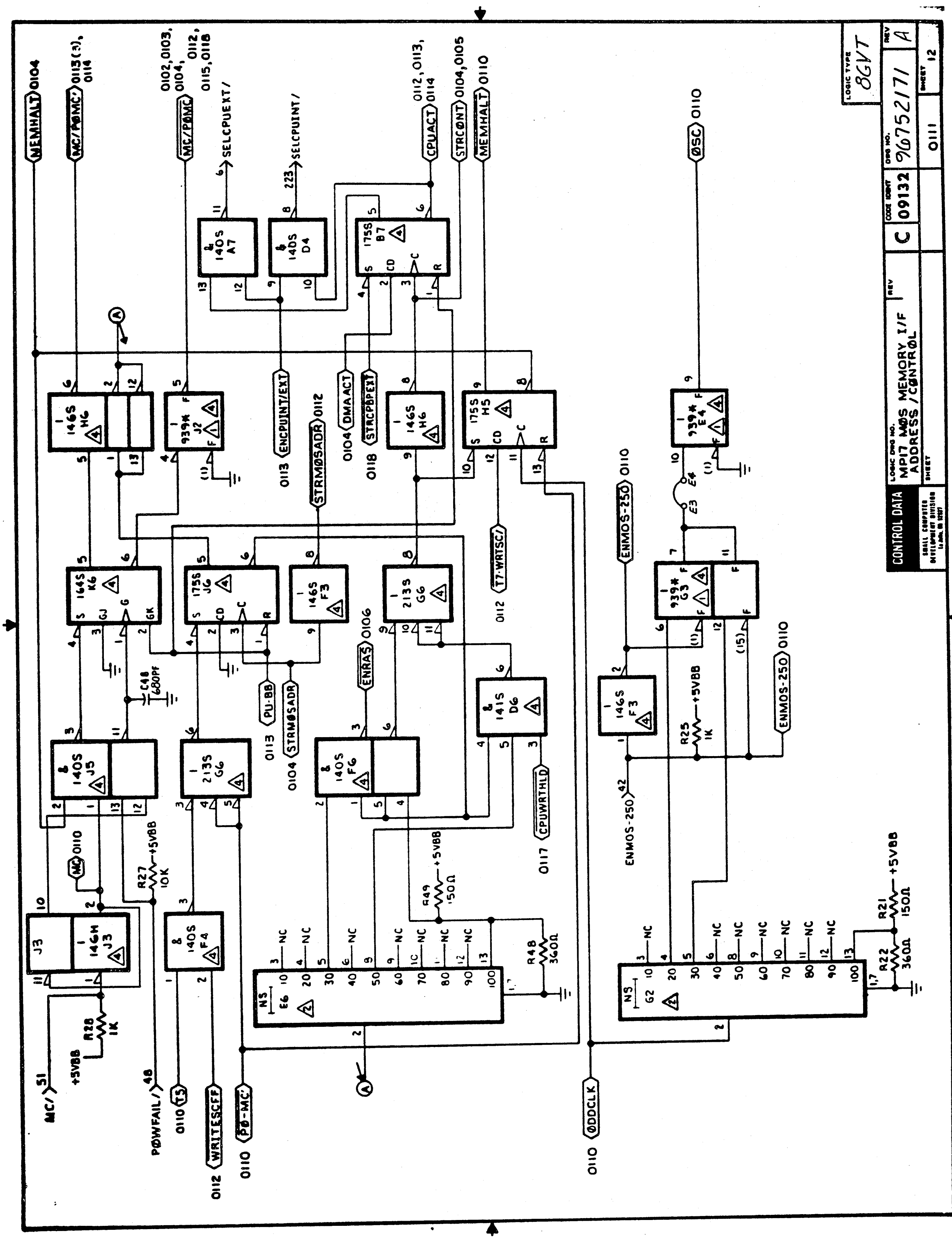


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 12 of 20)

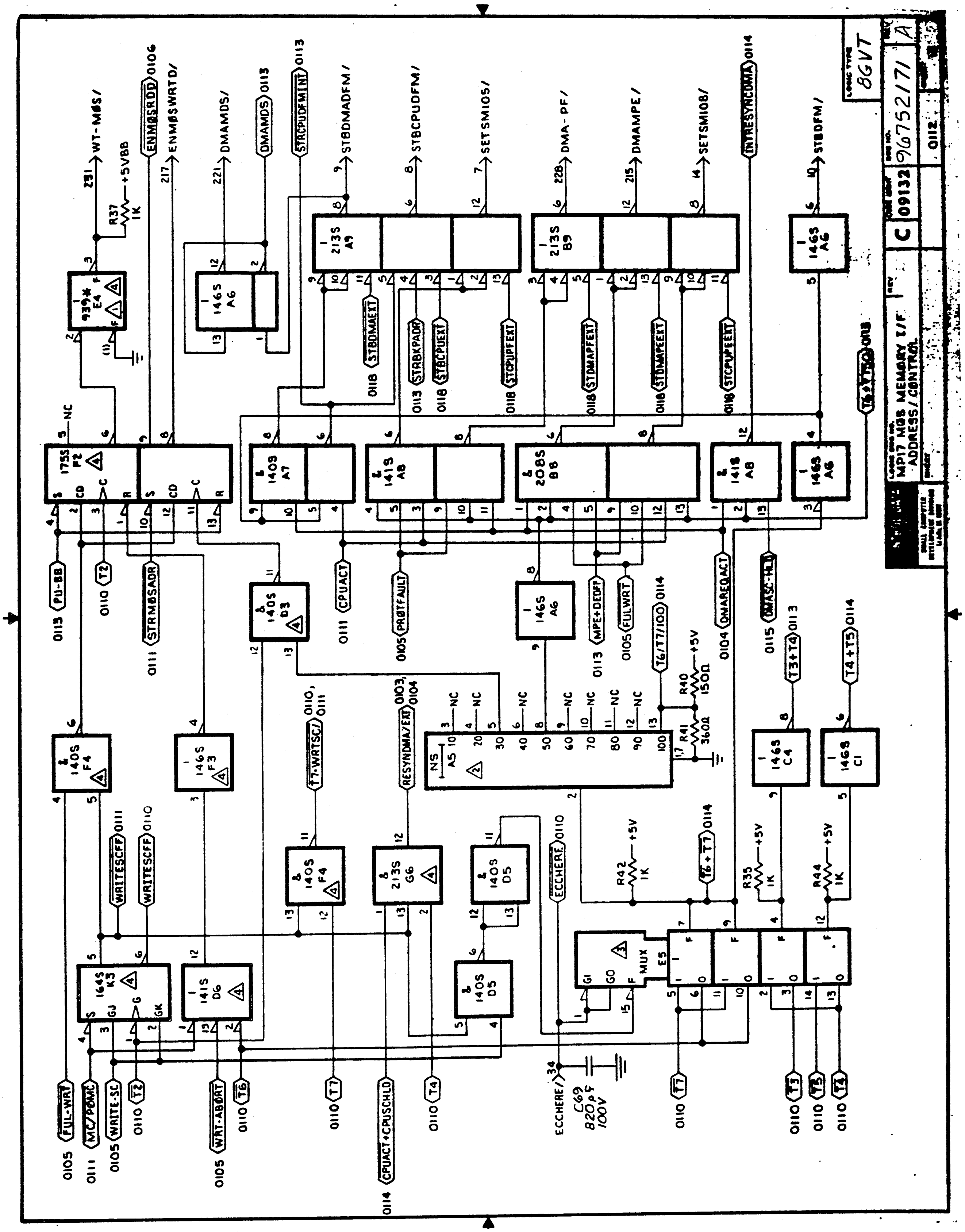


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 13 of 20)

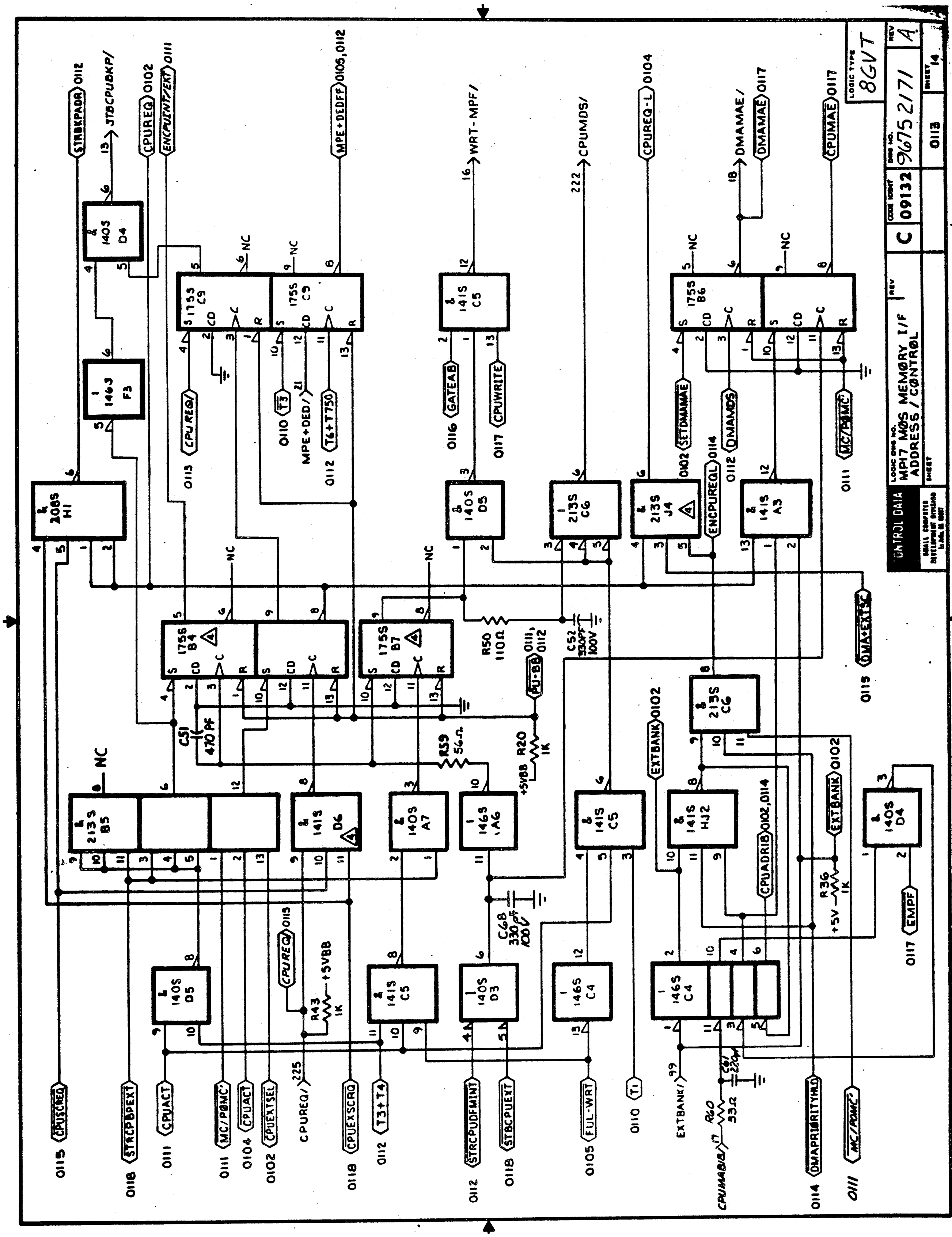


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 14 of 20)

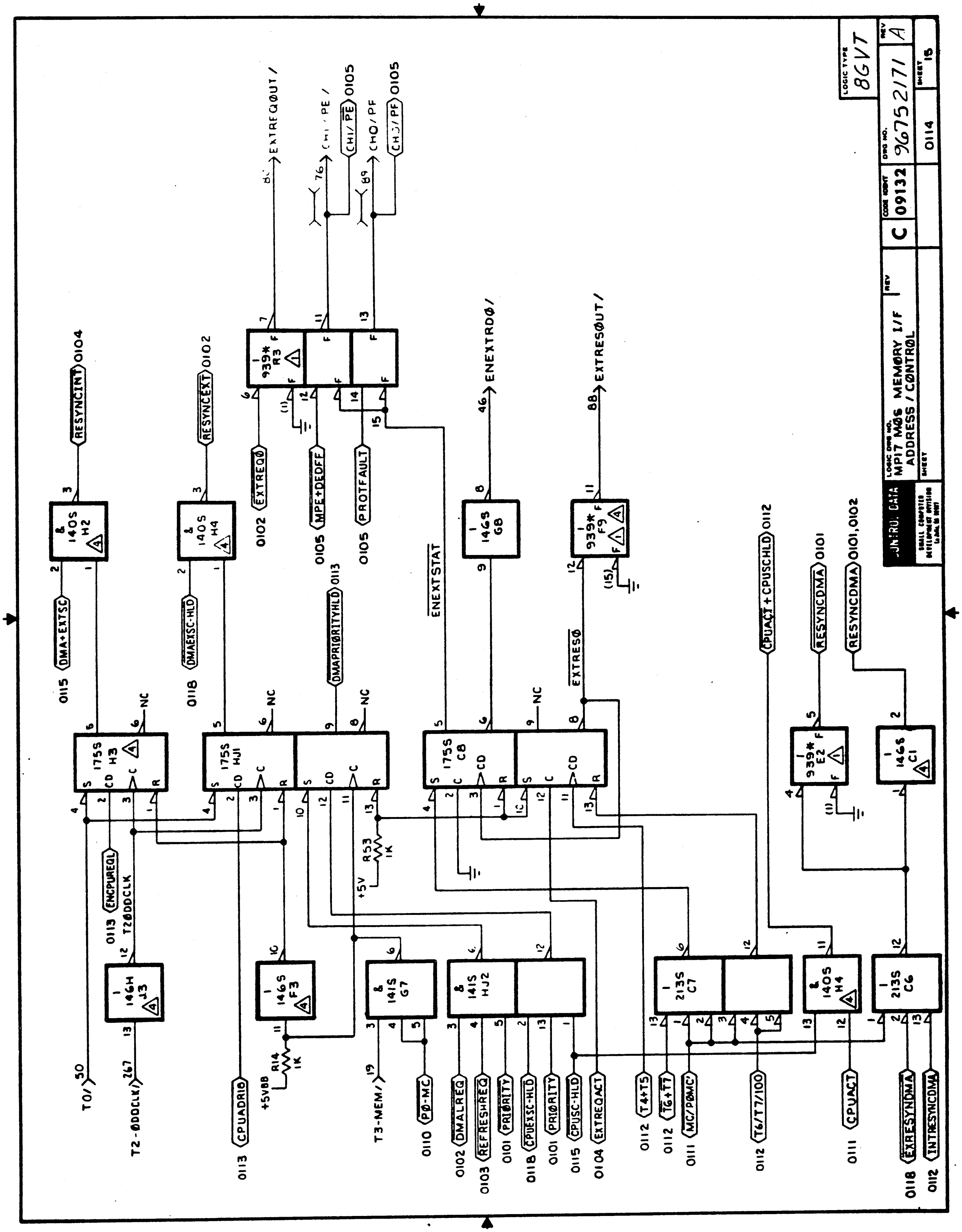


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 15 of 20)

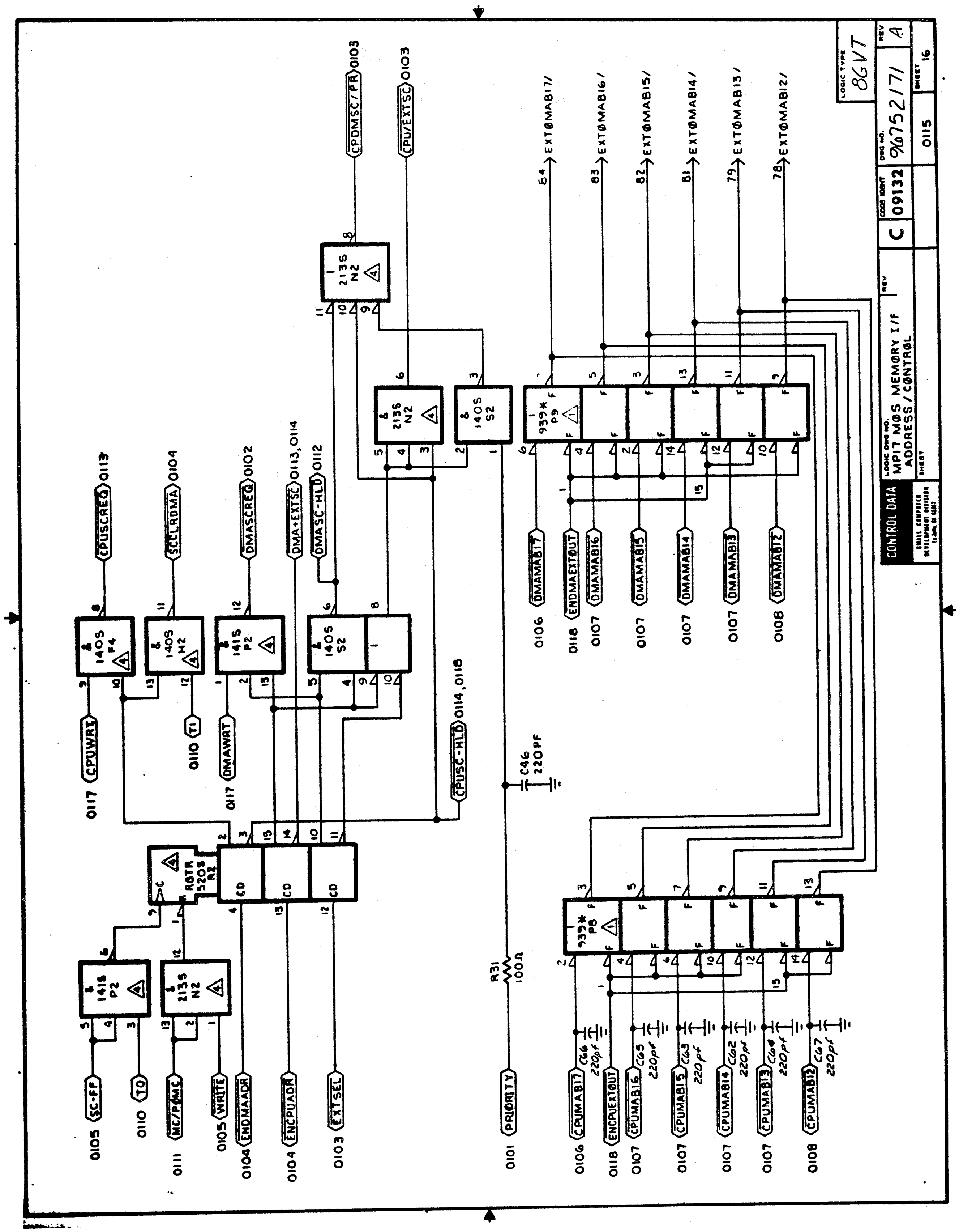


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 16 of 20)

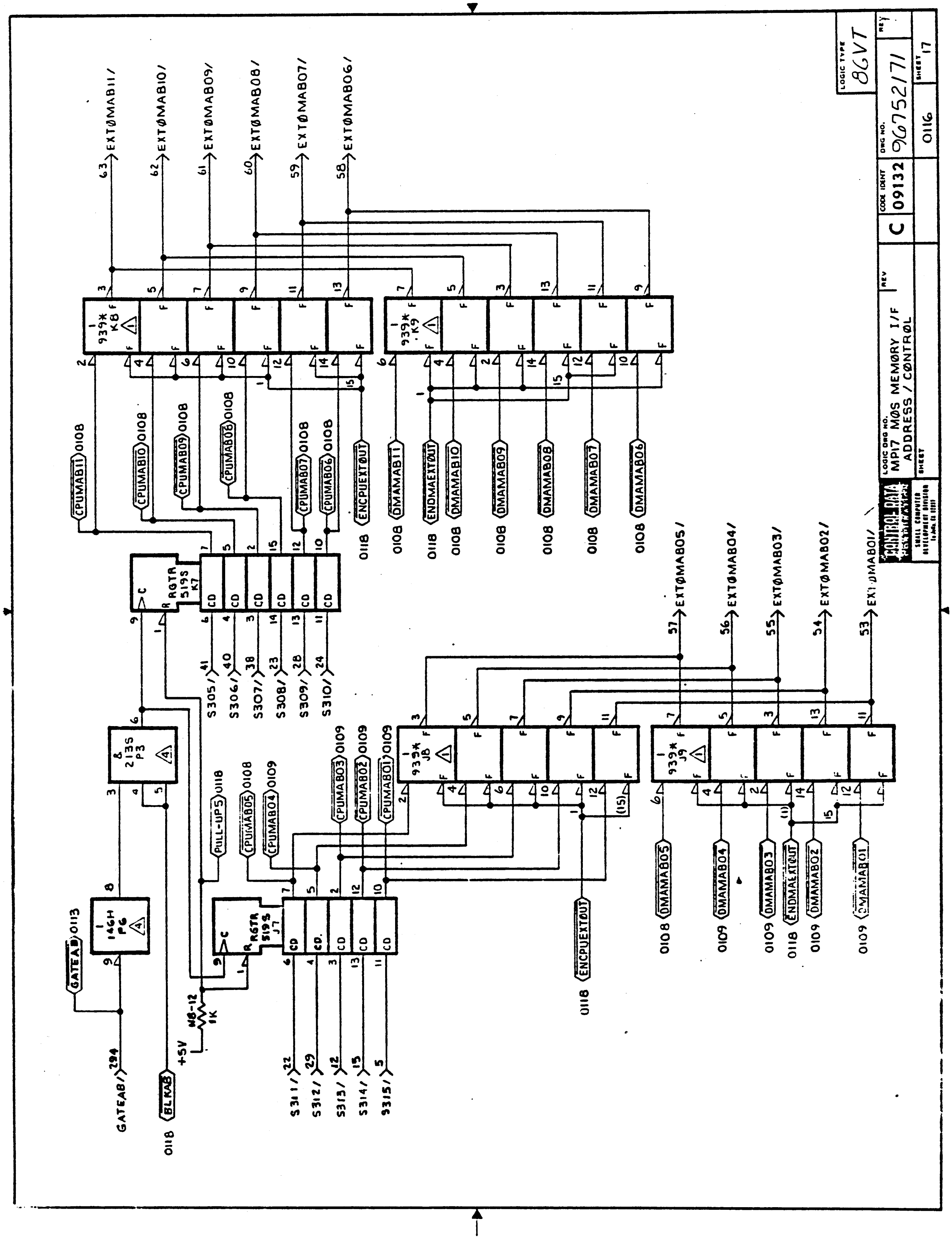


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 17 of 20)

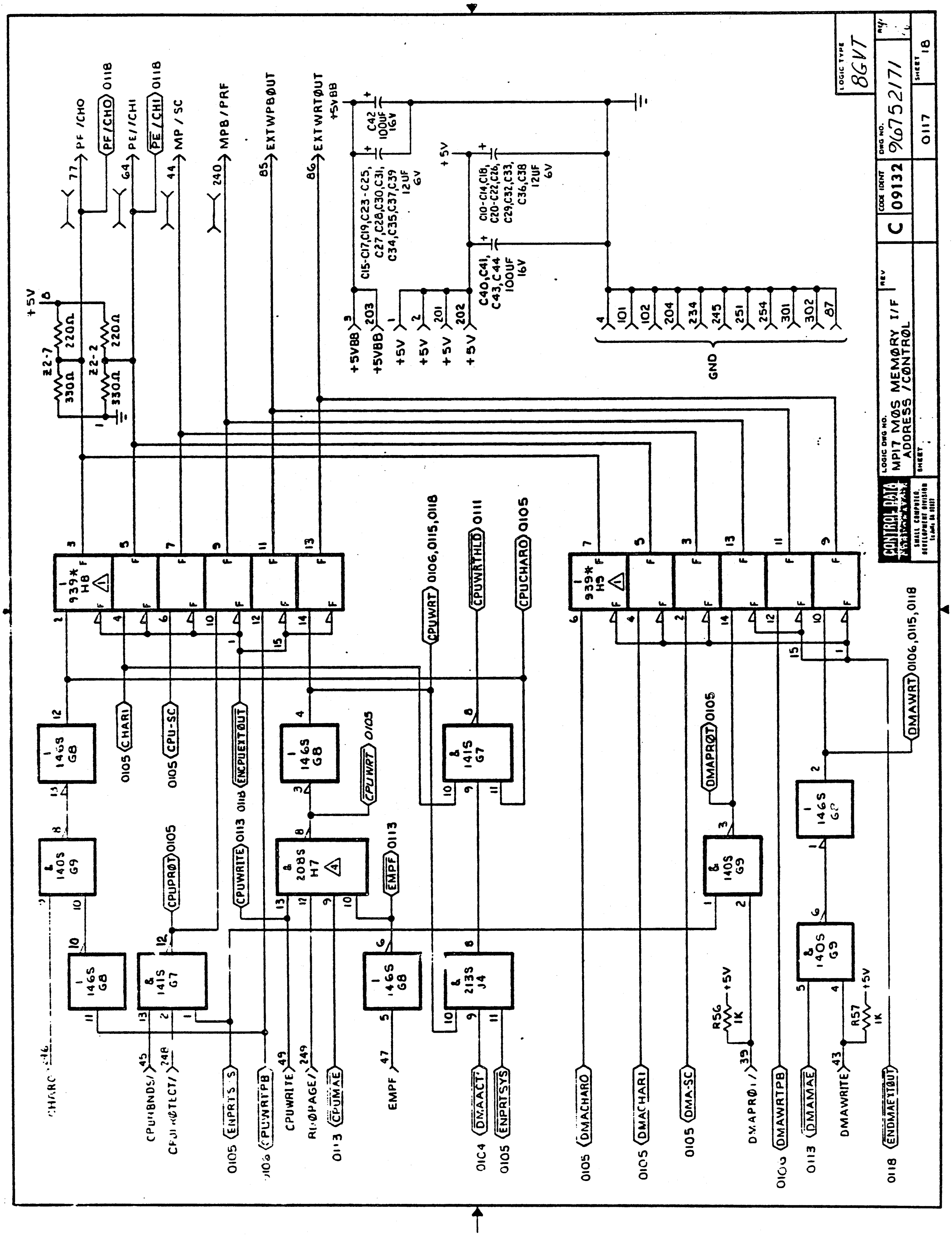


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 18 of 20)

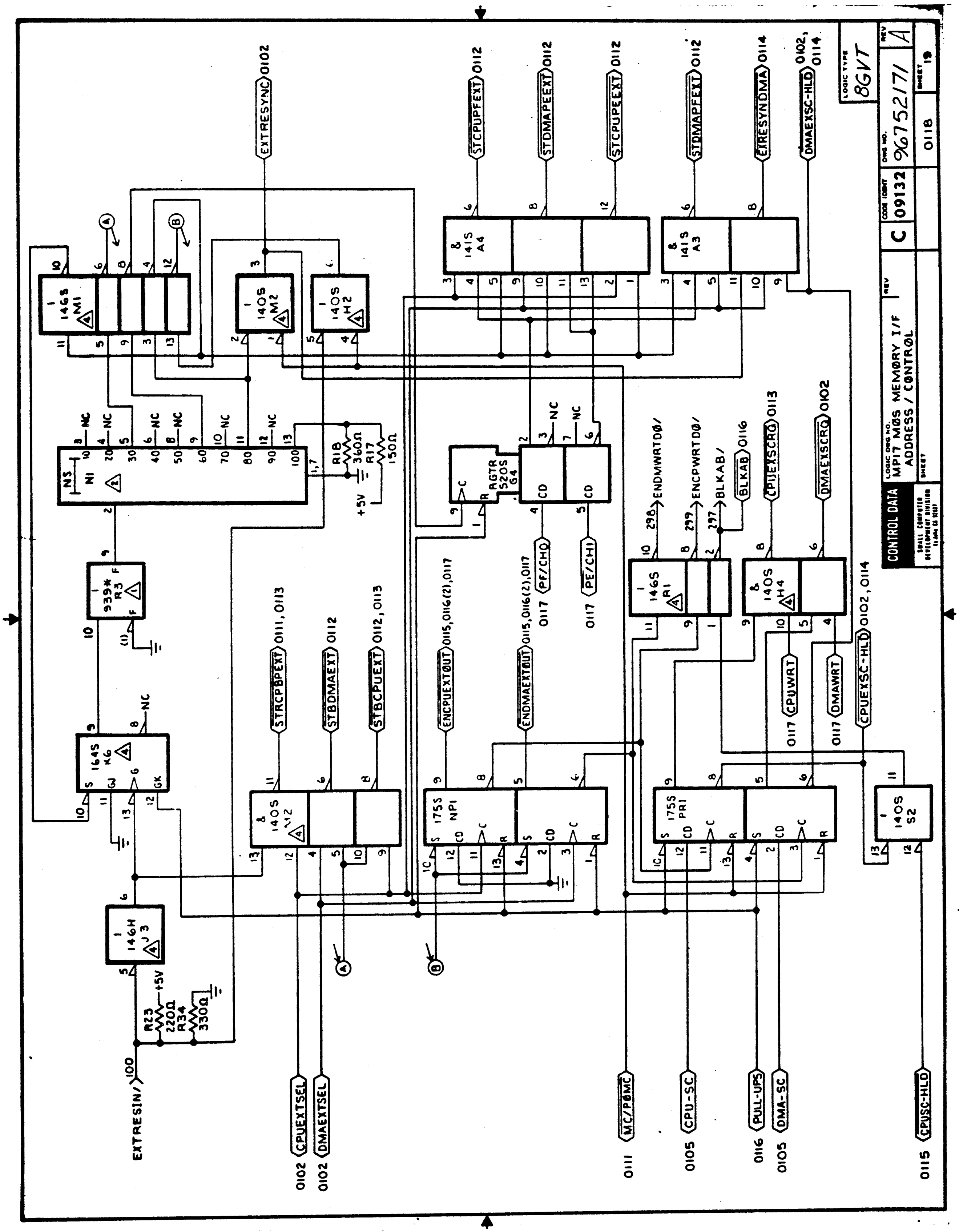


Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 19 of 20)

I(CA-5TA)

DWN		2/9/78		TITLE LOGIC - MOS MEM I/F ADDR/CONT	PREFIX DR	DOCUMENT NO 96752171	REV B
CHKD		2-16-78		FIRST USED ON 8GVT		SHEET 1 OF 1	
ENG		3-20-78					
MFG		3-27-78					
APPR		3-29-78	CODE IDENT				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS21078	CL. B. PRE-RELEASED		3-28-78	AW
B	DS22127	INACTIVE SERVICE USE ONLY SUPERSEDED BY NONE		11-6-81	

INACTIVE

NOTES

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DETACHED LISTS

AA6010

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Figure 5-10.1. MOS Memory Interface Address/Control (PWA 96752170) Logic Diagram (Sheet 20 of 20)

SIGNAL	PIN	
BLKAB/	297	0118
CAS/	239	0110
CHARO	246	0117
CHAR1	269	0105
CHR-0/	289	0105
CHR-1/	290	0105
CHO/PF	89	0114
CH1/PE/	76	0114
CPUMAB12/	268	0108
CPUMAB13/	286	0107
CPUMAB14/	280	0107
CPUMAB15/	293	0107
CPUMAB16/	285	0107
CPUMAB17/	283	0106
CPUMAB18/	17	0113
CPUMDS/	282	0113
CPUNBDS/	45	0117
CPUPRØTECT/	248	0117
CPUREQ/	225	0113
CPUWRITE	49	0117
CPUWRTPB	36	0106
CPU-SC/	272	0105
CS/	237	0107
CPUBKPWRT	266	0105
DMACHARO	230	0105
DMACHAR1	250	0105
DMAMAB01/	37	0109
DMAMAB02/	253	0109
DMAMAB03/	255	0109
DMAMAB04/	256	0109
DMAMAB05/	263	0108
DMAMAB06/	35	0108
DMAMAB07/	277	0108
DMAMAB08/	52	0108
DMAMAB09/	252	0108
DMAMAB10/	261	0108
DMAMAB11/	262	0108
DMAMAB12/	274	0108
DMAMAB13/	292	0107
DMAMAB14/	281	0107
DMAMAB15/	282	0107

SIGNAL	PIN	
DMAMAB16/	271	0107
DMAMAB17/	284	0106
DMAMAE/	18	0113
DMAMDS/	221	0112
DMAMPE/	215	0112
DMAPRØT/	39	0117
DMAREQACT/	296	0104
DMAWRITE	43	0117
DMAWRTPB/	273	0106
DMA1-INT	210	0101
DMA1-MR/	11	0101
DMA1-RA/	227	0101
DMA2-INT	205	0101
DMA2-MR/	214	0101
DMA2-RA/	219	0101
DMA3 INT	243	0101
DMA3-MR/	212	0101
DMA3-RA/	220	0101
DMA4-INT	211	0101
DMA4-MR/	213	0101
DMA4-RA/	216	0101
DMA-PF/	228	0112
DMA-SC/	270	0105
ECCHERE/	34	0112
EMPF	47	0117
ENCPWRTDØ/	299	0118
ENDMWRTDØ/	298	0118
ENEXTRDØ/	46	0114
ENMØSWRTD/	217	0112
ENMØS-250	42	0111
ENPRTSYS	247	0105
EXTBANK/	99	0113
EXTIMAB01/	65	0109
EXTIMAB02/	66	0109
EXTIMAB03/	67	0109
EXTIMAB04/	68	0109
EXTIMAB05/	69	0108
EXTIMAB06/	70	0108
EXTIMAB07/	71	0108
EXTIMAB08/	72	0108
EXTIMAB09/	73	0108

SIGNAL	PIN	
EXTIMAB10/	74	0108
EXTIMAB11/	75	0108
EXTIMAB12/	90	0108
EXTIMAB13/	91	0107
EXTIMAB14/	93	0107
EXTIMAB15/	94	0107
EXTIMAB16/	95	0107
EXTIMAB17/	96	0106
EXTØMAB01/	53	0116
EXTØMAB02/	54	0116
EXTØMAB03/	55	0116
EXTØMAB04/	56	0116
EXTØMAB05/	57	0116
EXTØMAB06/	58	0116
EXTØMAB07/	59	0116
EXTØMAB08/	60	0116
EXTØMAB09/	61	0116
EXTØMAB10/	62	0116
EXTØMAB11/	63	0116
EXTØMAB12/	78	0115
EXTØMAB13/	79	0115
EXTØMAB14/	81	0115
EXTØMAB15/	82	0115
EXTØMAB16/	83	0115
EXTØMAB17/	84	0115
EXTREQACT/	295	0104
EXTREQIN/	92	0103
EXTREQØUT/	80	0114
EXTRESIN/	100	0118
EXTRESØUT/	88	0114
EXTWPBIN	97	0106
EXTWPBØUT	85	0117
EXTWRTIN	98	0106
EXTWRTØUT	86	0117
EI6KNO-1/	208	0106
EI6KNO-2/	207	0106
EI6KNO-3/	206	0106
EI6KNO-4/	209	0106
EI6KNI-1/	226	0106
EI6KNI-2/	26	0106
EI6KNI-3/	25	0106
EI6KNI-4/	27	0106

SIGNAL	PIN	
GATEAB/	294	0116
GND	4	0117
GND	101	0117
GND	102	0117
GND	204	0117
GND	234	0117
GND	245	0117
GND	251	0117
GND	254	0117
GND	301	0117
GND	302	0117
GND	87	0117
MCTM/	279	0102
MC/	51	0111
MØSMA00	258	0109
MØSMA01	257	0109
MØSMA02	260	0109
MØSMA03	259	0109
MØSMA04	265	0109
MØSMA05	264	0109
MPB-L	20	0105
MPB/PRF	240	0117
MPE+DED/	21	0113
MP /SC	44	0117
PE//CH1	64	0117
PF/CHO	77	0117
PØWERFAIL/	48	0110
PRF/MPB	288	0105
PRIØRITY	218	0101
RASI6KO-1/	236	0106
RASI6KO-2/	32	0106
RASI6KO-3/	33	0106
RASI6KO-4/	232	0106
RASI6KI-1/	244	0106
RASI6KI-2/	30	0106
RASI6KI-3/	233	0106
RASI6KI-4/	31	0106
RDØPAGE/	249	0117

SIGNAL	PIN	
SC/MPL	287	0105
SELCPUEXT/	6	0111
SELCPUINT/	223	0111
SETSMI05/	7	0112
SETSMI08/	14	0112
SLTBLK0/	238	0107
SLTBLK1/	235	0107
SLTBLK2/	241	0107
SLTBLK3/	242	0107
STBCPUBKP/	13	0113
STBCPUDFM/	8	0112
STBDFM/	10	0112
STBDMADFM/	9	0112
STCP/EXD/	224	0110
S305/	41	0116
S306/	40	0116
S307/	38	0116
S308/	23	0116
S309/	28	0116
S310/	24	0116
S311/	22	0116
S312/	29	0116
S313/	12	0116
S314/	15	0116
S315/	5	0116
T0/	50	0114
T0-MEM/	275	0110
T2-ØDDCLK	267	0114
T3-MEM/	19	0114
WRT-MPF/	16	0113
WRT-PB/	291	0106
WT-MØS/	231	0112
+5V	1	0117
+5V	2	0117
+5V	201	0117
+5V	202	0117
+5V BB	3	0117
+5V BB	203	0117

6. 8T98 IS SIMILAR TO 939
5. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S138
4. IC TO BE CONNECTED TO +5VBB
3. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S257
2. NO ELEMENT IDENTIFIER AVAILABLE FOR 100NS DELAY
1. 8T97 IS SIMILAR TO 939

NOTES: UNLESS OTHERWISE SPECIFIED

DR 96752174

CONTROL DATA CORPORATION — MPI7 — Bob Johnson 2/8/78 — 2-16-78 — 3-2-78

MPI7 MØS MEMØRY I/F ADDRESS/CØNTRØL

8GWT

C 09132 96752174 A

PWA No. 96752173 PWB No. 96753834

SHEET 1 OF 19

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 1 of 20)

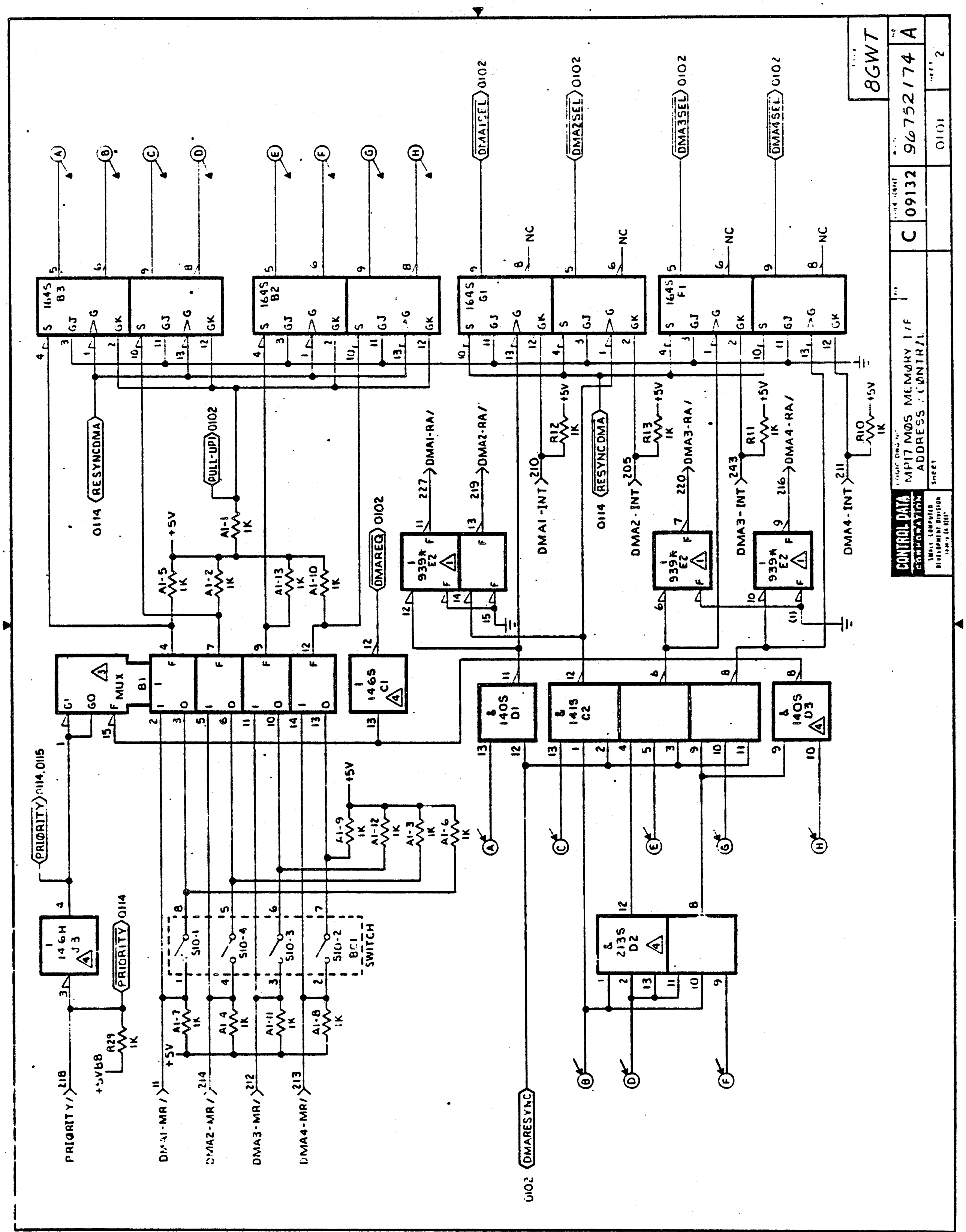

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 2 of 20)

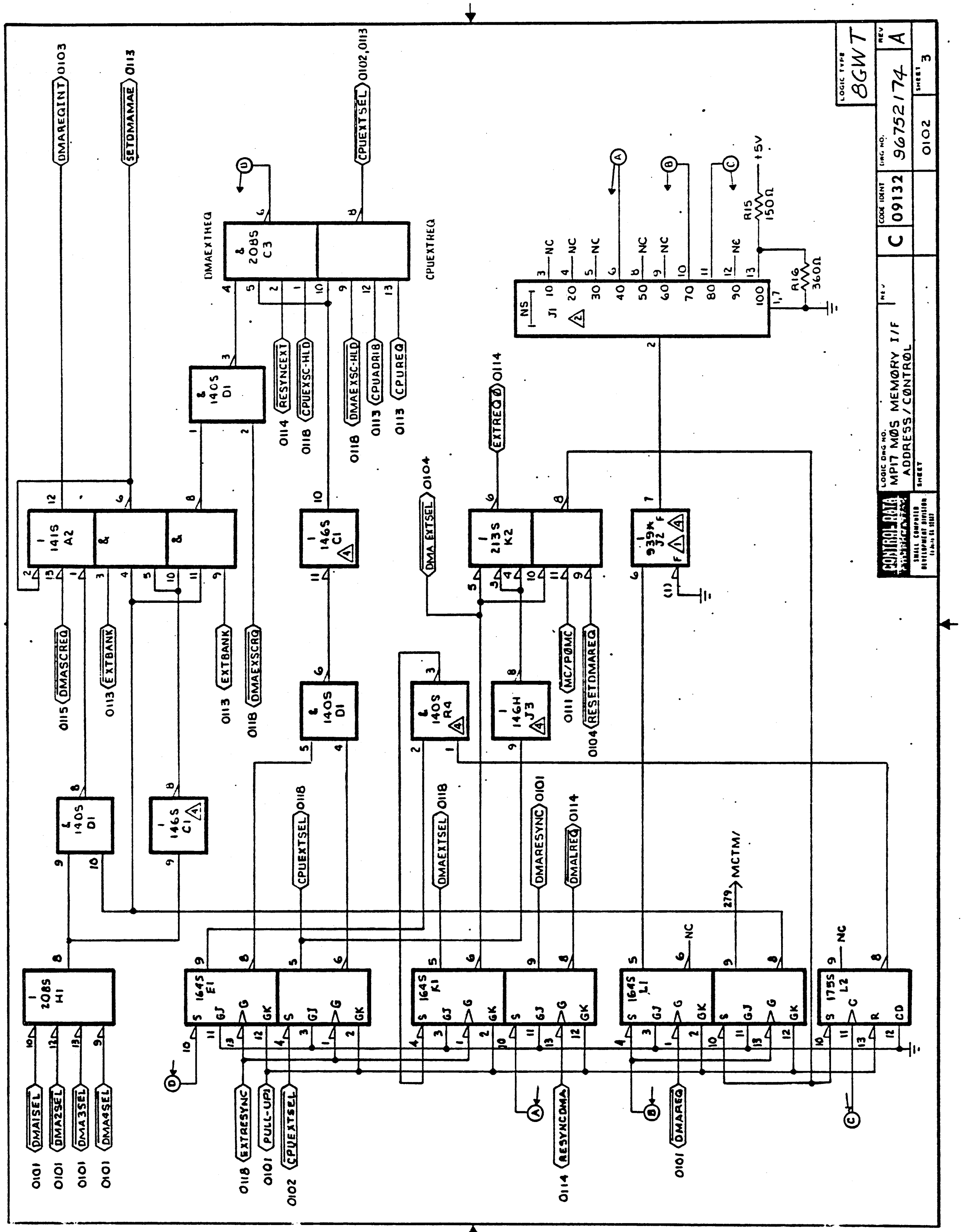

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 3 of 20)

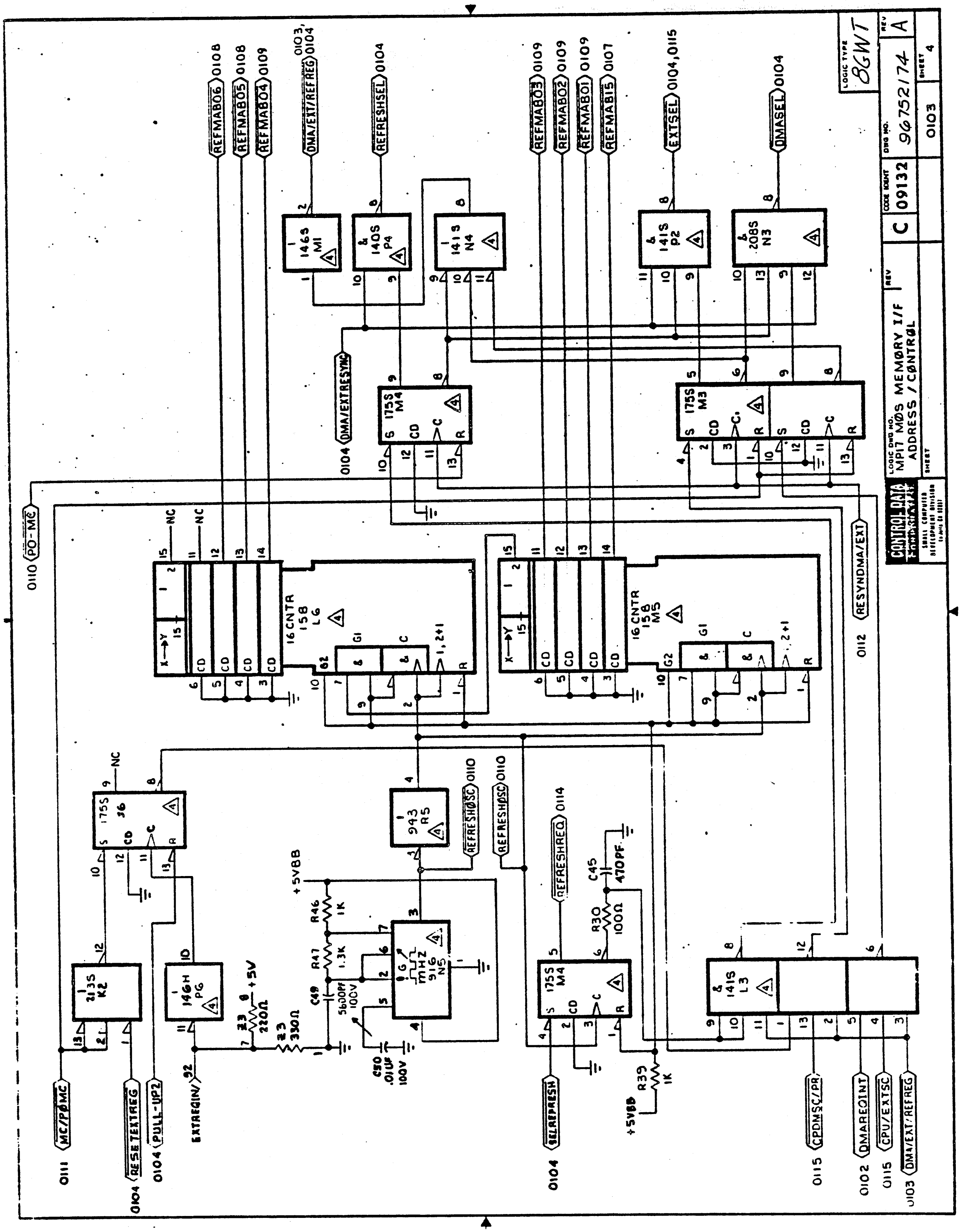

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 4 of 20)

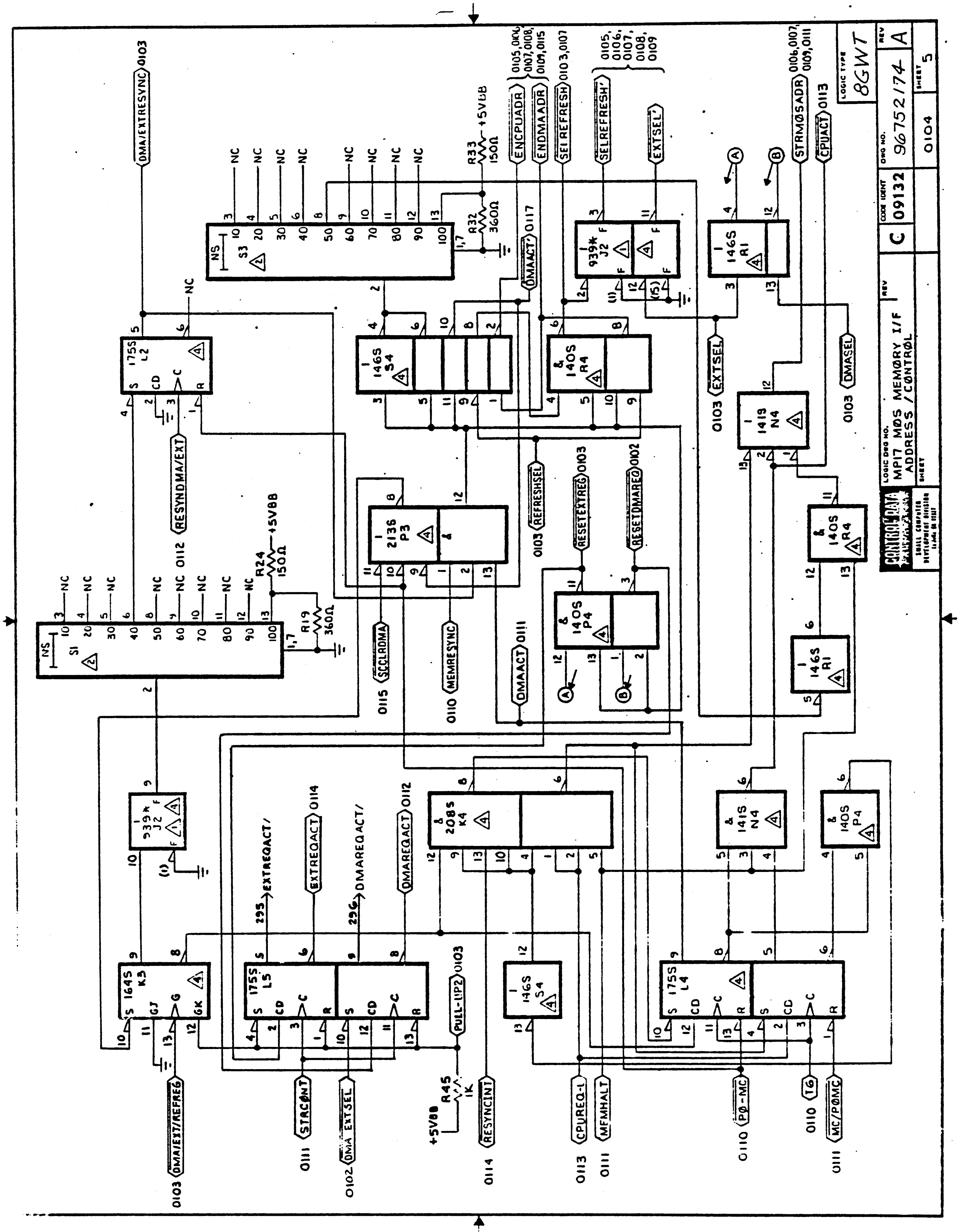

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 5 of 20)

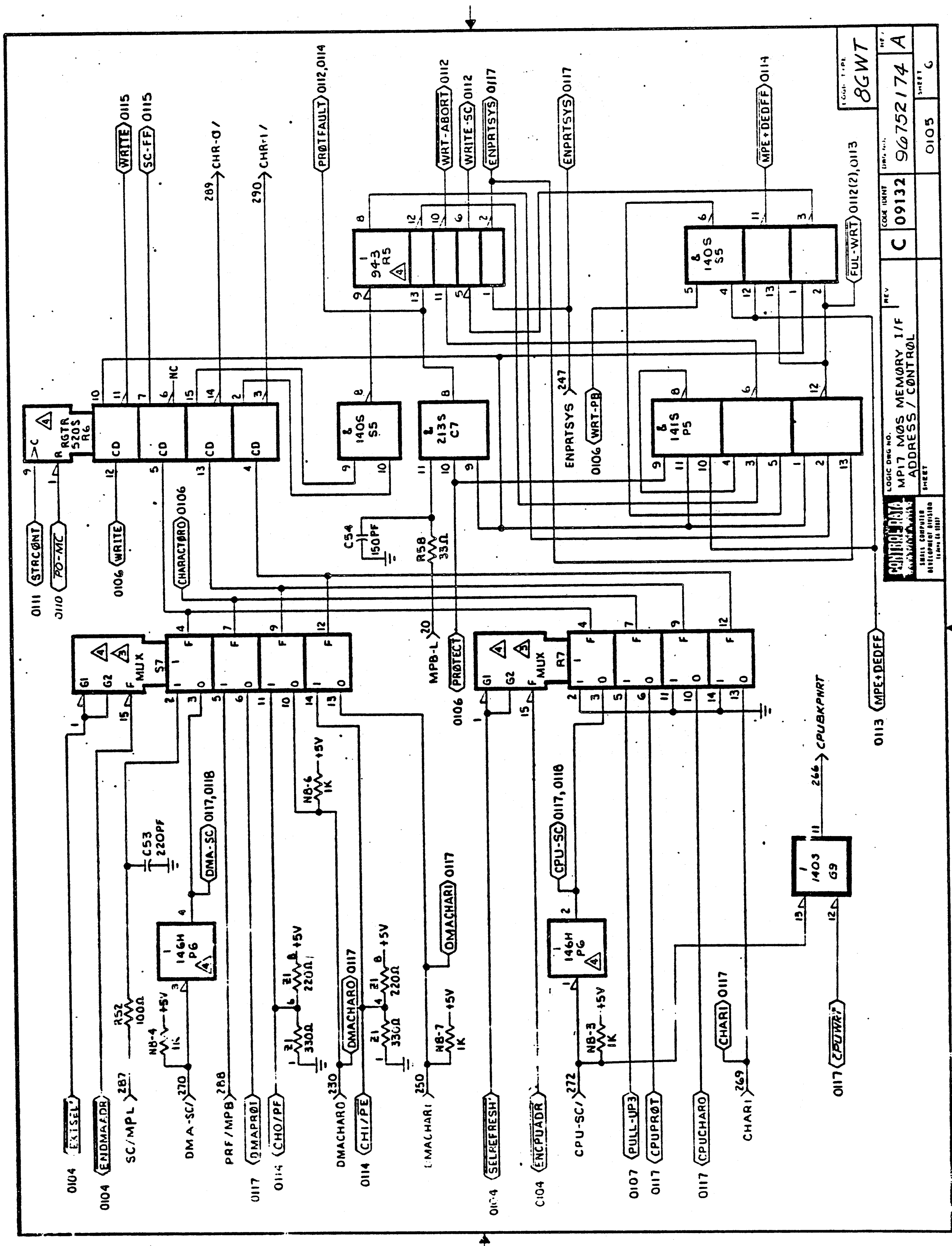

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 6 of 20)

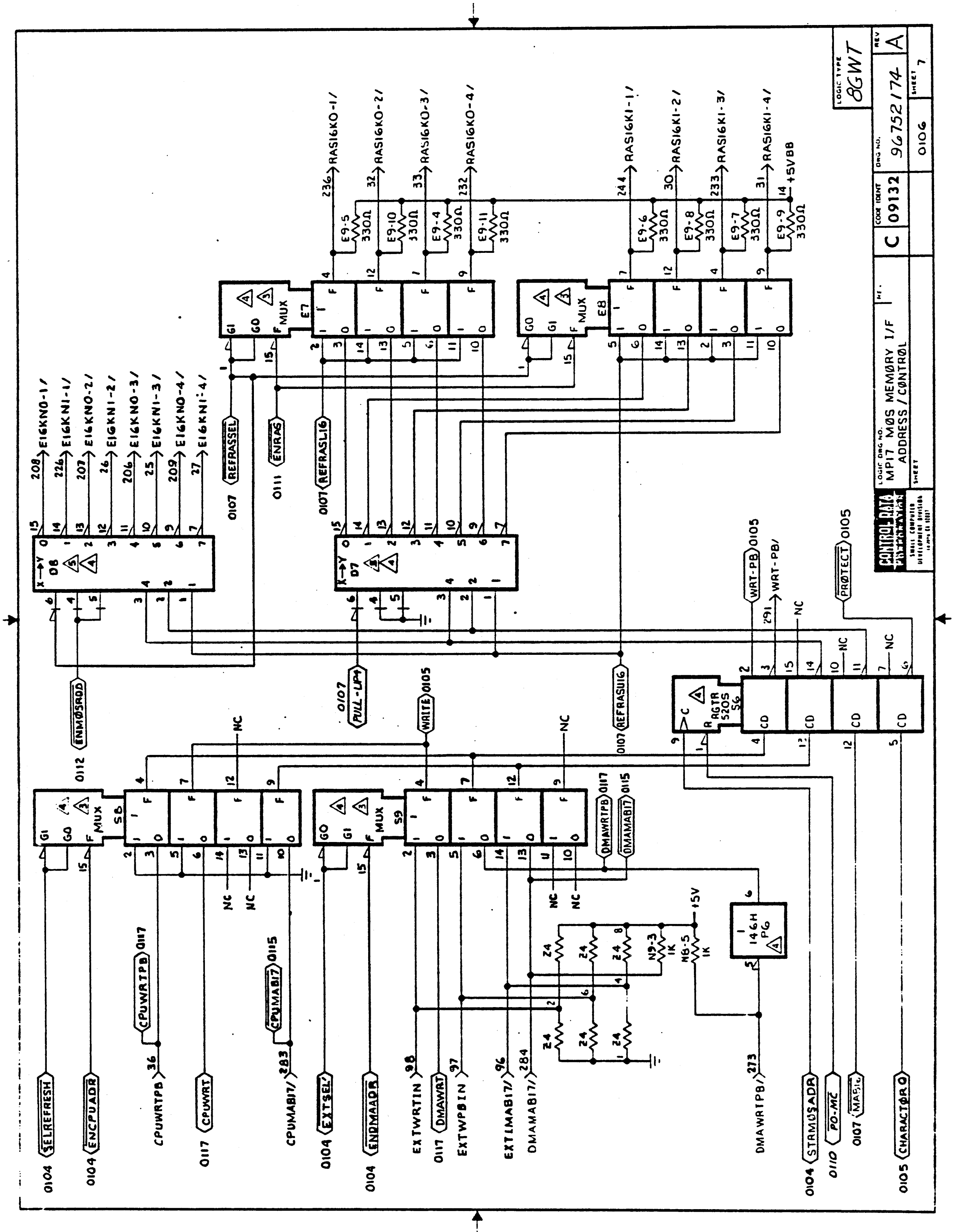

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 7 of 20)

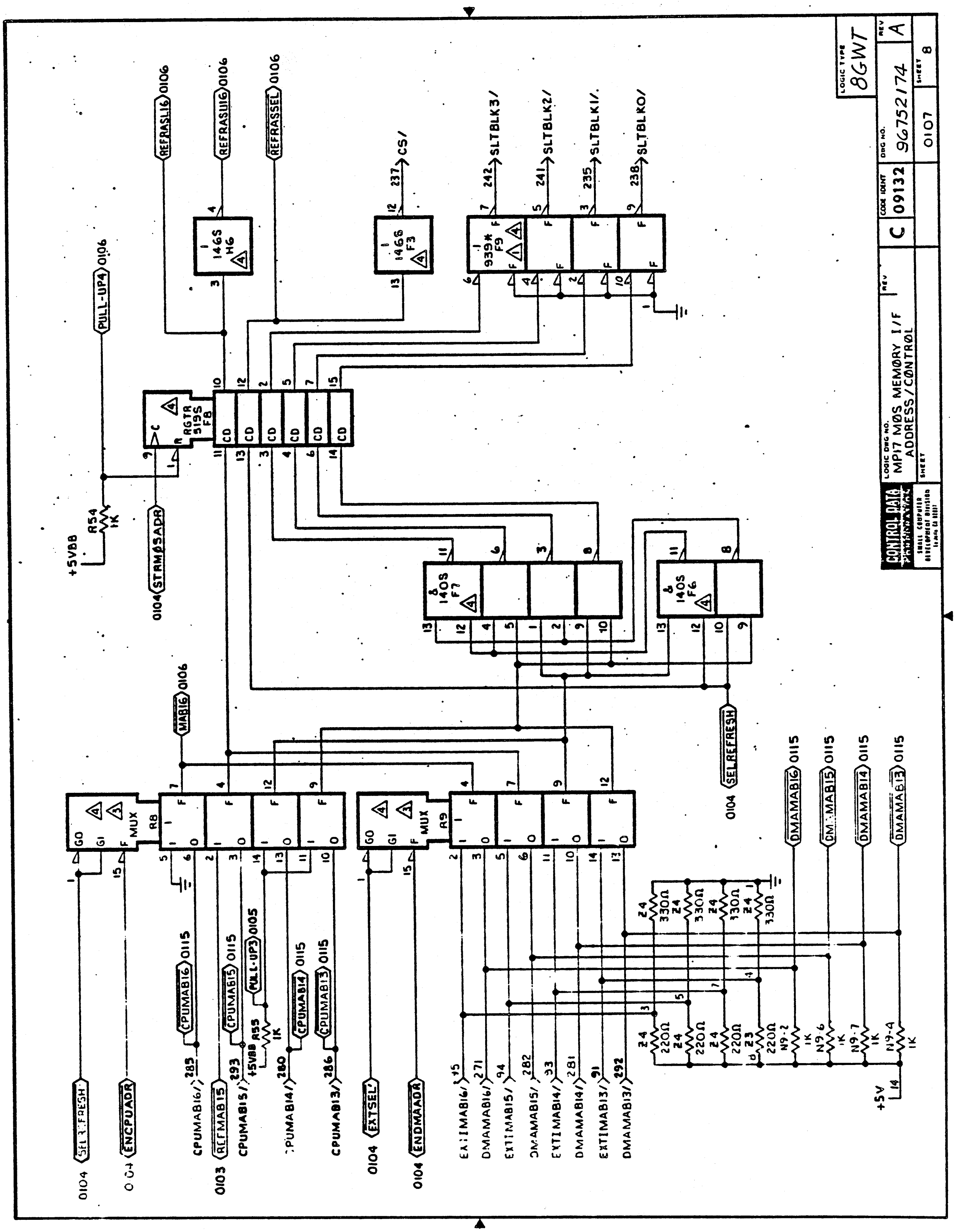

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 8 of 20)

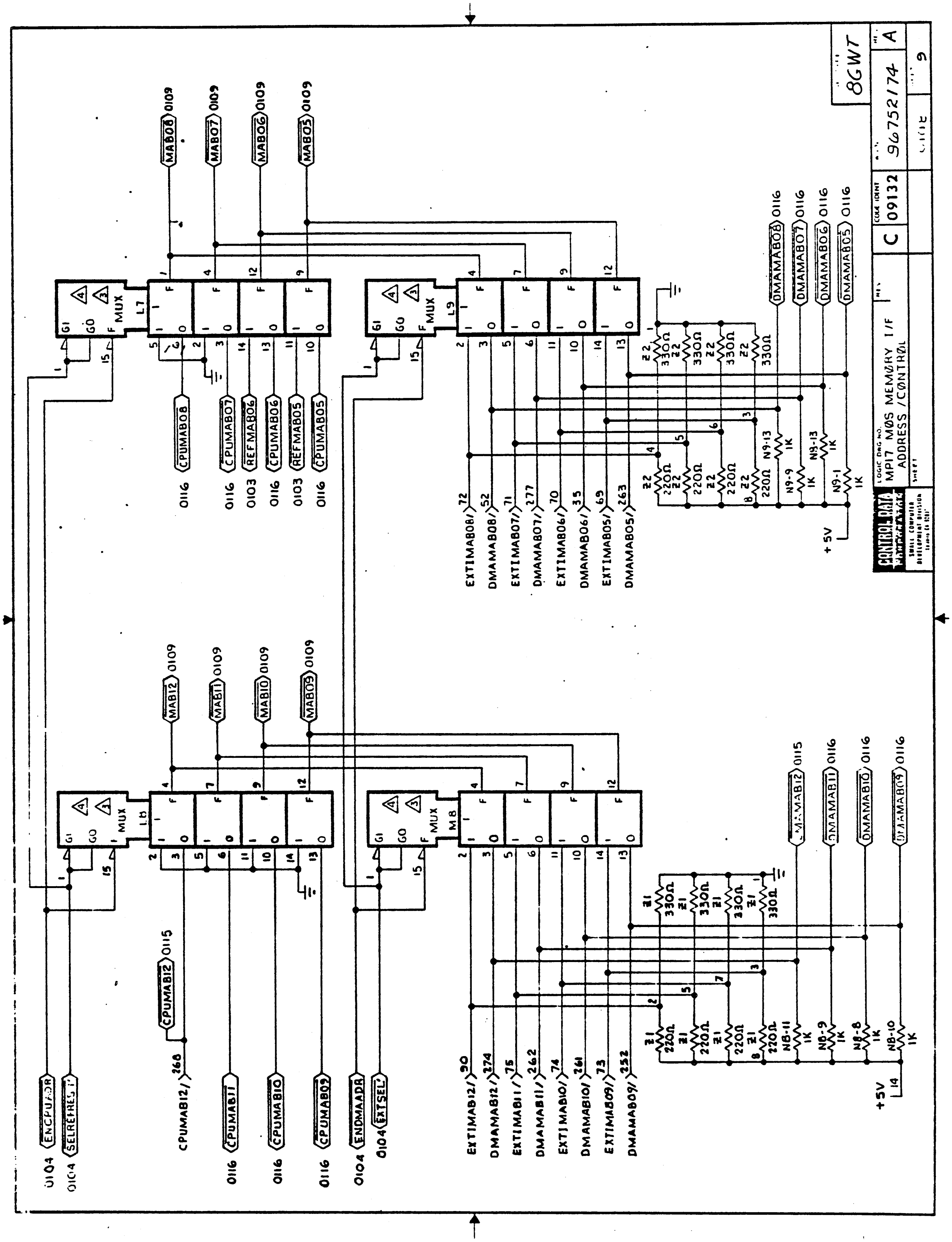

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 9 of 20)

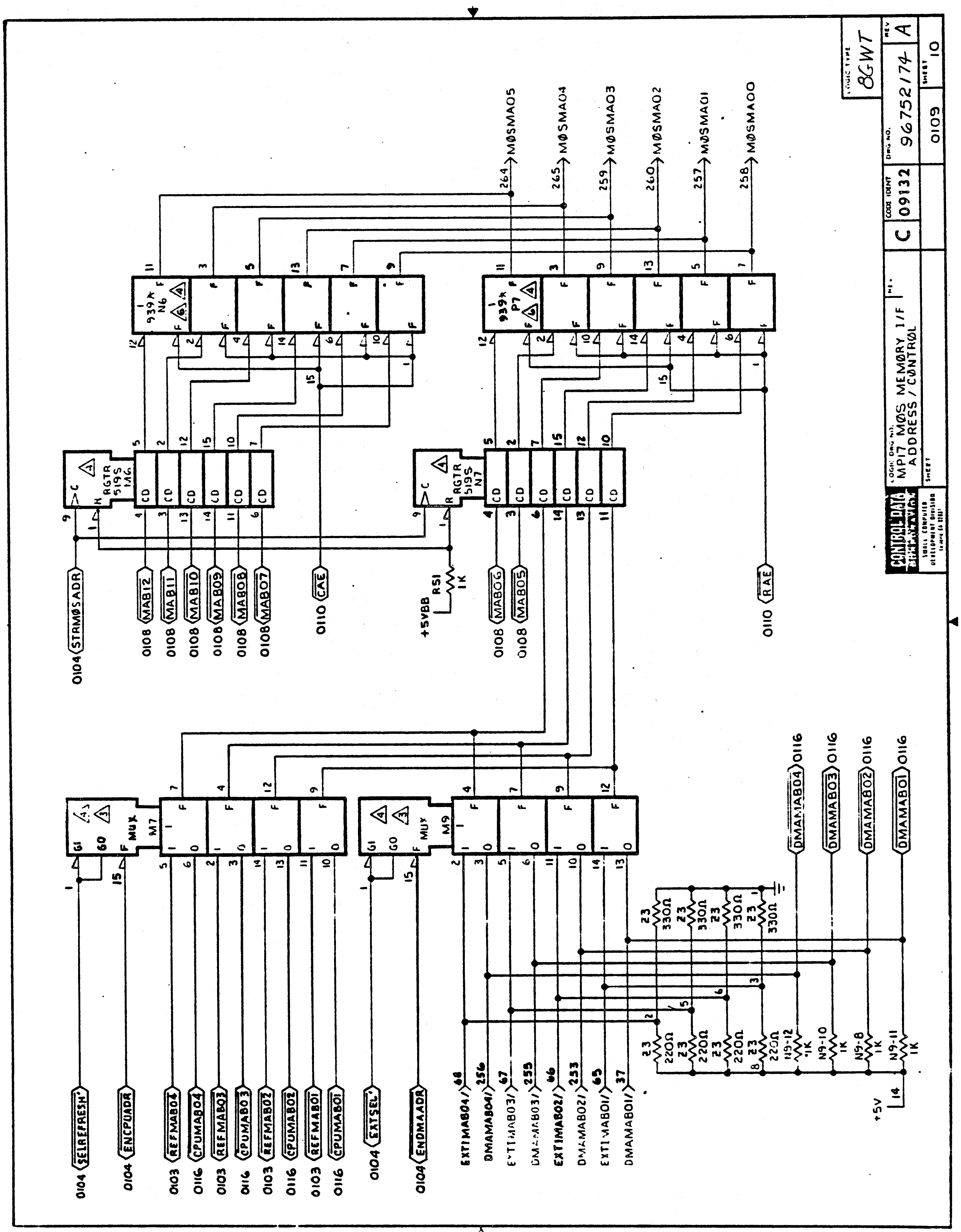

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 10 of 20)

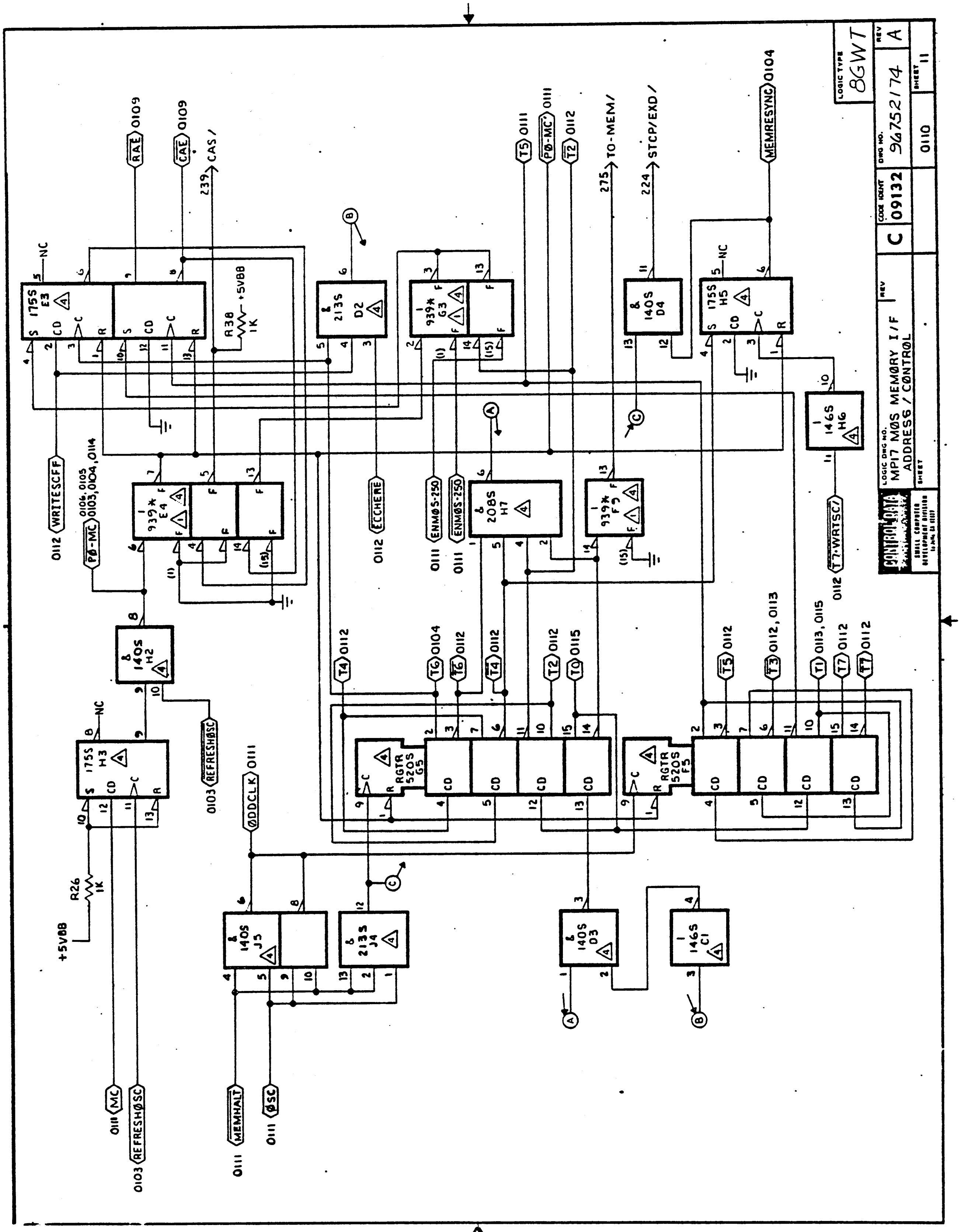

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 11 of 20)

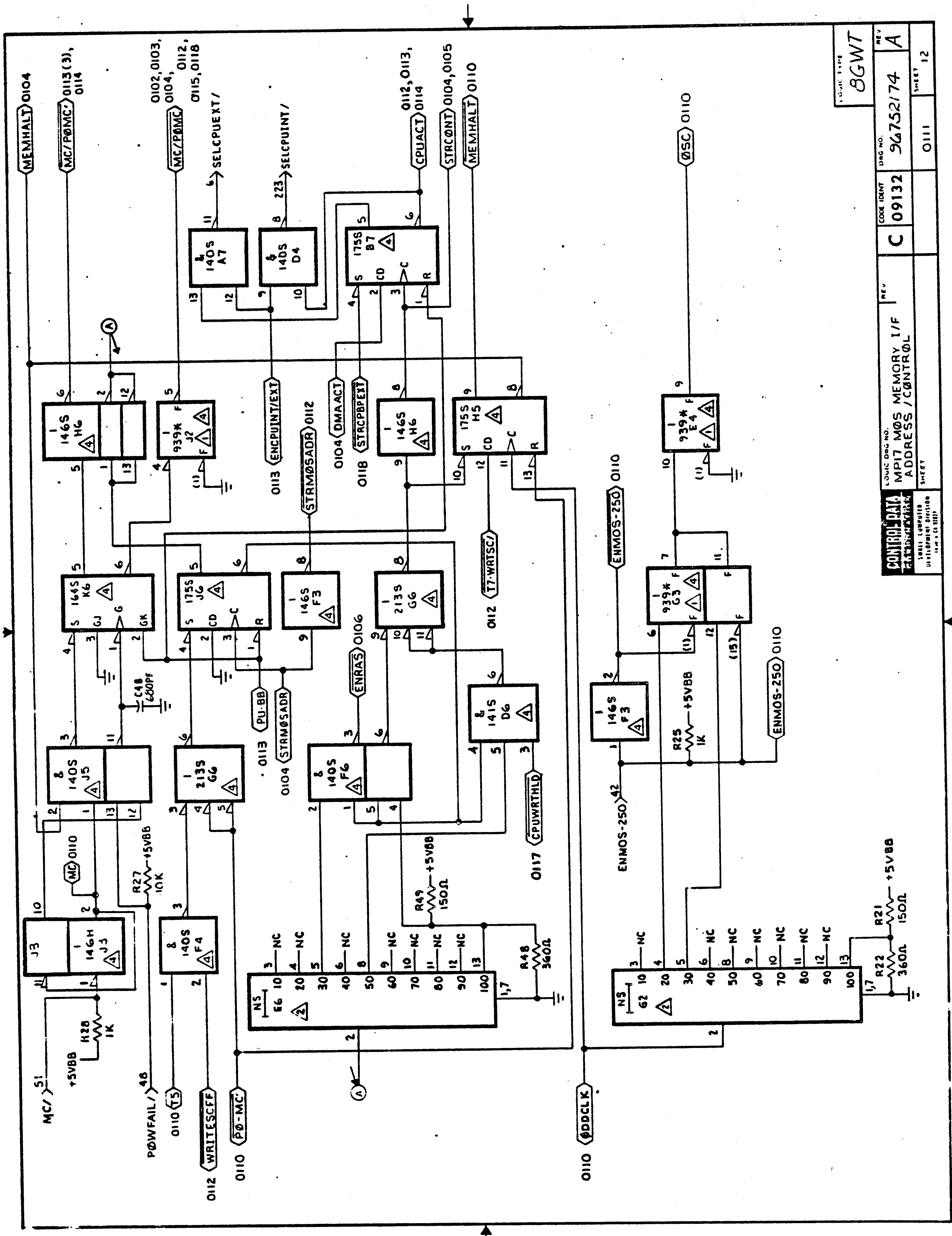

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 12 of 20)

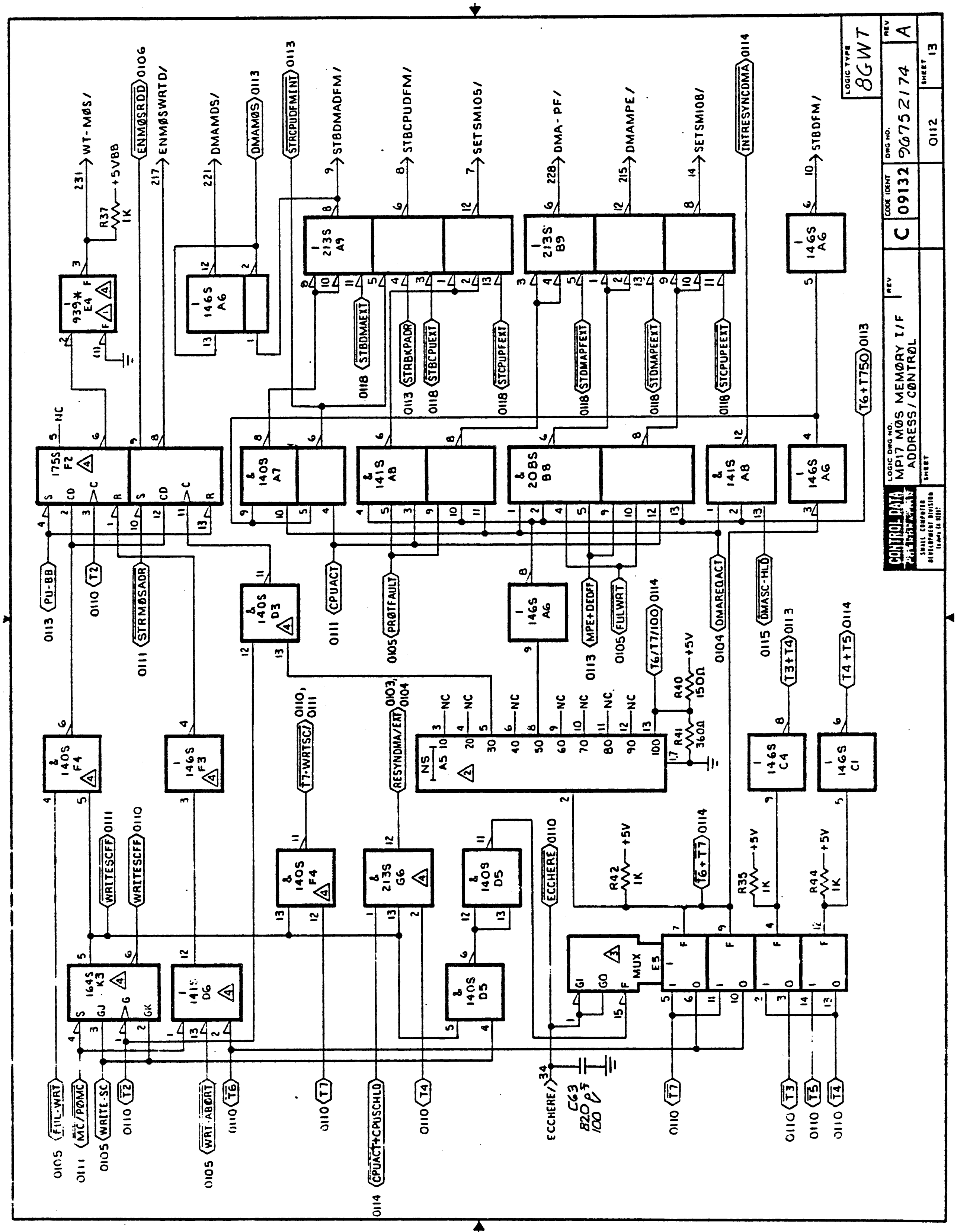

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 13 of 20)

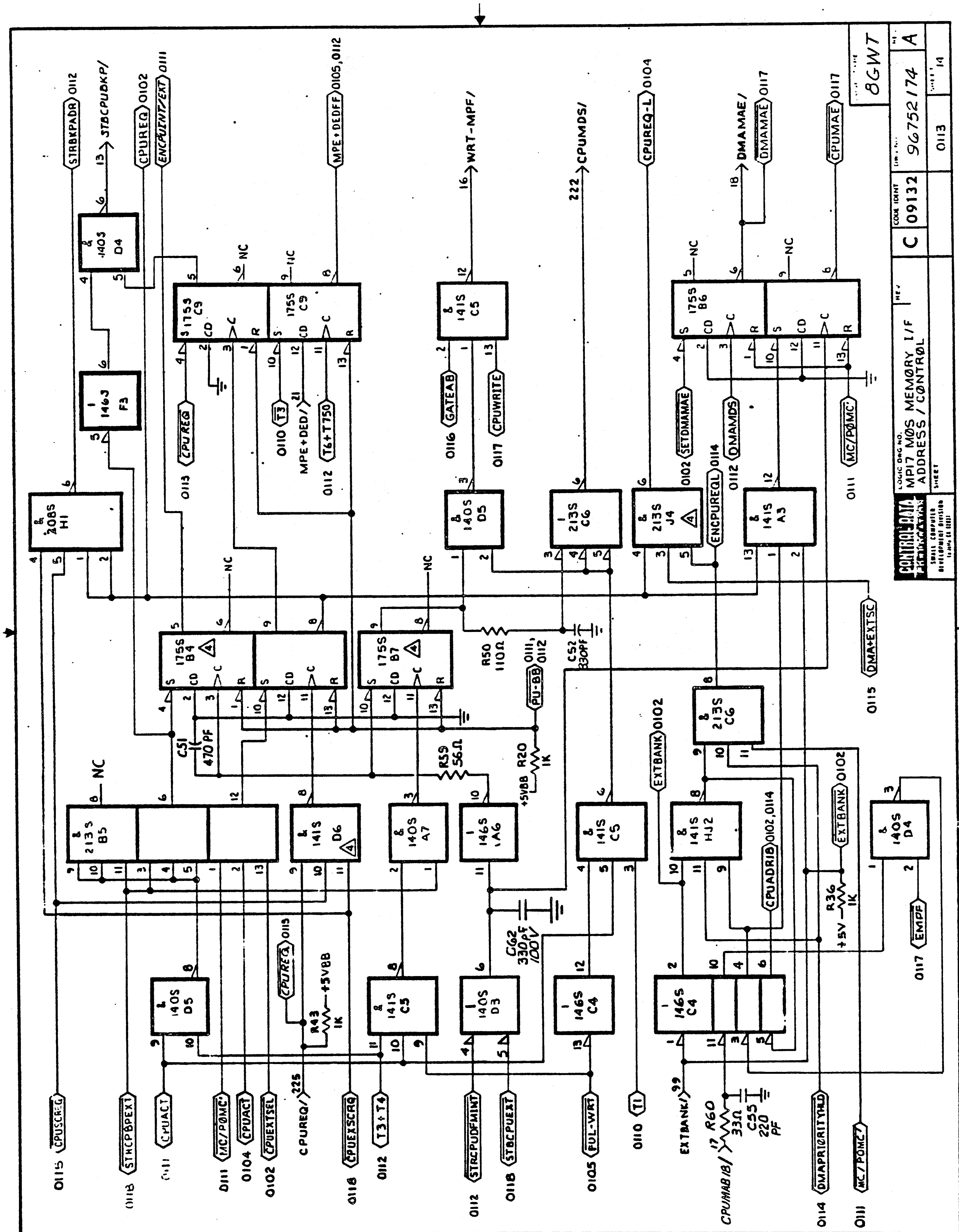

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 14 of 20)

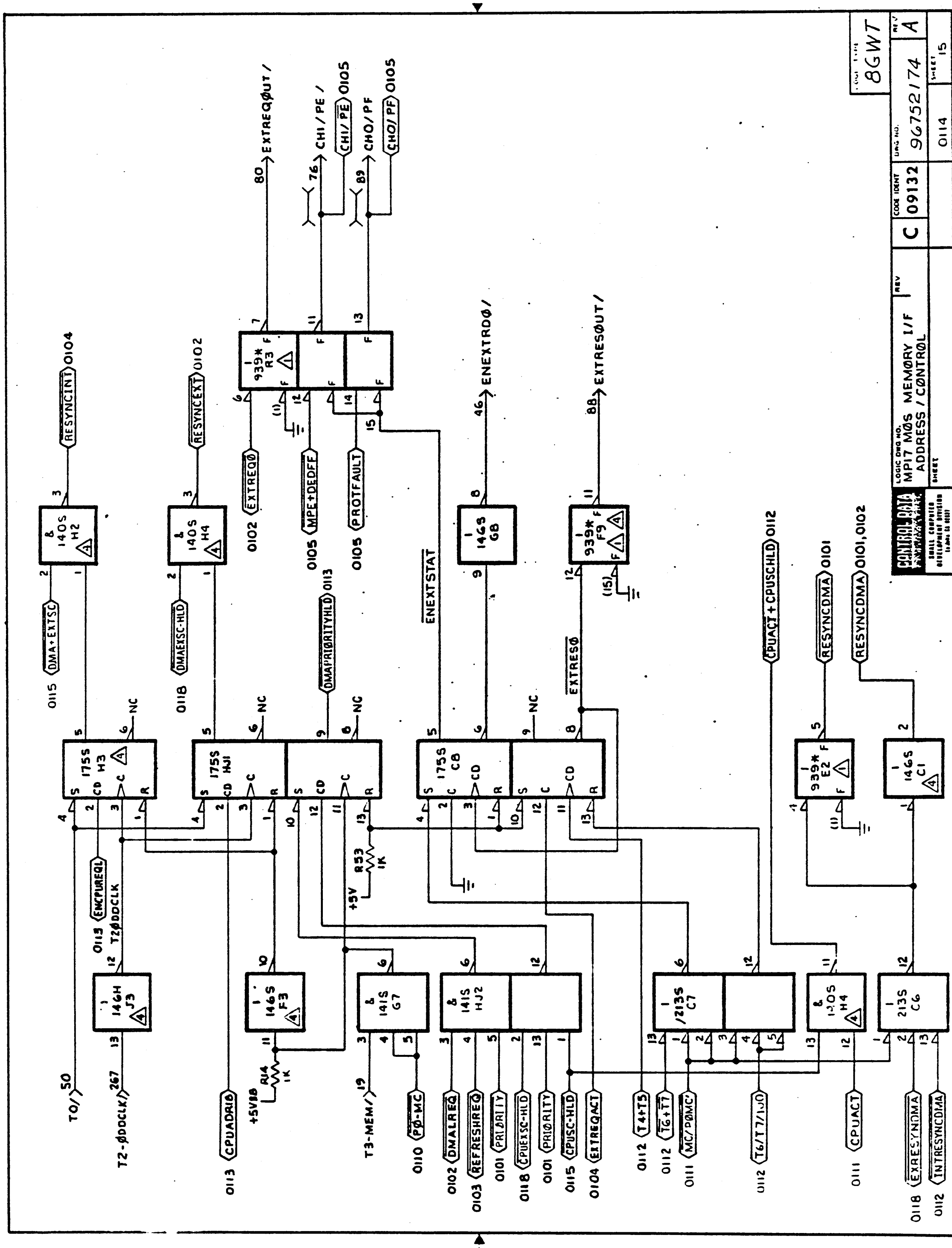

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 15 of 20)

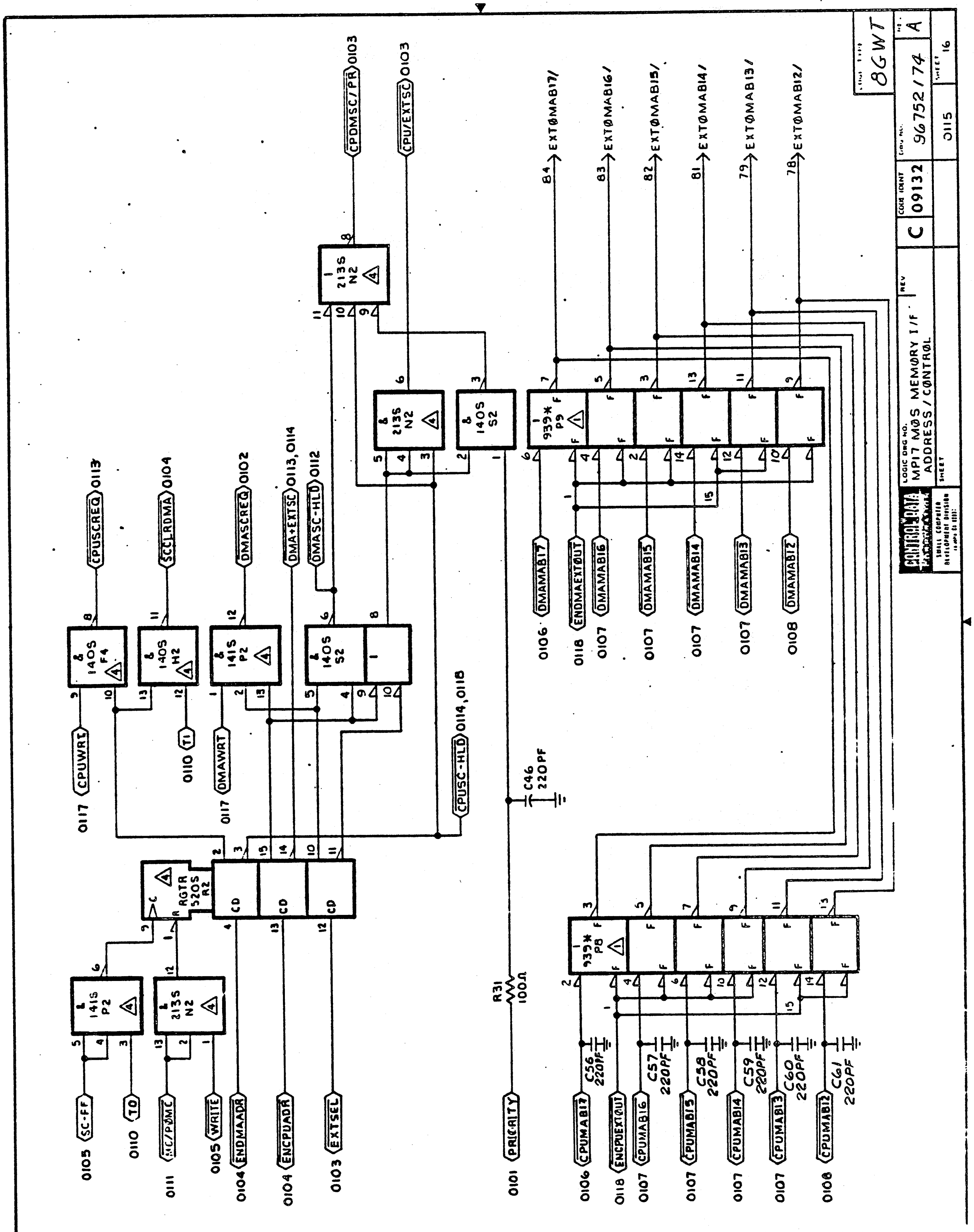

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 16 of 20)

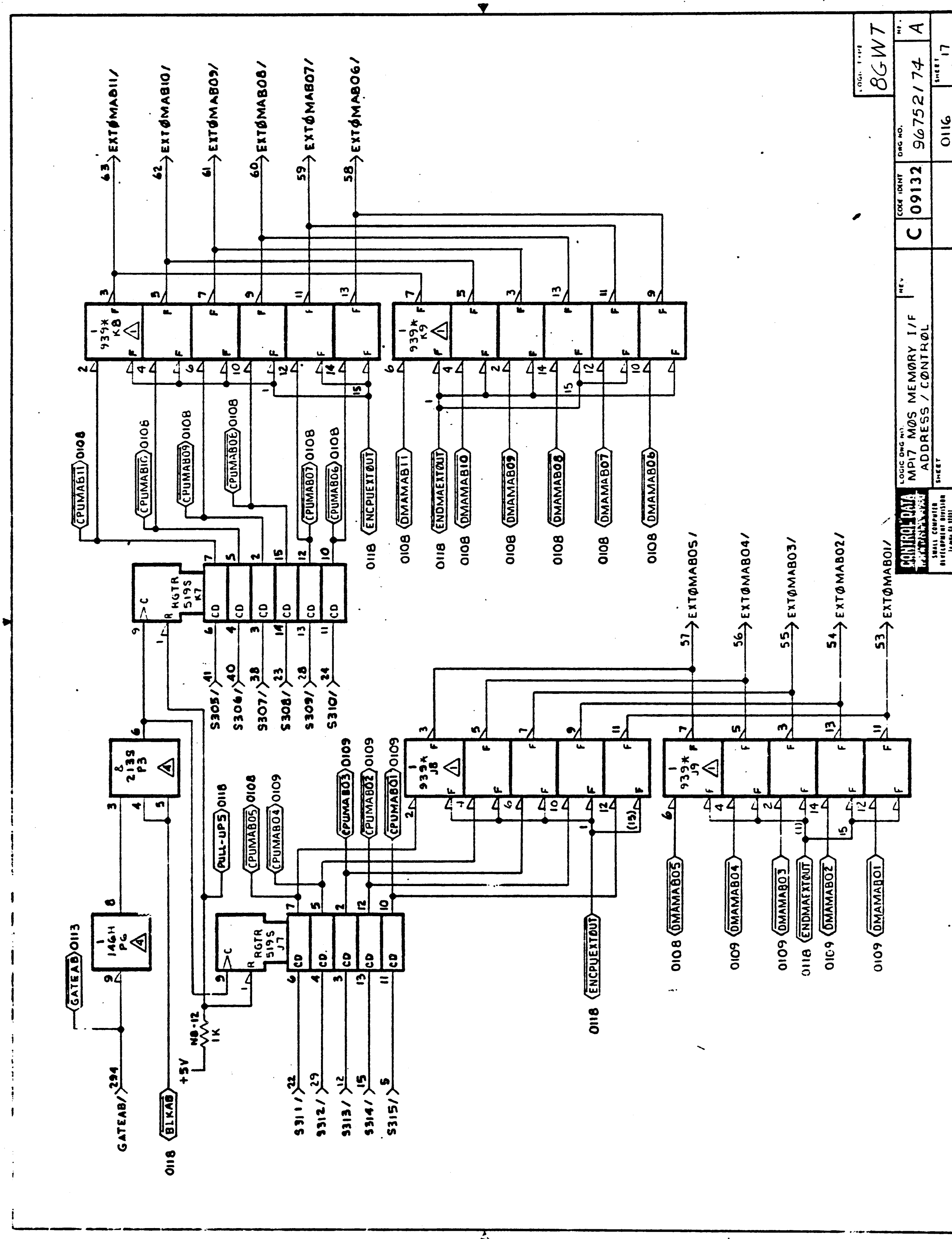

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 17 of 20)

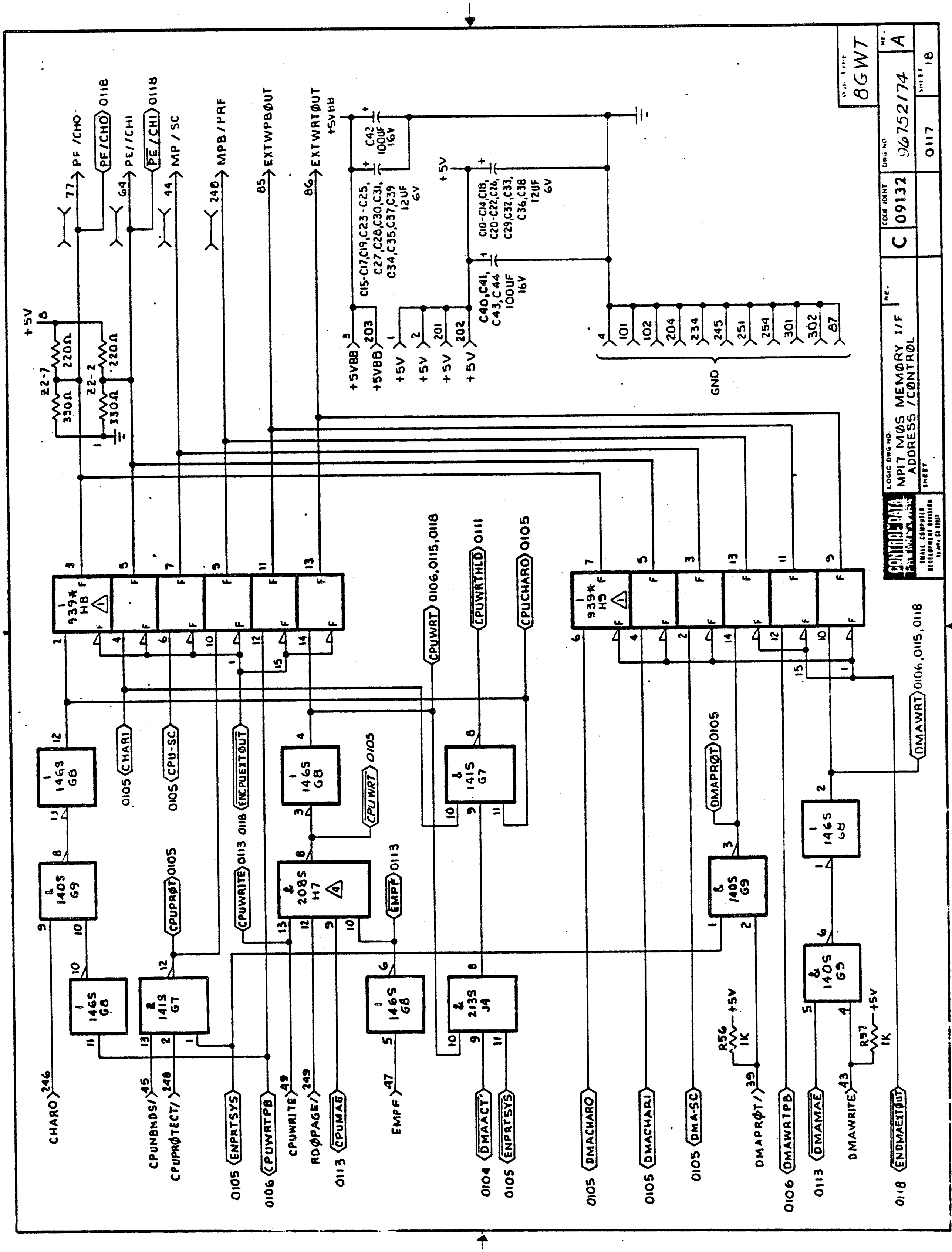

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 18 of 20)

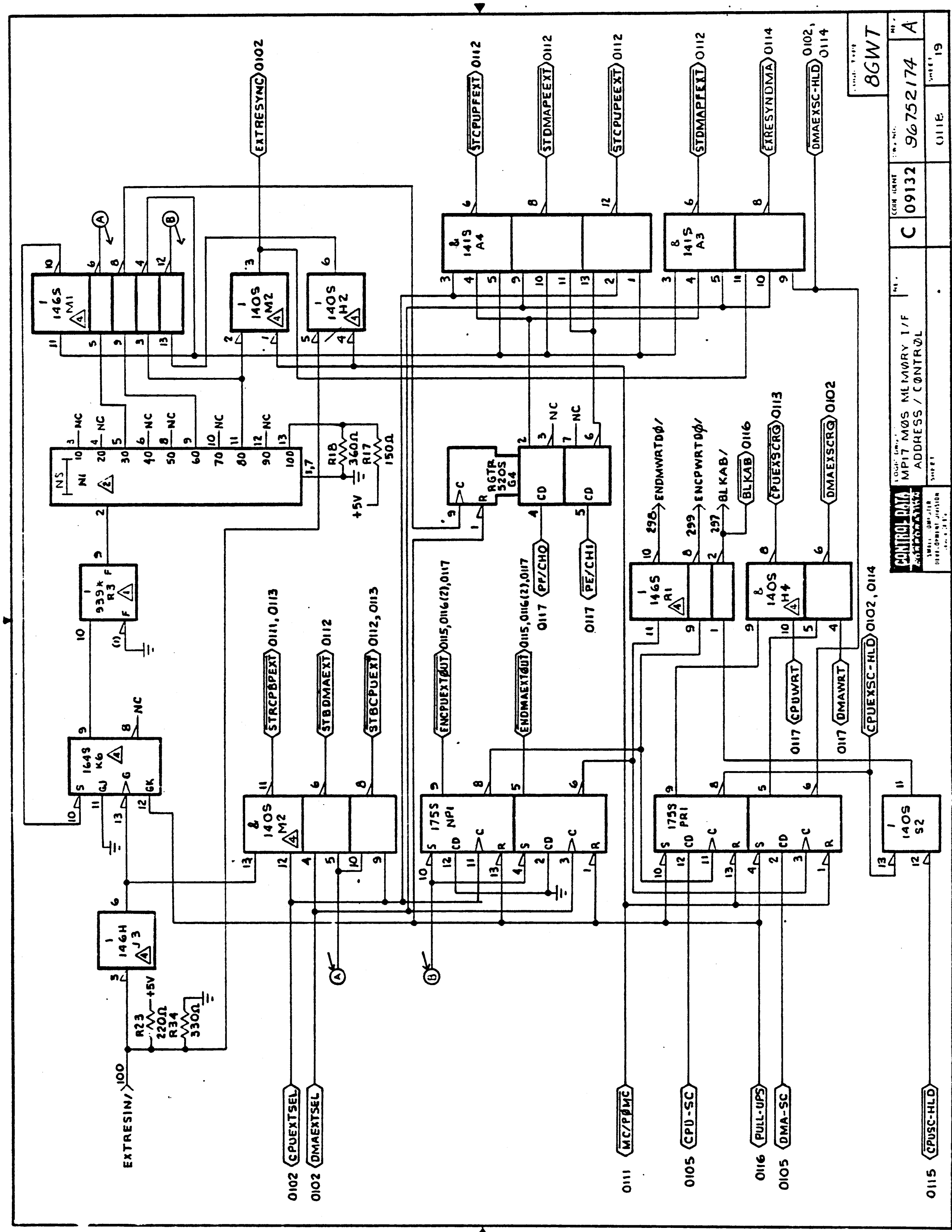

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 19 of 20)

DWN	B. Hodson	2/10/78
CHK		2-16-78
ENG	R. Warner	3-20-78
MFG		3-29-78
APPR		3-29-78

CONTROL DATA CORPORATION

DATA SYSTEMS LA JOLLA DIVISION

LOGIC- MOS MEM I/F ADDR/CONT

8GWT

DR 96752174 A

SHEET 1 OF 1

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS21078	CL. B. PRE-RELEASED	BJ	3-29-78	AW

SHEET REVISION STATUS

NOTES

DETACHED LISTS

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AA9180 REV 8-71

Figure 5-11. MOS Memory Interface Address/Control (PWA 96752173) Logic Diagram (Sheet 20 of 20)

SIGNAL	PIN	CROSS REF NO
BLKAB/	297	0118
CAS/	239	0110
CHAR0	246	0117
CHAR1	269	0105
CHR-0/	289	0105
CHR-1/	290	0105
CH0/PF	89	0114
CH1/PE/	76	0114
CPUBKPWRT	266	0105
CPUMAB12/	268	0108
CPUMAB13/	286	0107
CPUMAB14/	280	0107
CPUMAB15/	293	0107
CPUMAB16/	285	0107
CPUMAB17/	283	0106
CPUMAB18/	17	0113
CPUMDS/	222	0113
CPUNBDS/	45	0117
CPUPROTECT/	248	0117
CPUREQ/	225	0113
CPUWRITE	49	0117
CPUWRTPB	36	0106
CPU-SC/	272	0105
CS/	237	0107
DMACHAR0	230	0105
DMACHAR1	250	0105
DMAMAB01/	37	0109
DMAMAB02/	253	0109
DMAMAB03/	255	0109
DMAMAB04/	256	0109
DMAMAB05/	263	0108
DMAMAB06/	35	0108
DMAMAB07/	277	0108
DMAMAB08/	52	0108
DMAMAB09/	252	0108
DMAMAB10/	261	0108
DMAMAB11/	262	0108
DMAMAB12/	274	0108
DMAMAB13/	292	0107
DMAMAB14/	281	0107
DMAMAB15/	282	0107
DMAMAB16/	271	0107
DMAMAB17/	284	0106
DMAMAE/	18	0113
DMAMDS/	221	0112
DMAMPE/	215	0112
DMAPRØT/	39	0117
DMAREQACT/	296	0104
DMAWRITE	43	0117
DMAWRTPB/	273	0106
DMA1-INT	210	0101
DMA1-MR/	11	0101
DMA1-RA/	227	0101
DMA2-INT	205	0101
DMA2-MR/	214	0101
DMA2-RA/	219	0101
DMA3-INT	243	0101
DMA3-MR/	212	0101
DMA3-RA/	220	0101
DMA4-INT	211	0101
DMA4-MR/	213	0101

SIGNAL	PIN	CROSS REF NO
DMA4-RA/	216	0101
DMA-PF/	228	0112
DMA-SC/	270	0105
ECCHERE/	34	0112
EMPF	47	0117
ENCPWRTDØ/	299	0118
ENDMWRTDØ/	298	0118
ENEXTRDØ/	46	0114
ENMØSWRTD/	217	0112
ENMØS-250	42	0111
ENPRTSYS	247	0105
EXTBANK/	99	0113
EXTIMAB01/	65	0109
EXTIMAB02/	66	0109
EXTIMAB03/	67	0109
EXTIMAB04/	68	0109
EXTIMAB05/	69	0108
EXTIMAB06/	70	0108
EXTIMAB07/	71	0108
EXTIMAB08/	72	0108
EXTIMAB09/	73	0108
EXTIMAB10/	74	0108
EXTIMAB11/	75	0108
EXTIMAB12/	90	0108
EXTIMAB13/	91	0107
EXTIMAB14/	93	0107
EXTIMAB15/	94	0107
EXTIMAB16/	95	0107
EXTIMAB17/	96	0106
EXTØMAB01/	53	0116
EXTØMAB02/	54	0116
EXTØMAB03/	55	0116
EXTØMAB04/	56	0116
EXTØMAB05/	57	0116
EXTØMAB06/	58	0116
EXTØMAB07/	59	0116
EXTØMAB08/	60	0116
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EXTØMAB10/	62	0116
EXTØMAB11/	63	0116
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EXTØMAB13/	79	0115
EXTØMAB14/	81	0115
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EXTØMAB17/	84	0115
EXTREQACT/	295	0104
EXTREQIN/	92	0103
EXTREQØUT/	80	0114
EXTRESIN/	100	0118
EXTRESØUT/	88	0114
EXTWPBIN	97	0106
EXTWPBØUT	85	0117
EXTWRTIN	98	0106
EXTWRTØUT	86	0117
EIGKN0-1/	203	0106
EIGKN0-2/	207	0106
EIGKN0-3/	206	0106
EIGKN0-4/	209	0106
EIGKN1-1/	[illegible]	0106
EIGKN1-2/	[illegible]	0106

SIGNAL	PIN	CROSS REF NO
EIGKN1-3/	25	0106
EIGKN1-4/	27	0106
GATE AB/	294	0116
GND	4	0117
GND	101	0117
GND	102	0117
GND	204	0117
GND	234	0117
GND	245	0117
GND	251	0117
GND	254	0117
GND	301	0117
GND	302	0117
GND	87	0117
MCTM/	279	0102
MC/	51	0111
MØSMA00	258	0109
MØSMA01	257	0109
MØSMA02	260	0109
MØSMA03	259	0109
MØSMA04	265	0109
MØSMA05	264	0109
MPB-L	20	0105
MPB/PRF	240	0117
MPE+DED/	21	0113
MP/SC	44	0117
PE//CH1	64	0117
PF/CH0	77	0117
POWERFAIL/	48	0110
PRF/MPB	288	0105
PRIØRITY	218	0101
RASIGK0-1/	236	0106
RASIGK0-2/	32	0106
RASIGK0-3/	33	0106
RASIGK0-4/	232	0106
RASIGK1-1/	244	0106
RASIGK1-2/	30	0106
RASIGK1-3/	233	0106
RASIGK1-4/	31	0106
RDØPAGE/	249	0117
SC/MPL	287	0105
SELCPUEXT/	6	0111
SELCPUINT/	223	0111
SETSMI05/	7	0112
SETSMI08/	14	0112
SLTBLK0/	238	0107
SLTBLK1/	235	0107
SLTBLK2/	241	0107
SLTBLK3/	242	0107
STBCPUBKP/	13	0113
STBCPUDFM/	8	0112
STBDFM/	10	0112
STBDMADFM/	9	0112
STCP/EXD/	224	0110
S305/	41	0116
S306/	40	0116
S307/	38	0116
S308/	23	0116
S309/	28	0116
S310/	24	0116
S311/	22	0116

SIGNAL	PIN	CROSS REF NO
S312/	29	0116
S313/	72	0116
S314/	15	0116
S315/	5	0116
TO/	50	0114
TO-MEM/	275	0110
T2-ØDDCLK	267	0114
T3-MEM/	19	0114
WRT-MPF/	16	0113
WRT-PB/	291	0106
WT-MOS/	231	0112
+5V	1	0117
+5V	2	0117
+5V	201	0117
+5V	202	0117
+5V BB	3	0117
+5V BB	203	0117

NOTES: UNLESS OTHERWISE SPECIFIED

△ IC TO BE CONNECTED TO +5VBB.

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS19373	[illegible]	BR	6-7-81	AW
B	DS22260	SEE ECO	J.V.W.	11-1-82	AW
C	DS22294	ADDED NEW CARD TYPE. CHG'D SHTS 2,4,6,7,8,12, 13,14,15 & 18. CORRECTED CLERICAL ERRORS ONLY	J.V.W.	7-29-83	AW

83RNT

LOGIC TYPE 81PUT / 82RHT

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037

TITLE: MEMORY INTERFACE ADDRESS

BA212 A

DR	[illegible]	3-2-82
CHK	[illegible]	3/2/82
ENGR	[illegible]	5/21/82
MFG		
APPD	[illegible]	6-7-81

C | CODE IDENT NO 09132 | DRAWING NUMBER 96890851

96890552 | SHEET 1 OF 19

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 1 of 19)

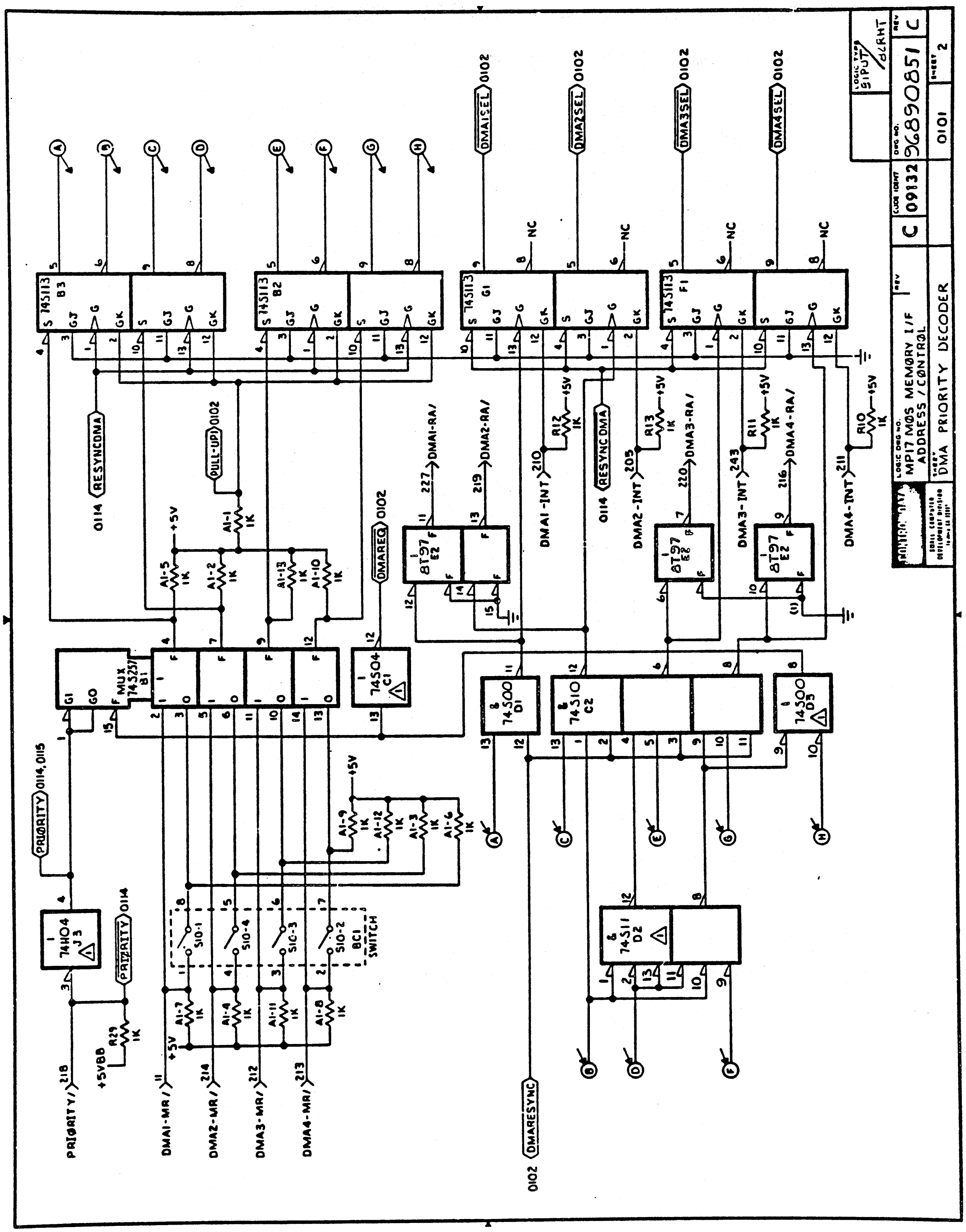

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 2 of 19)

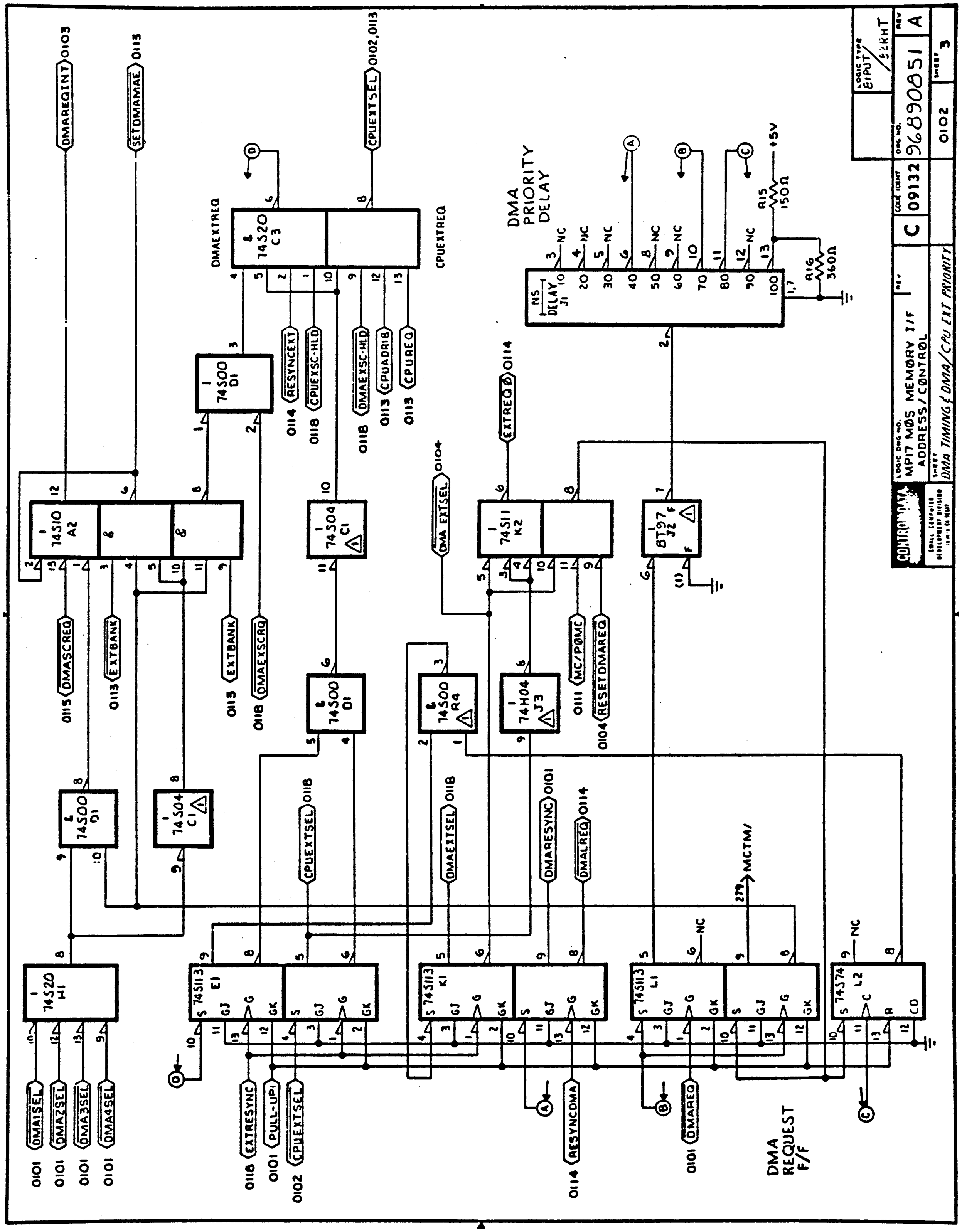

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 3 of 19)

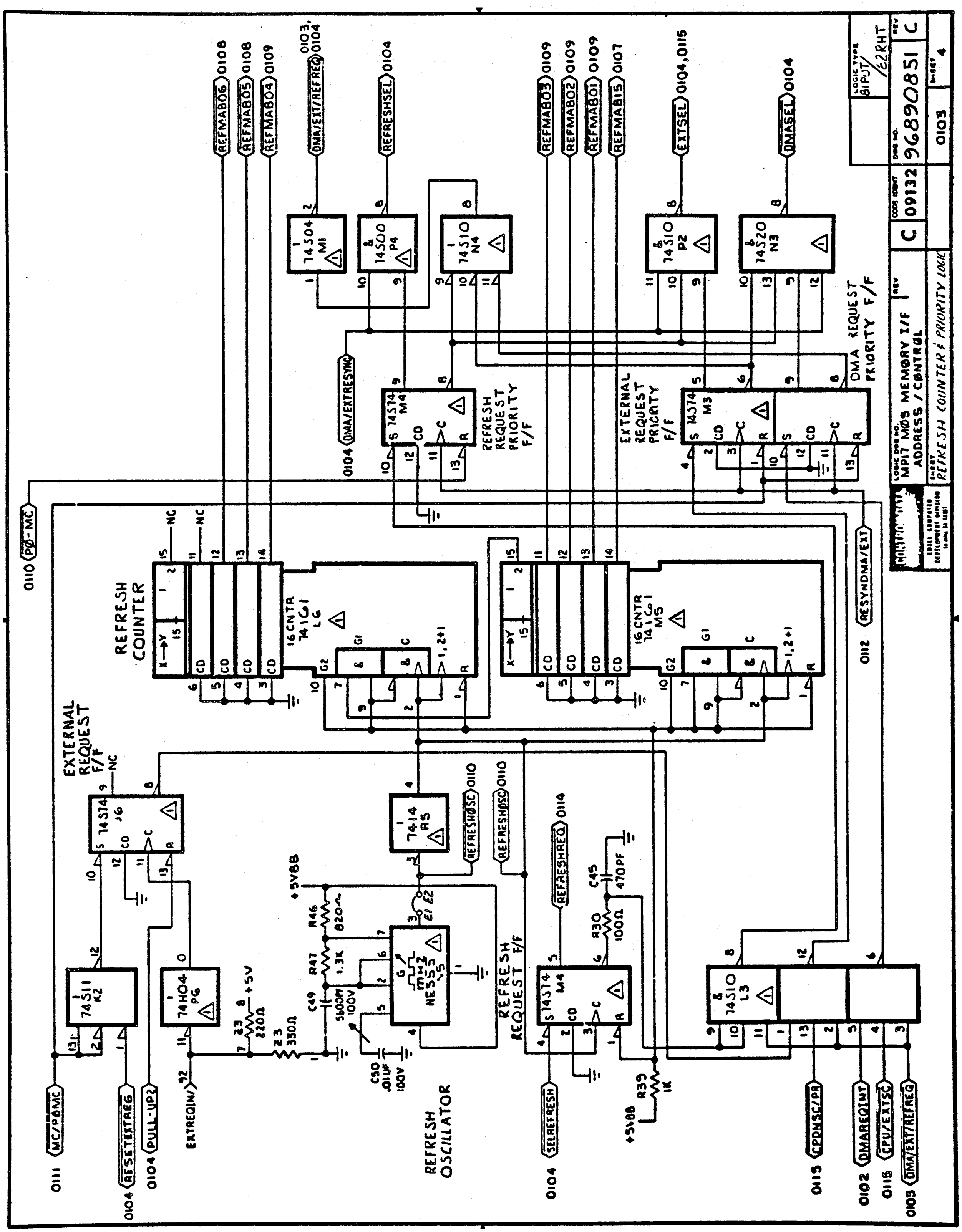

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 4 of 19)

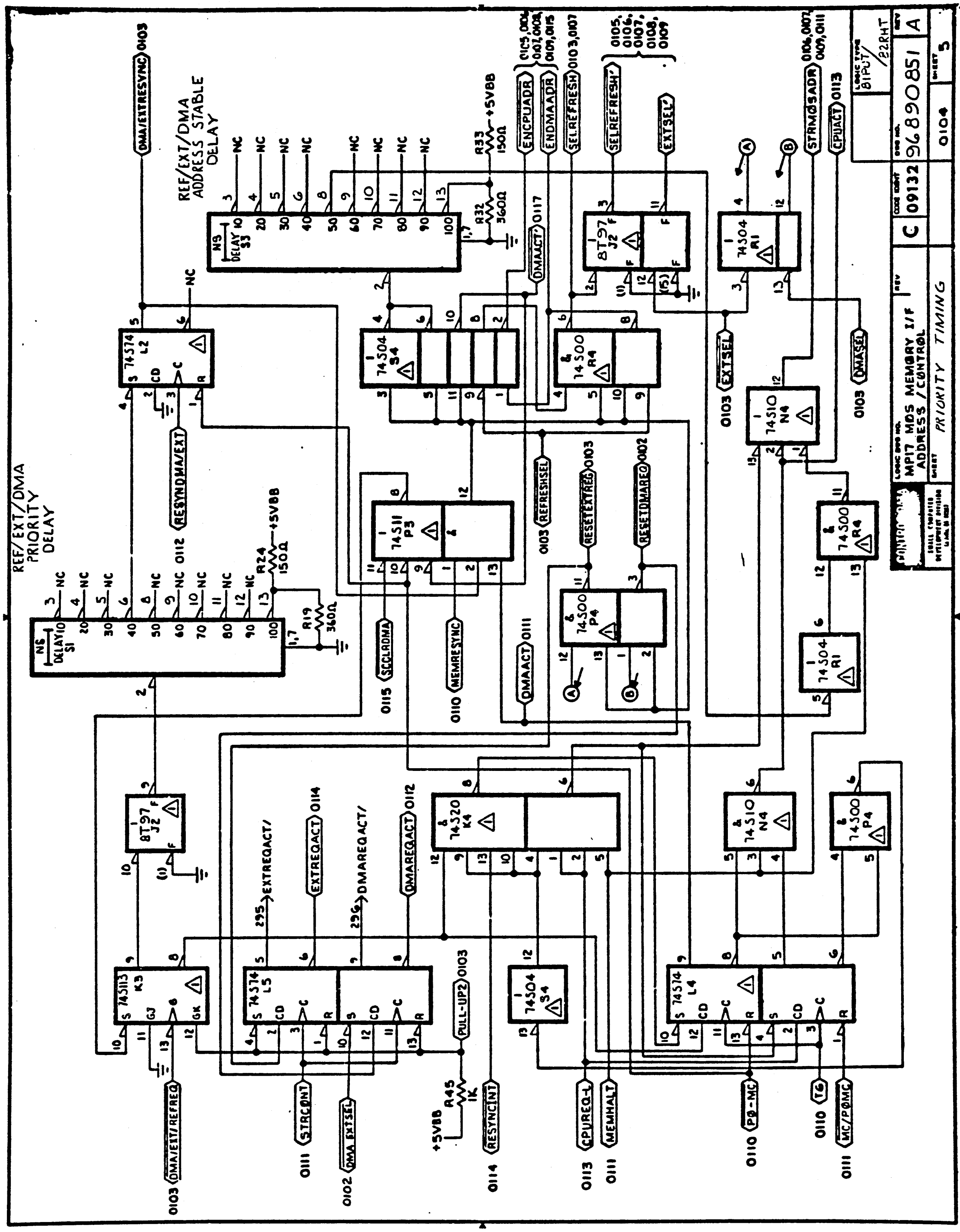

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 5 of 19)

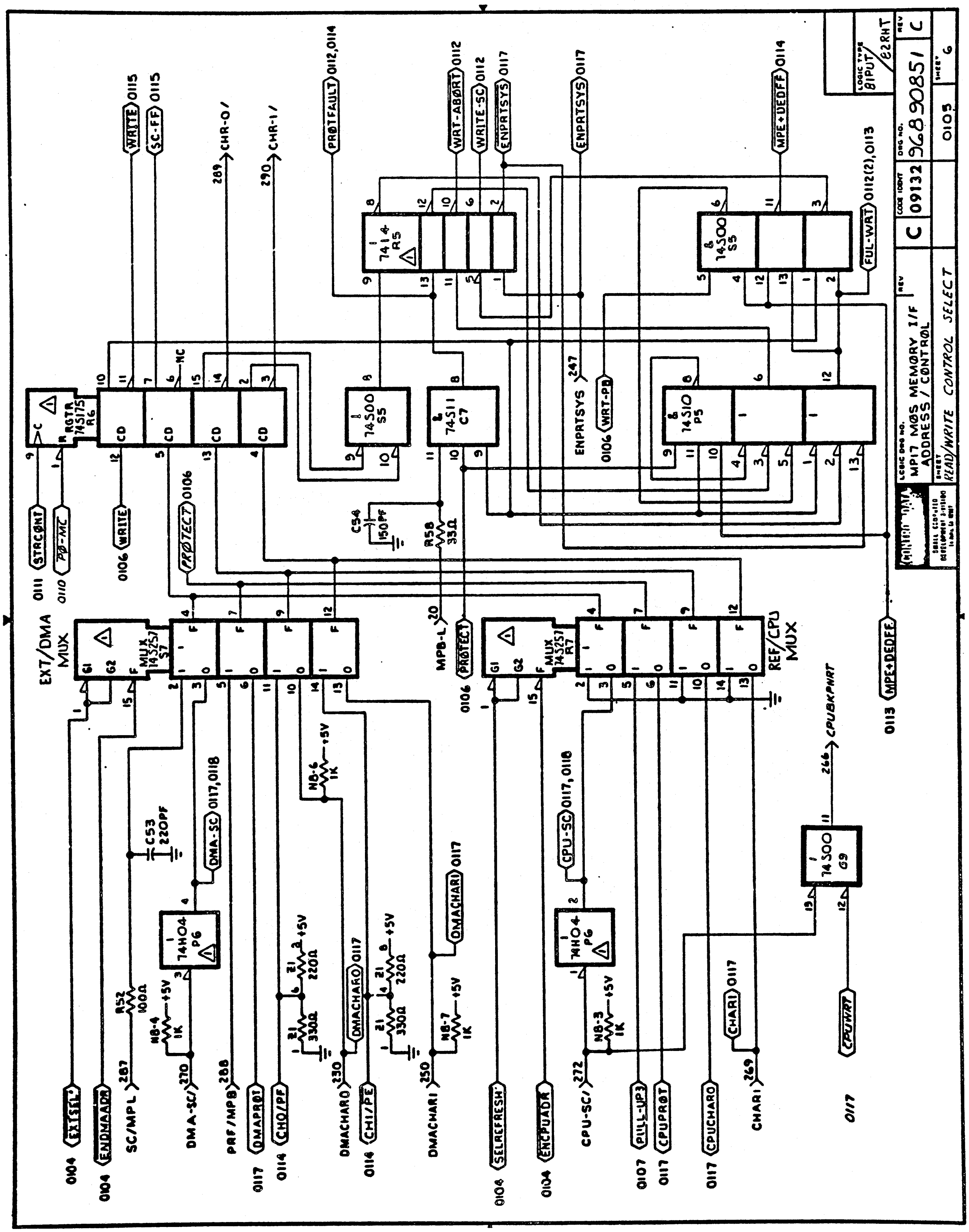

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 6 of 19)

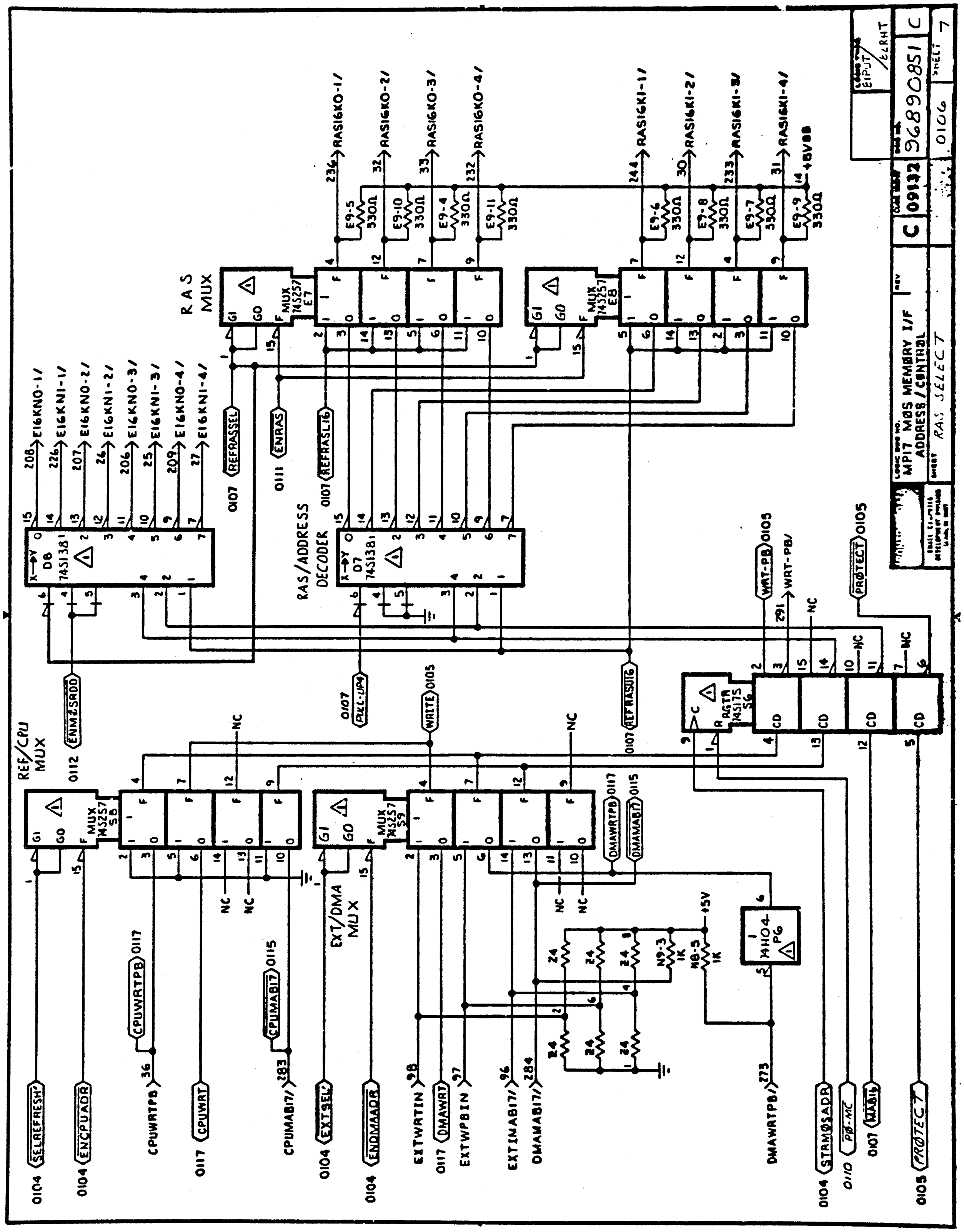

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 7 of 19)

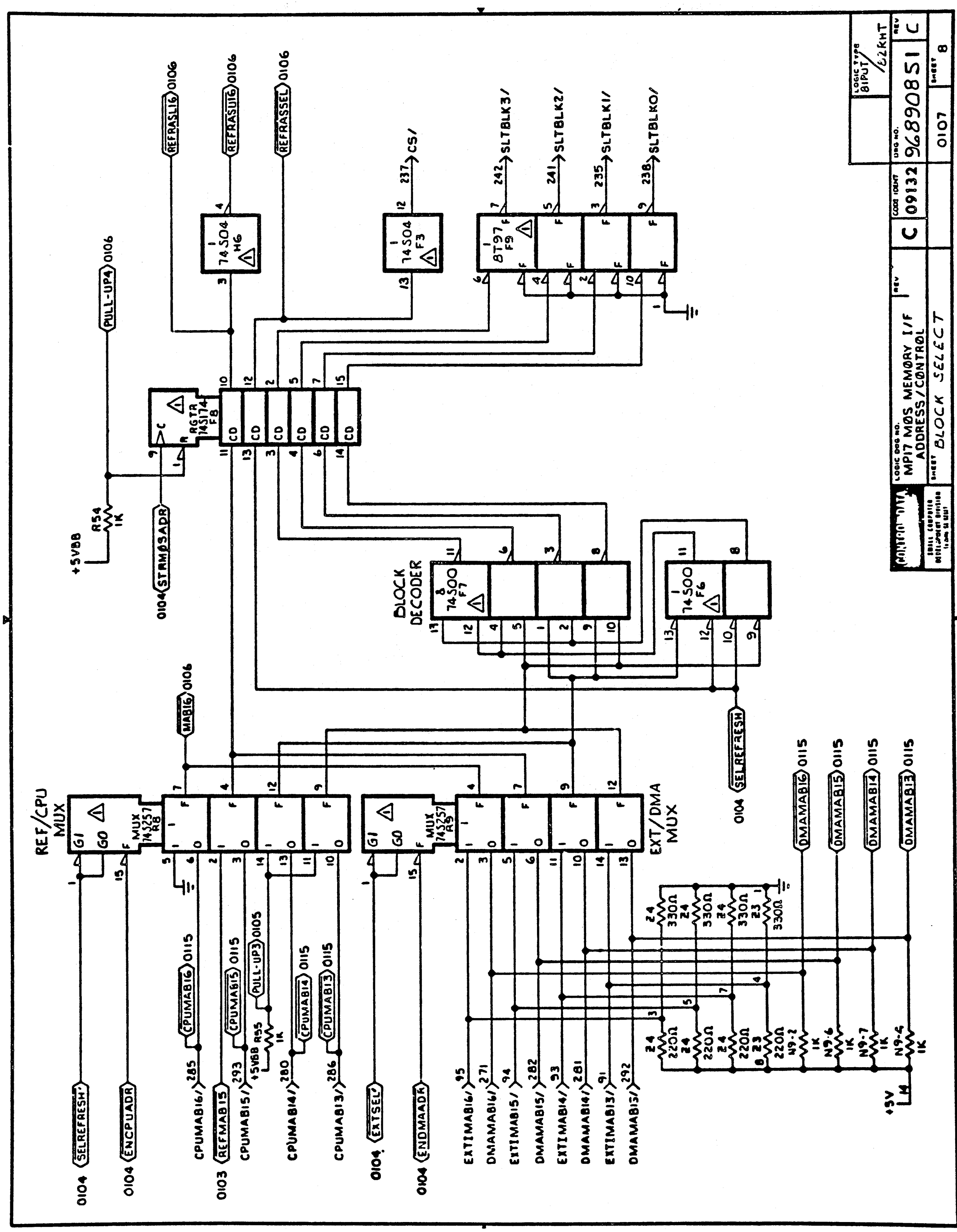

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 8 of 19)

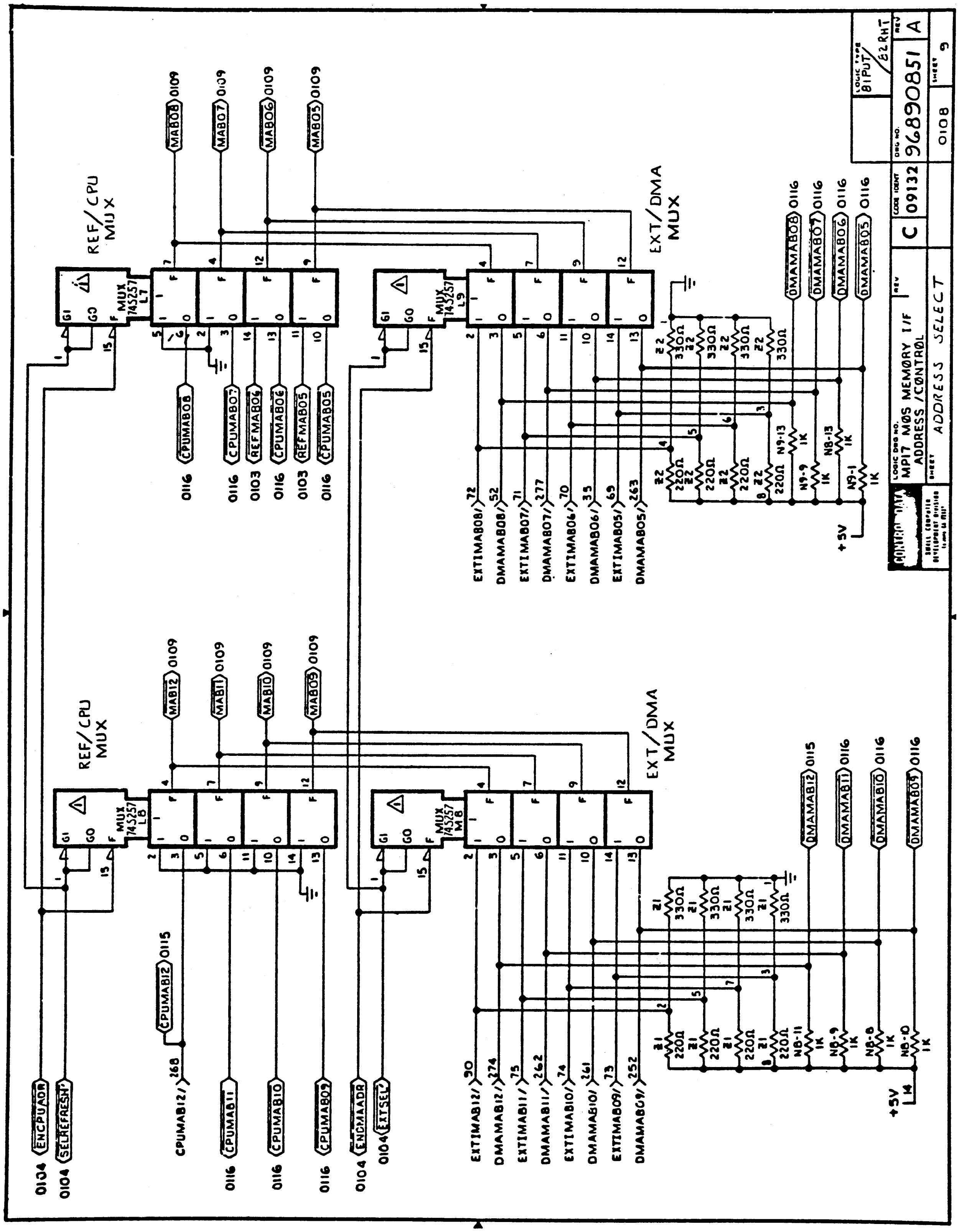

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 9 of 19)

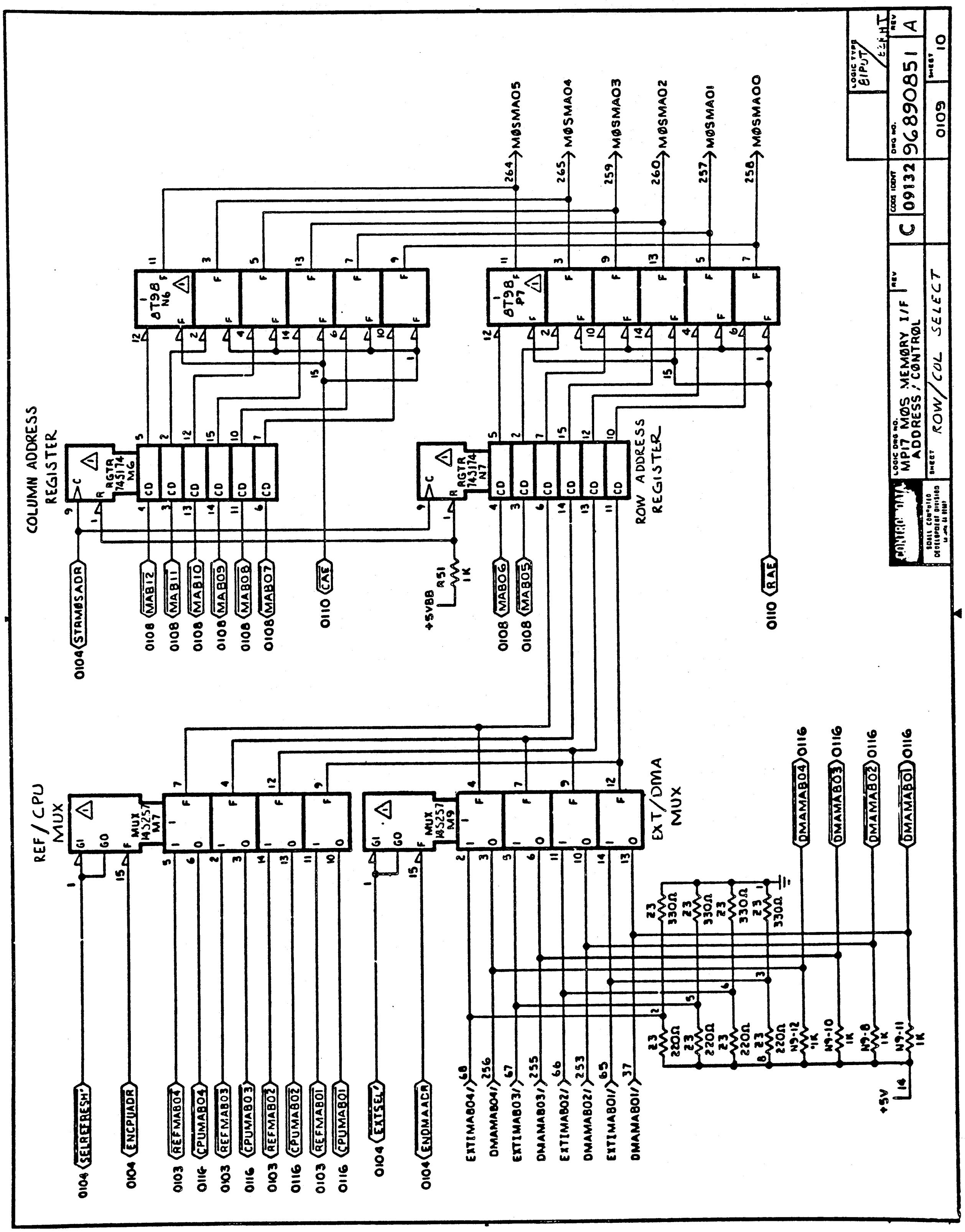

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 10 of 19)

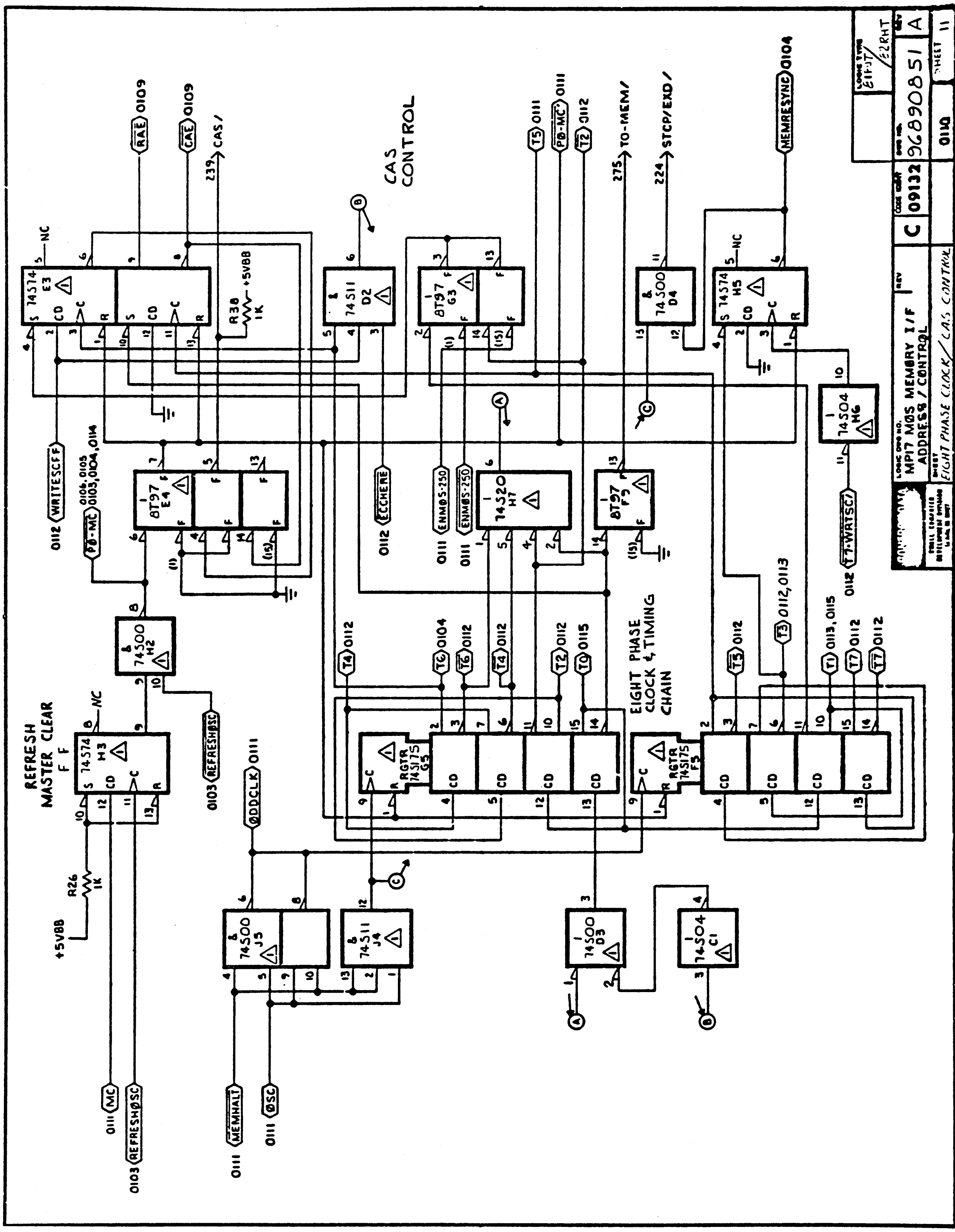

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 11 of 19)

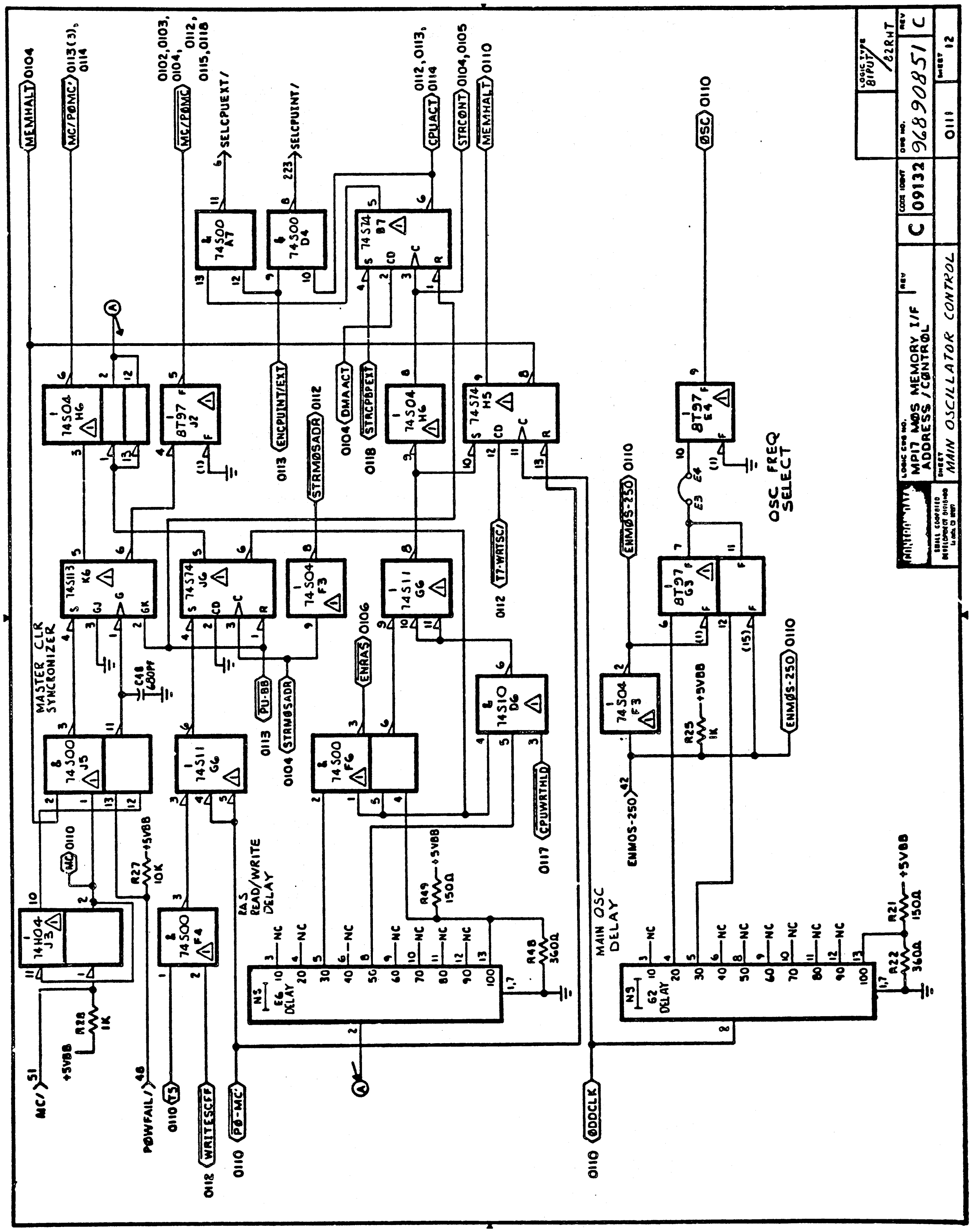

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 12 of 19)

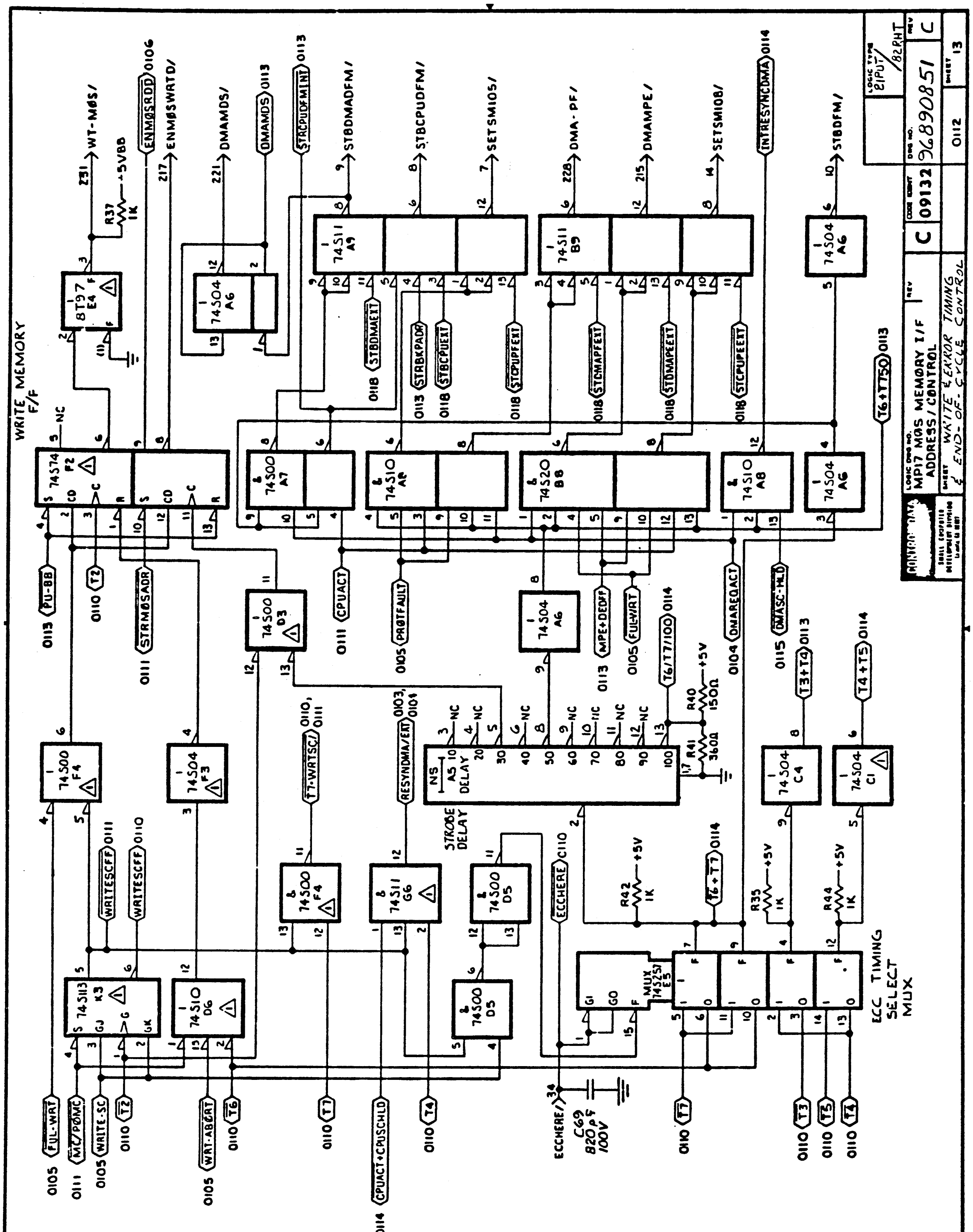

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 13 of 19)

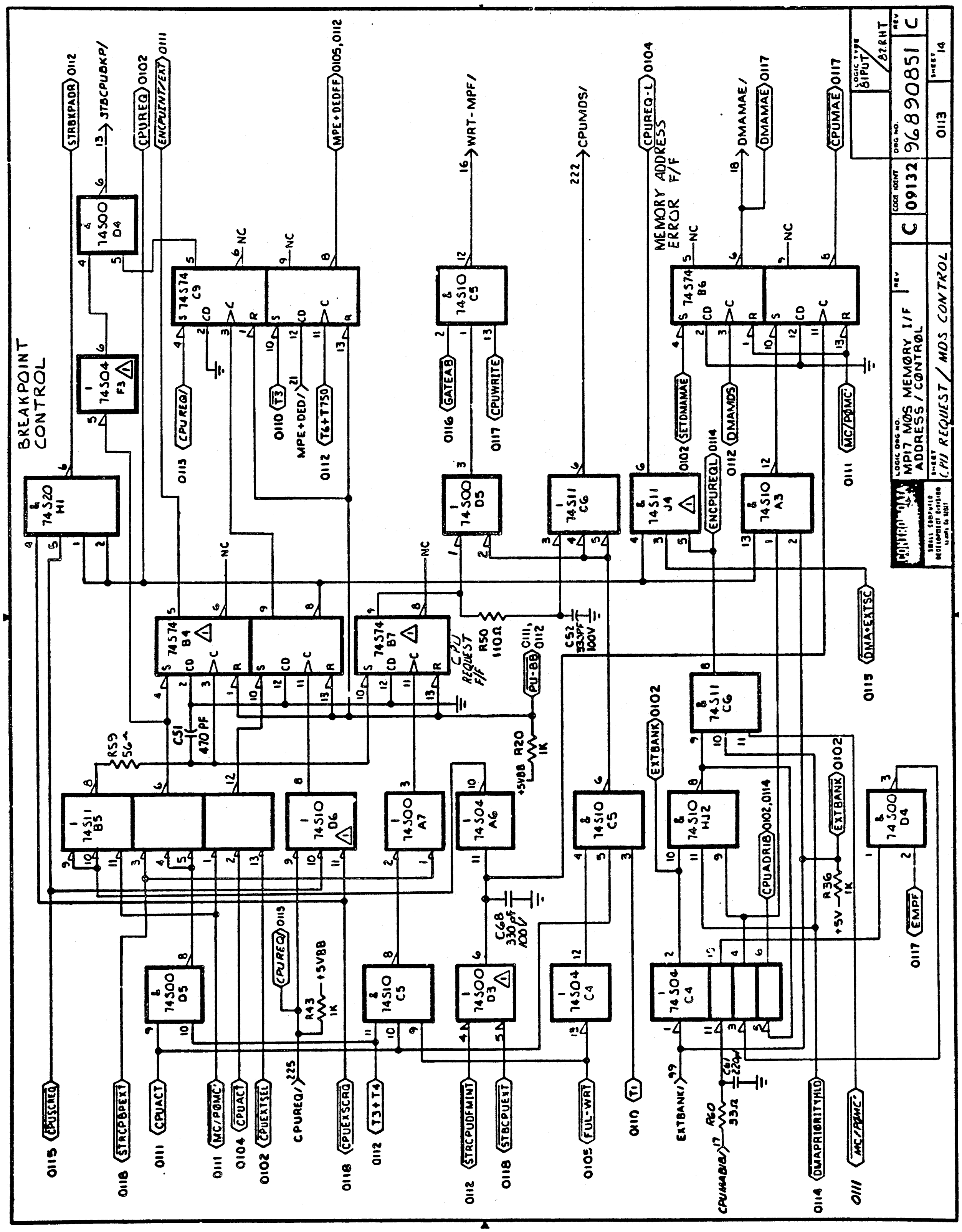

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 14 of 19)

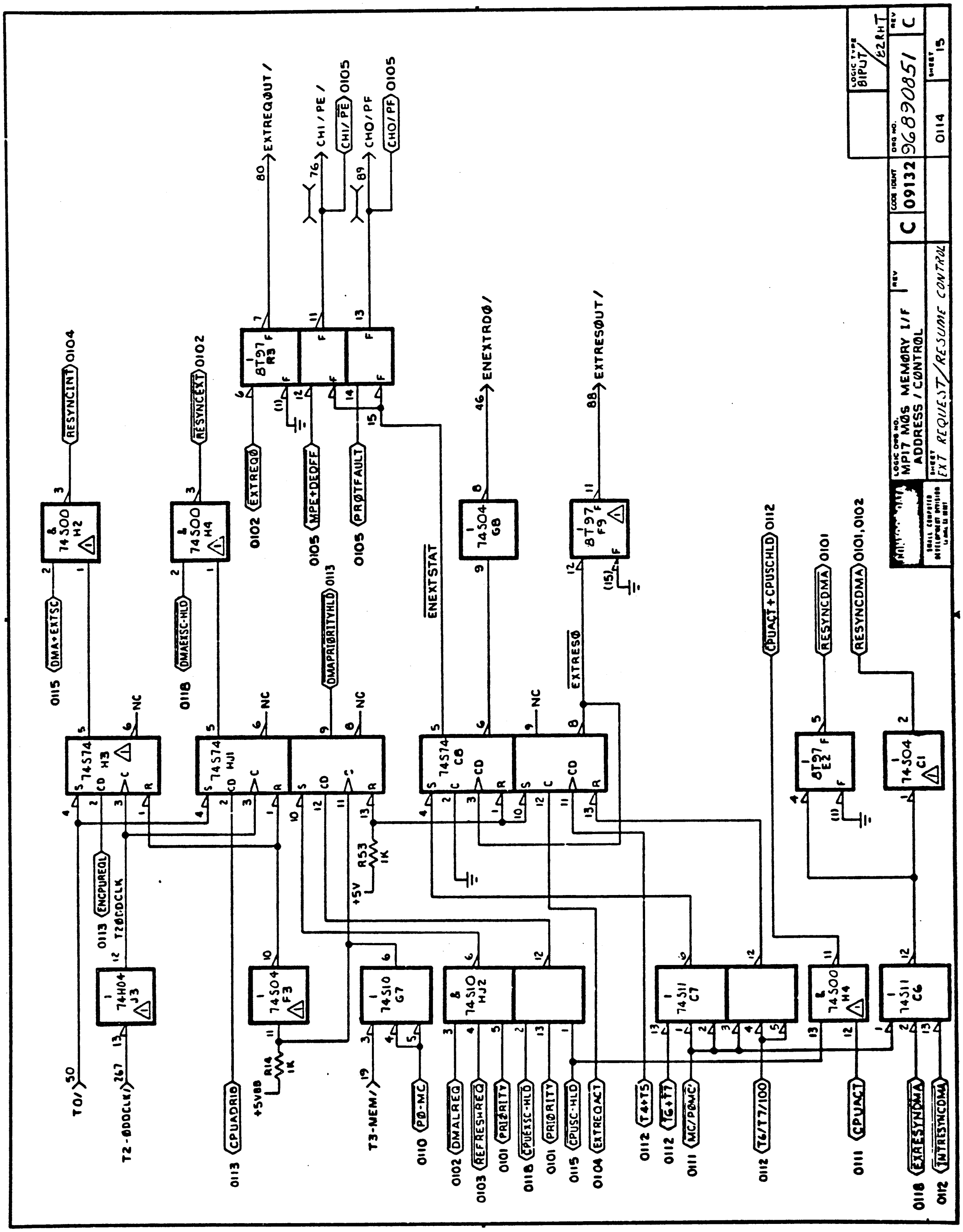

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 15 of 19)

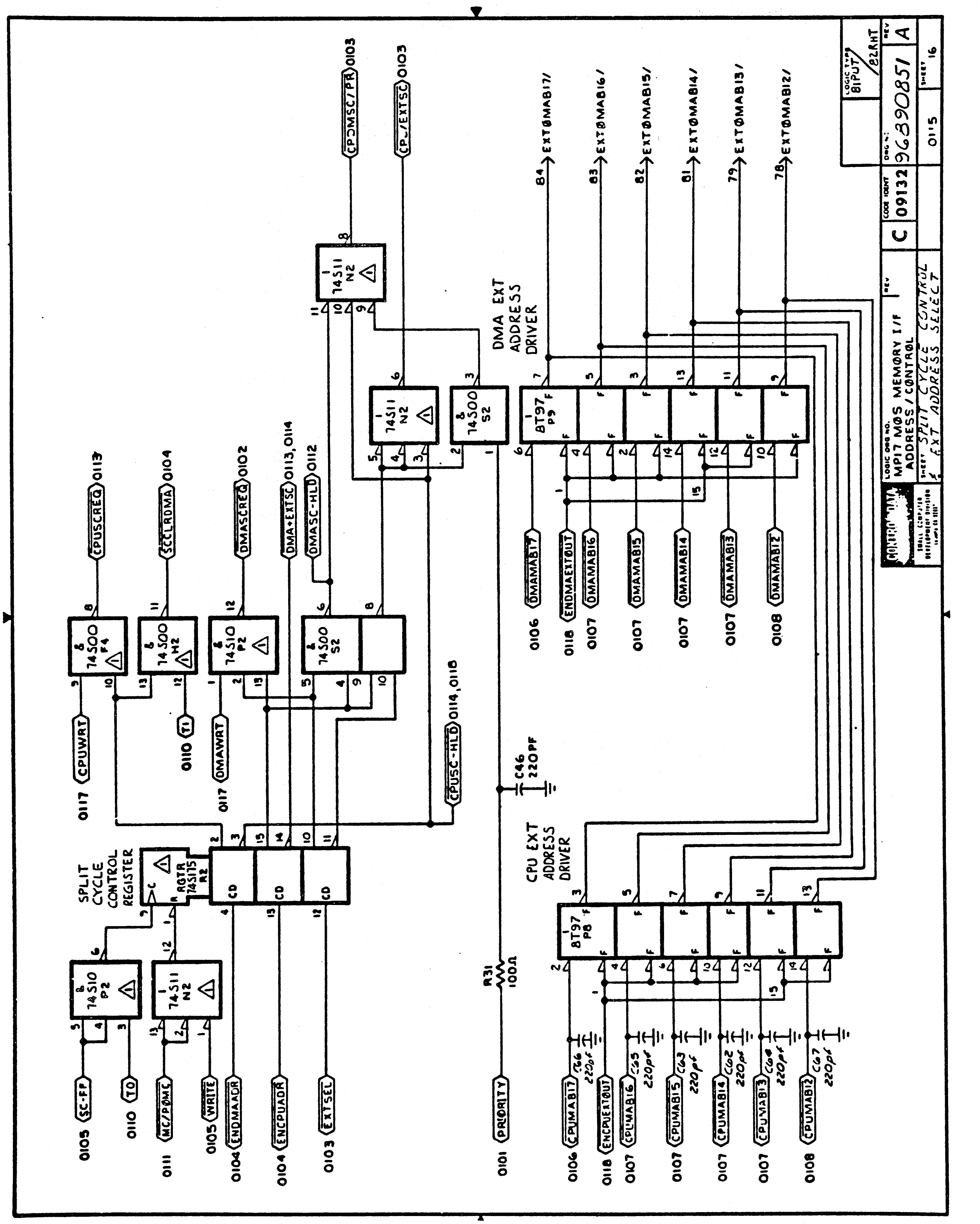

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 16 of 19)

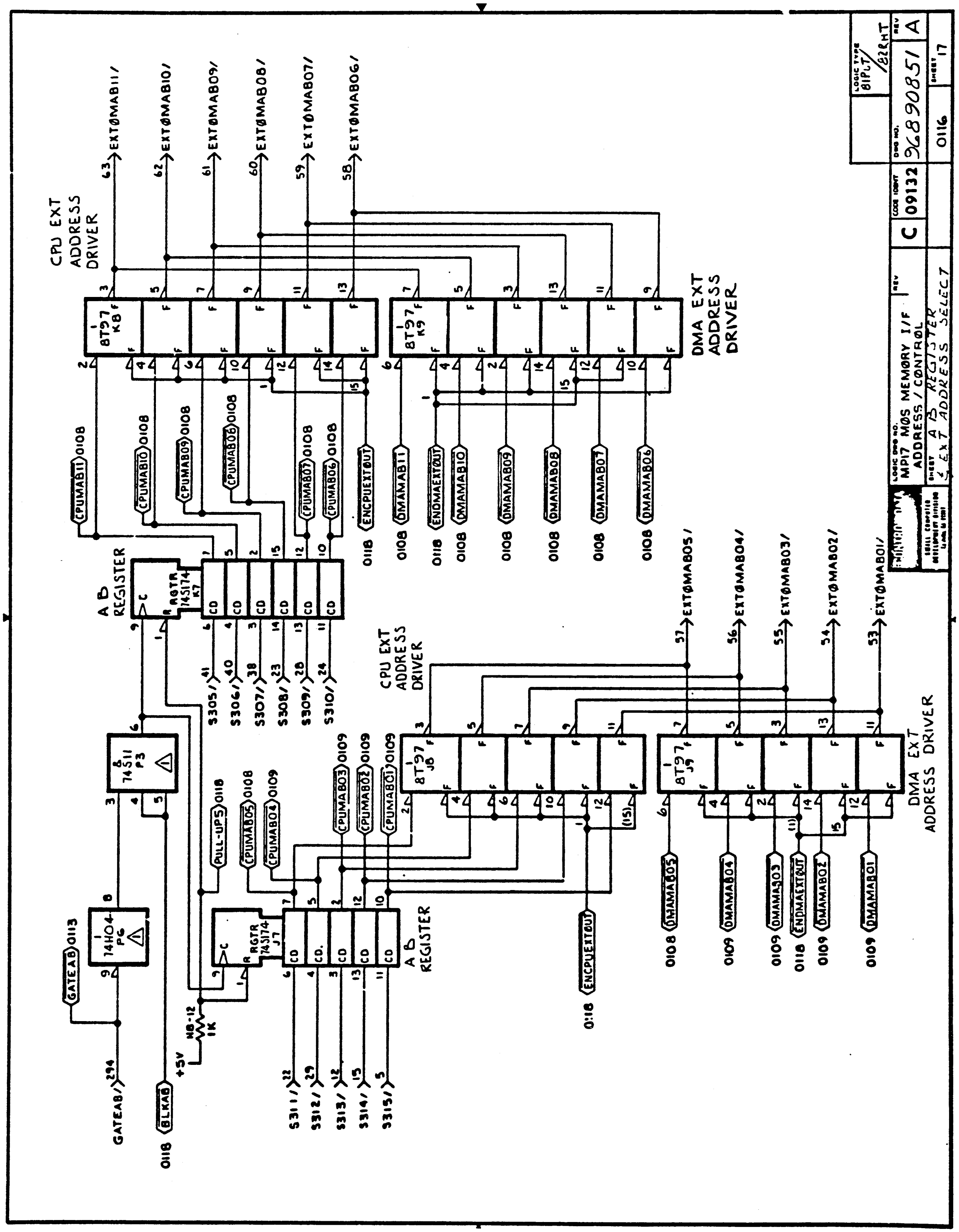

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 17 of 19)

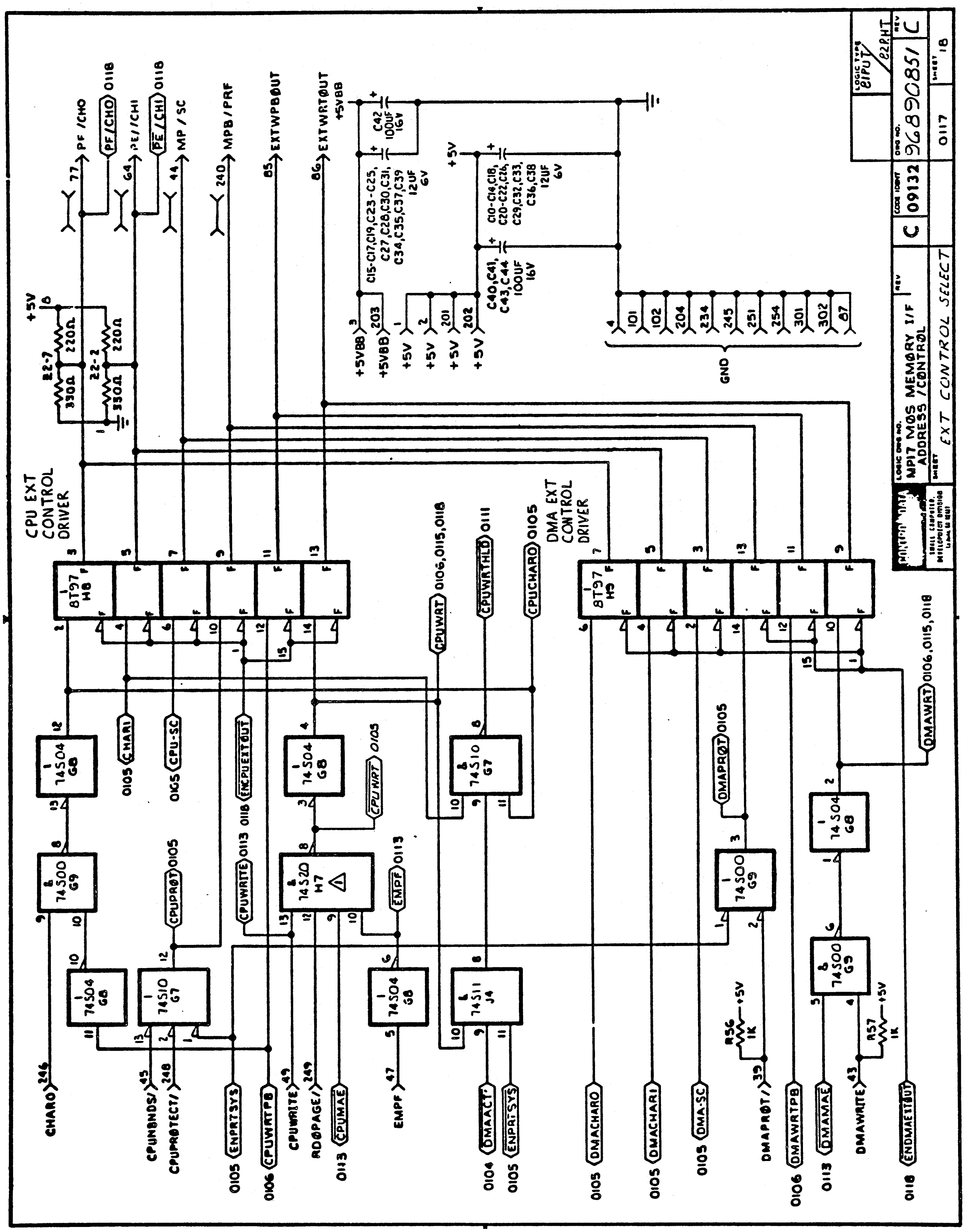

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 18 of 19)

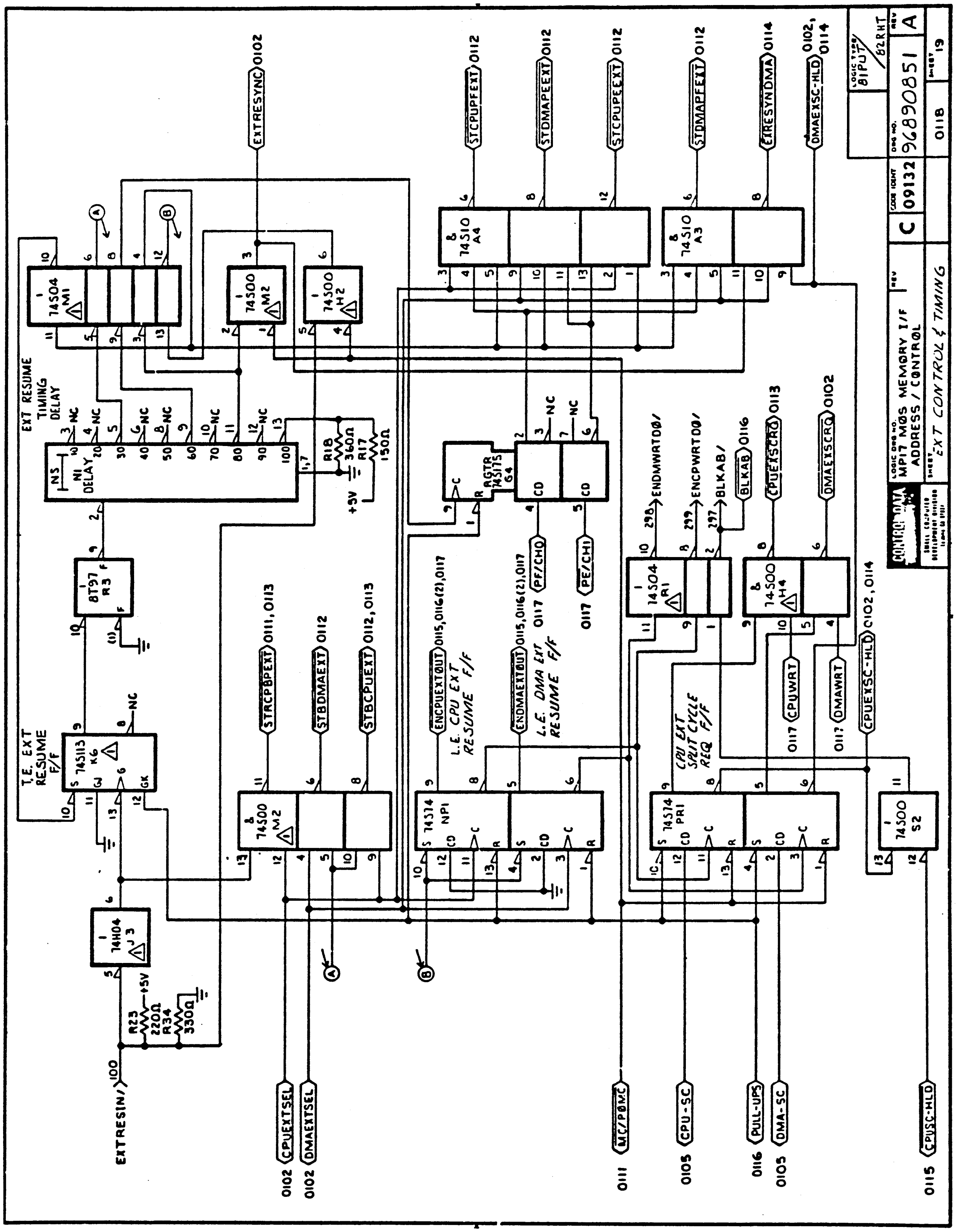

Figure 5-12. MOS Memory Interface Address (PWAs 96890551, 96890552 and 96890630) Logic Diagram (Sheet 19 of 19)

SIGNAL	PIN	CROSS REF NO
BLKAB/	229	0101
BUS 00	92	0120
BUS 01	94	0120
BUS 02	95	0120
BUS 03	91	0120
BUS 04	295	0120
BUS 05	43	0120
BUS 06	44	0120
BUS 07	57	0120
BUS 08	84	0120
BUS 09	97	0120
BUS 10	64	0120
BUS 11	296	0120
BUS 12	89	0120
BUS 13	99	0120
BUS 14	10	0120
BUS 15	283	0120
CHR-0/	80	0109
CHR-1/	278	0109
CPUDFM01	71	0119
CPUDFM02	73	0119
CPUDFM03	66	0119
CPUDFM04	77	0119
CPUDFM05	63	0119
CPUDFM06	65	0119
CPUDFM07	267	0119
CPUDFM08	65	0119
CPUDFM09	86	0119
CPUDFM10	291	0119
CPUDFM11	260	0119
CPUDFM12	58	0119
CPUDFM13	259	0119
CPUDFM14	266	0119
CPUDFM15	275	0119
CPUDFM16	276	0119
CPUNBNDS/	216	0106
CPUMAB 12/	50	0103
CPUMAB 13/	48	0103
CPUMAB 14/	49	0103
CPUMAB 15/	51	0103
CPUMAB 16/	270	0103
CPUMAB 17/	26	0103

SIGNAL	PIN	CROSS REF NO
CPUMAB 18/	68	010
CS/	239	0114
DMAD01/	76	0116
DMAD02/	261	0116
DMAD03/	31	0116
DMAD04/	228	0116
DMAD05/	255	0116
DMAD06/	252	0116
DMAD07/	42	0116
DMAD08/	258	0116
DMAD09/	257	0116
DMAD10/	37	0116
DMAD11/	45	0116
DMAD12/	60	0116
DMAD13/	62	0116
DMAD14/	61	0116
DMAD15/	59	0116
DMAD16/	52	0116
DMADFM01	264	0121
DMADFM02	241	0121
DMADFM03	5	0121
DMADFM04	47	0121
DMADFM05	14	0121
DMADFM06	32	0121
DMADFM07	17	0121
DMADFM08	30	0121
DMADFM09	16	0121
DMADFM10	8	0121
DMADFM11	18	0121
DMADFM12	265	0121
DMADFM13	12	0121
DMADFM14	67	0121
DMADFM15	21	0121
DMADFM16	34	0121
DMAMPB/	46	0121
DMAMPL/	259	0121
DMAREQACT/	78	0109
ECC 00	87	0113
ECC 01	285	0113
ECC 02	288	0113
ECC 03	90	0113
ECC 04	289	0113

SIGNAL	PIN	CROSS REF NO
ECC HERE/	83	0112
EMPF	298	0101
ENCPWRTDØ/	227	0106
ENDMWRTDØ/	36	0106
ENEXTRDØ/	19	0118
ENMEMBUS/	98	0120
ENMØSWRTD/	284	0109
ENPATSYS	93	0114
EVENPAR	100	0119
EXTREQACT/	79	0109
GATEAB/	205	0101
GATELBDS/	53	0101
GATEUBDS/	215	0101
GND	4	0109
GND	101	0109
GND	102	0109
GND	204	0109
GND	251	0109
GND	254	0109
GND	301	0109
GND	302	0109
MC/	56	0101
MD00	255	0110
MD01	268	0110
MD02	269	0110
MD03	256	0110
MD04	280	0110
MD05	277	0110
MD06	271	0110
MD07	263	0110
MD08	272	0110
MD09	274	0110
MD10	281	0110
MD11	273	0110
MD12	293	0110
MD13	290	0110
MD14	286	0110
MD15	287	0110
MEMPAØTBT/	70	0119
MIR 28'	9	0101
MIR 29'	300	0101
MIR 30'	7	0101

SIGNAL	PIN	CROSS REF NO
MIR 31'	11	0101
MPAR	85	0114
MPB-L	72	0115
MPB/PRF	250	0109
MPE+DED/	292	0113
MPL/SC	249	0109
MPRØT	82	0114
MULTIND	13	0102
PAGE MØDE/	3	0101
PGM FILES/	203	0101
PRF/MPB	226	0110
RDØ PAGE/	240	0101
RØP INT/	20	0101
S300/	54	0102
S301/	56	0102
S302/	55	0102
S303/	53	0102
S304/	39	0102
S305/	41	0102
S306/	40	0102
S307/	38	0102
S308/	23	0102
S309/	28	0102
S310/	24	0102
S311/	22	0102
S312/	29	0102
S313/	35	0102
S314/	15	0102
S315/	27	0102
SC/MPL	225	0110
SEC STATUS/	294	0118
SELCPUEXT/	74	0117
SELCPUINT/	75	0117
STBCPUDFM/	88	0119
STBDFM/	81	0115
STBDMADFM/	6	0121
STCP/EXD/	262	0108
TO'/	25	0101
TO-MEM/	257	0106
WRT-MPF/	217	0101
WRT-PB/	282	0109
XI01	209	0110

SIGNAL	PIN	CROSS REF NO
XI02	208	0110
XI03	207	0110
XI04	206	0110
XI05	211	0110
XI06	213	0110
XI07	218	0110
XI08	214	0110
XI09	212	0110
XI10	210	0110
XI11	220	0110
XI12	222	0110
XI13	224	0110
XI14	223	0110
XI15	221	0110
XI16	219	0110
XØ01	233	0109
XØ02	232	0109
XØ03	231	0109
XØ04	230	0109
XØ05	235	0109
XØ06	237	0109
XØ07	242	0109
XØ08	238	0109
XØ09	236	0109
XØ10	234	0109
XØ11	244	0108
XØ12	246	0108
XØ13	248	0108
XØ14	247	0108
XØ15	245	0108
XØ16	243	0108
+5V	1	0109
+5V	2	0109
-5V	201	0109
+5V	202	0109

7. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S257.

6. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S253.

5. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S138.

4. 8T98 IS SIMILAR TO 939

3. 74S258 IS SIMILAR TO 74S257.

2. NO ELEMENT IDENTIFIER AVAILABLE FOR 82S09.

1. 8T97 IS SIMILAR TO 939.

8. CAPACITOR PROVISIONAL *NOT ON PWA

NOTES UNLESS OTHERWISE SPECIFIED

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

CONTROL DATA — SMALL COMPUTER DEVELOPMENT DIVISION

TITLE: LOGIC DIAGRAM - MOS MEMORY INTERFACE (DATA)

LOGIC TYPE: 7FWT

C | CODE IDENT NO 09132 | DRAWING NUMBER 96752105 | REV A

SHEET 1 OF 22

PWA NO 96752104 | PWB NO 96740700

DR 5012562105 DETACHED LIST

APPD A. Welch 11-9-77

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 1 of 23)

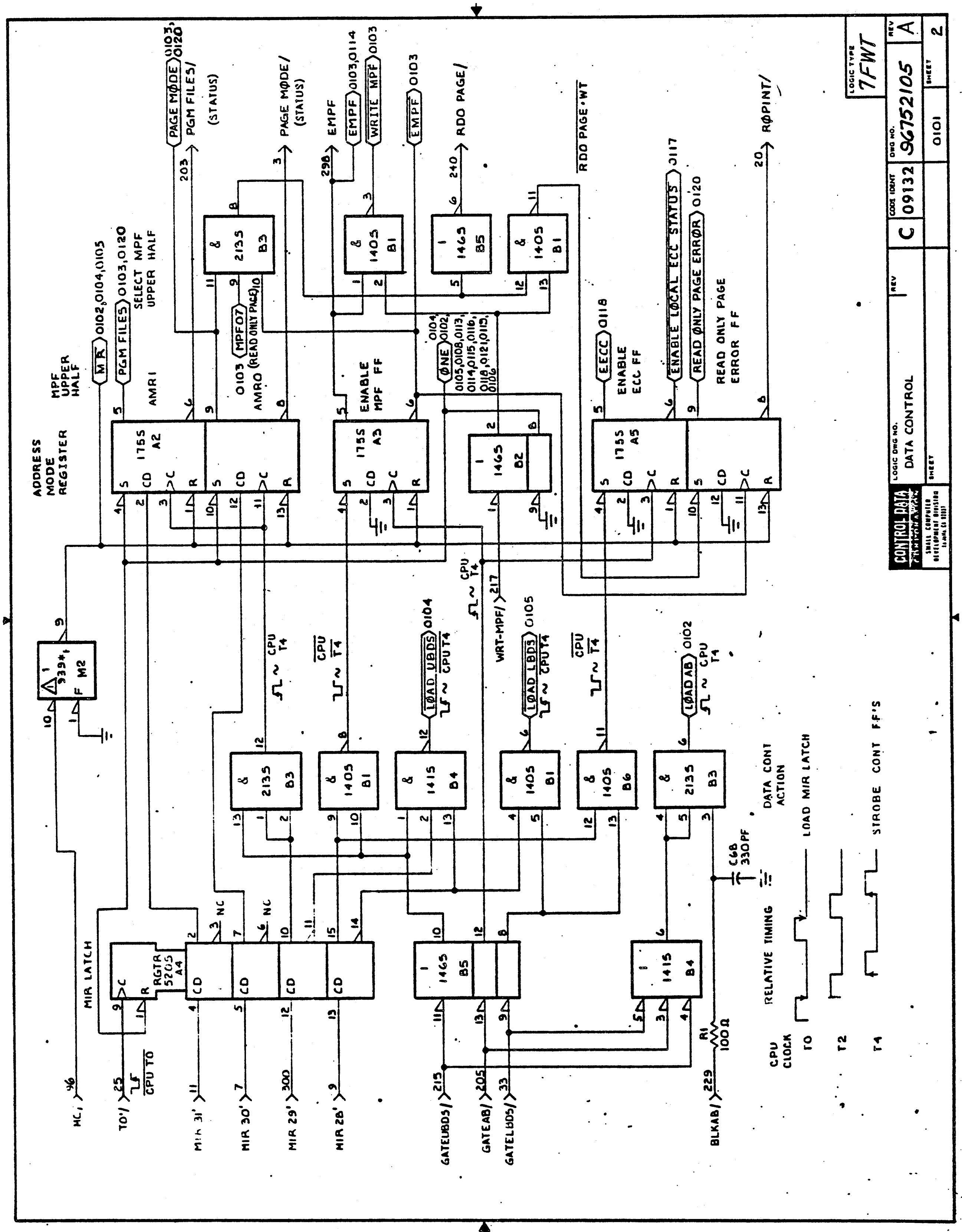

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 2 of 23)

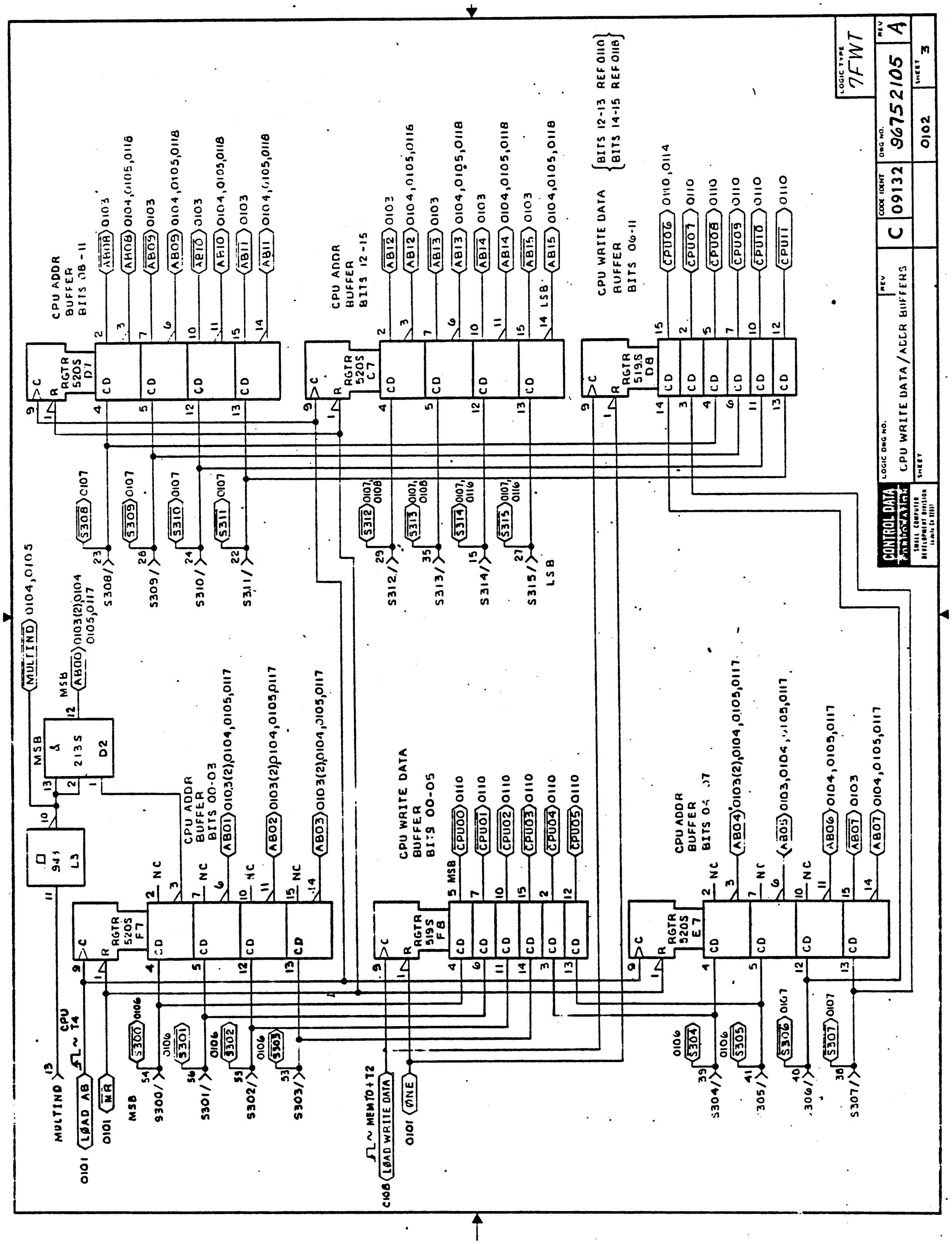

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 3 of 23)

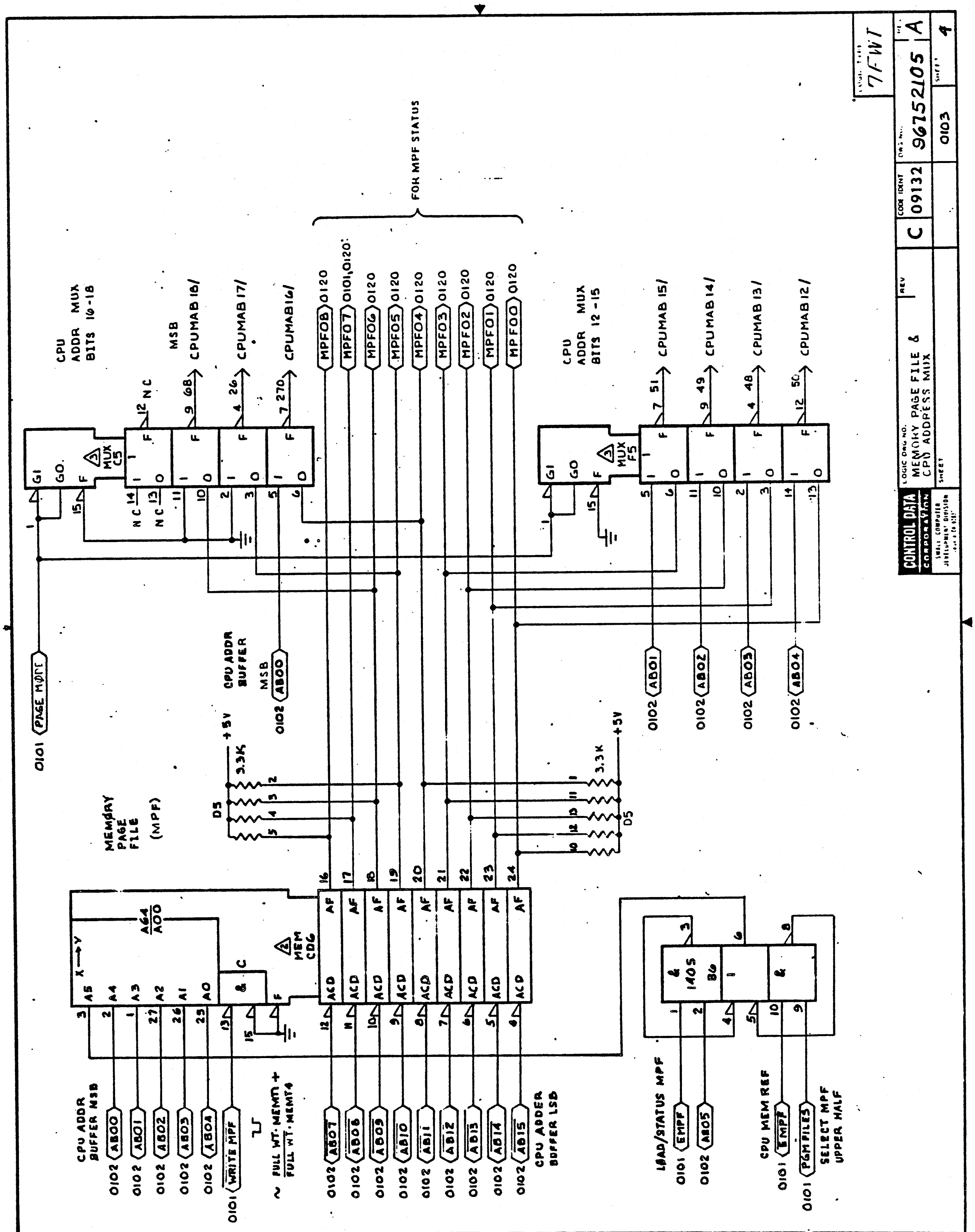

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 4 of 23)

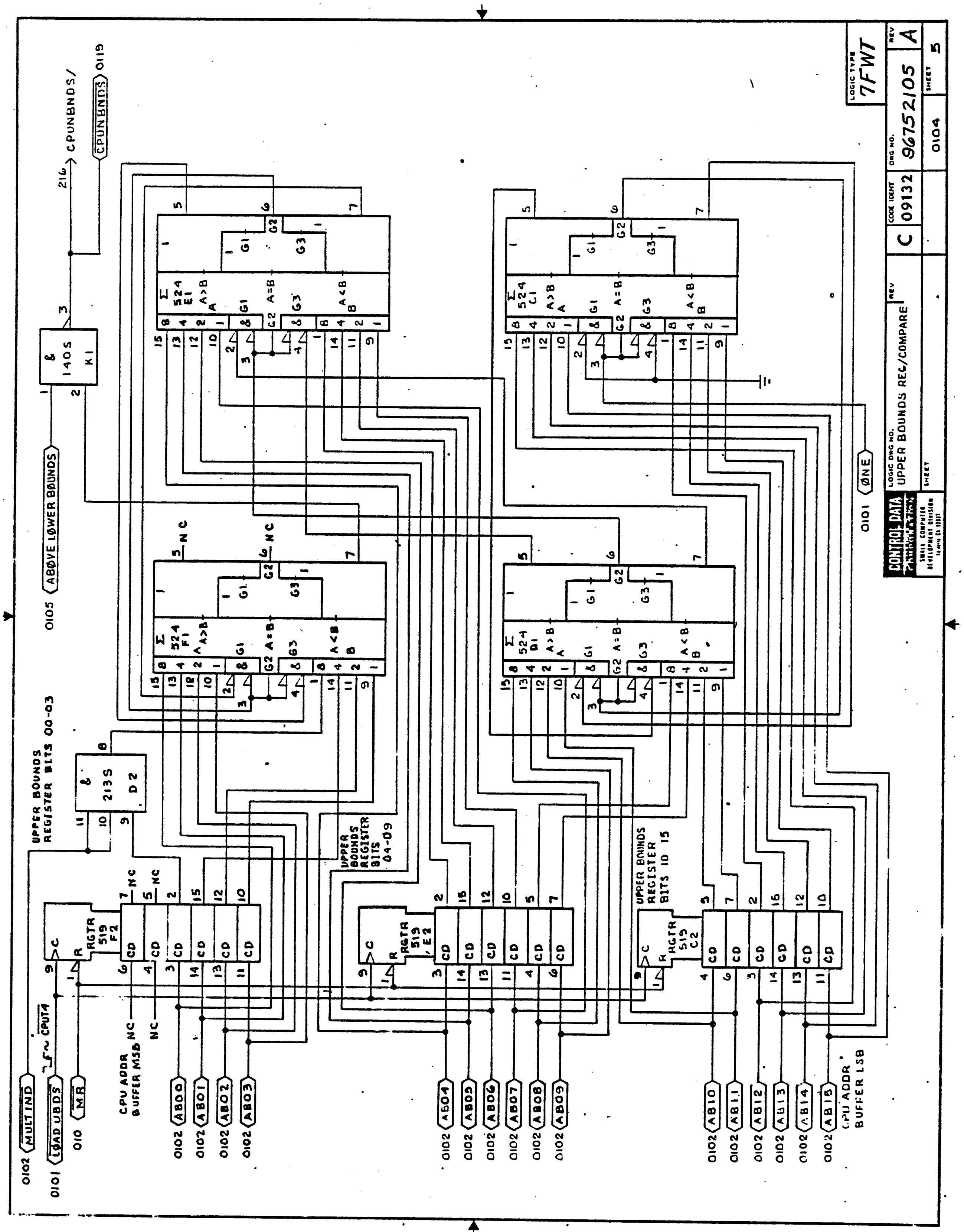

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 5 of 23)

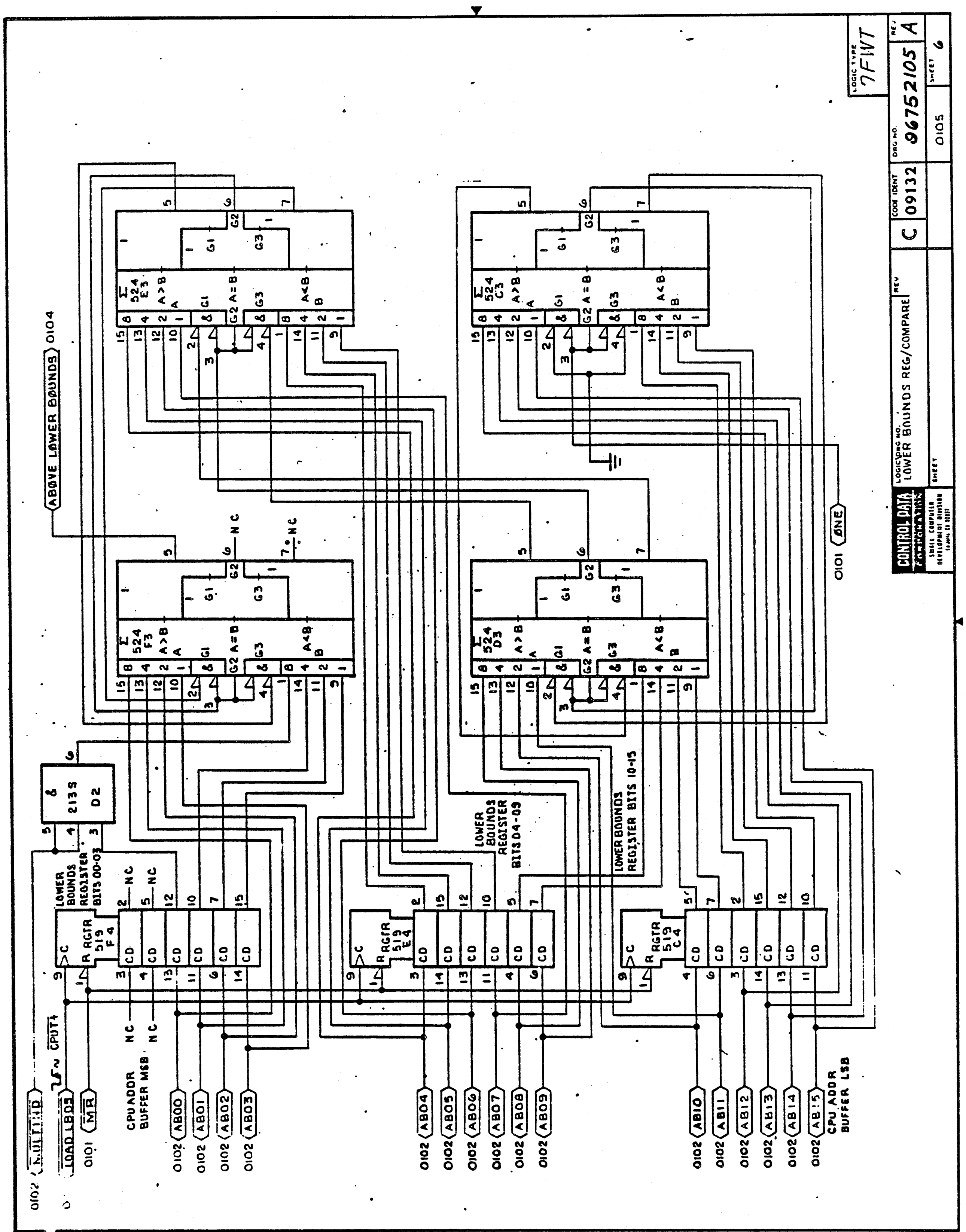

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 6 of 23)

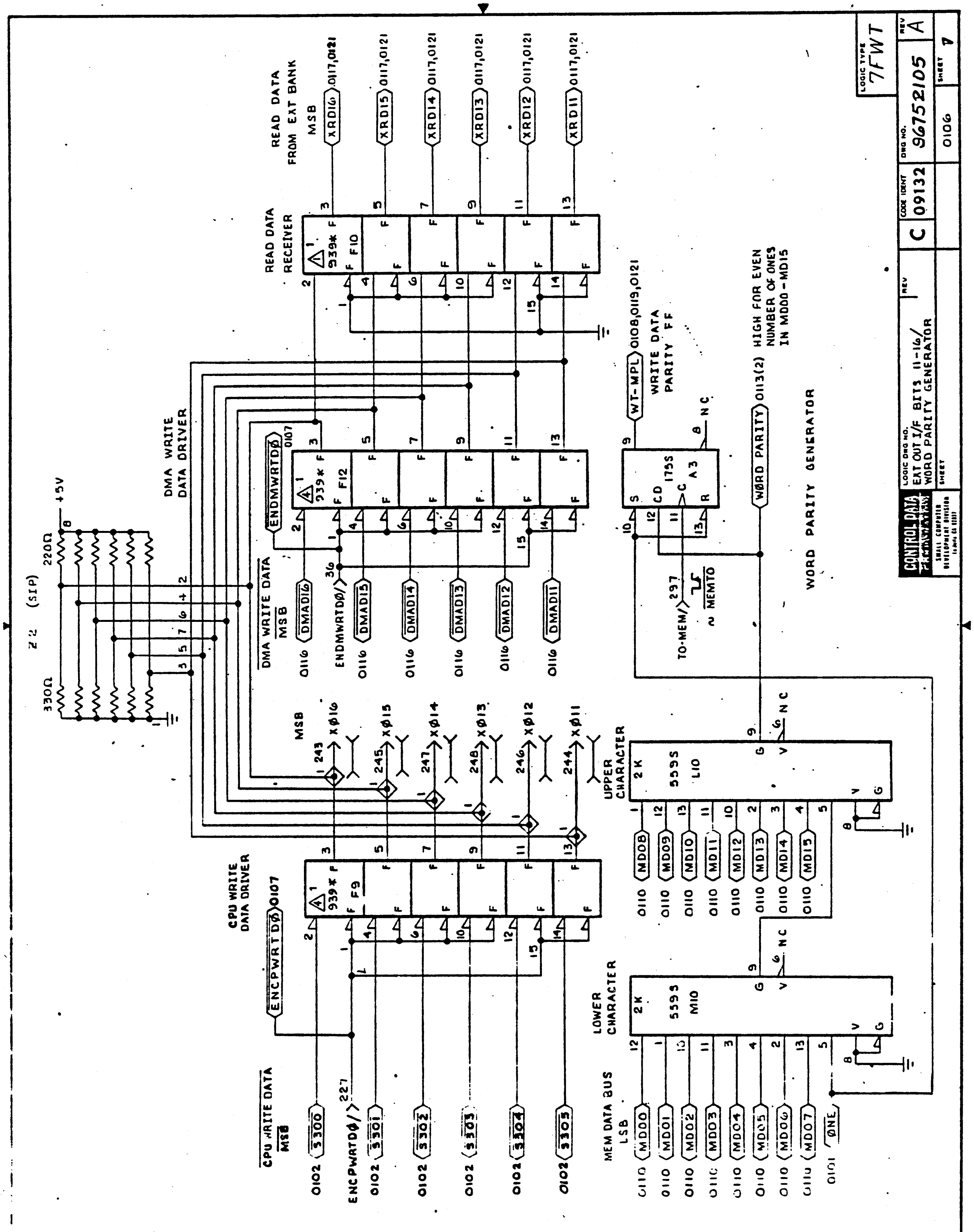

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 7 of 23)

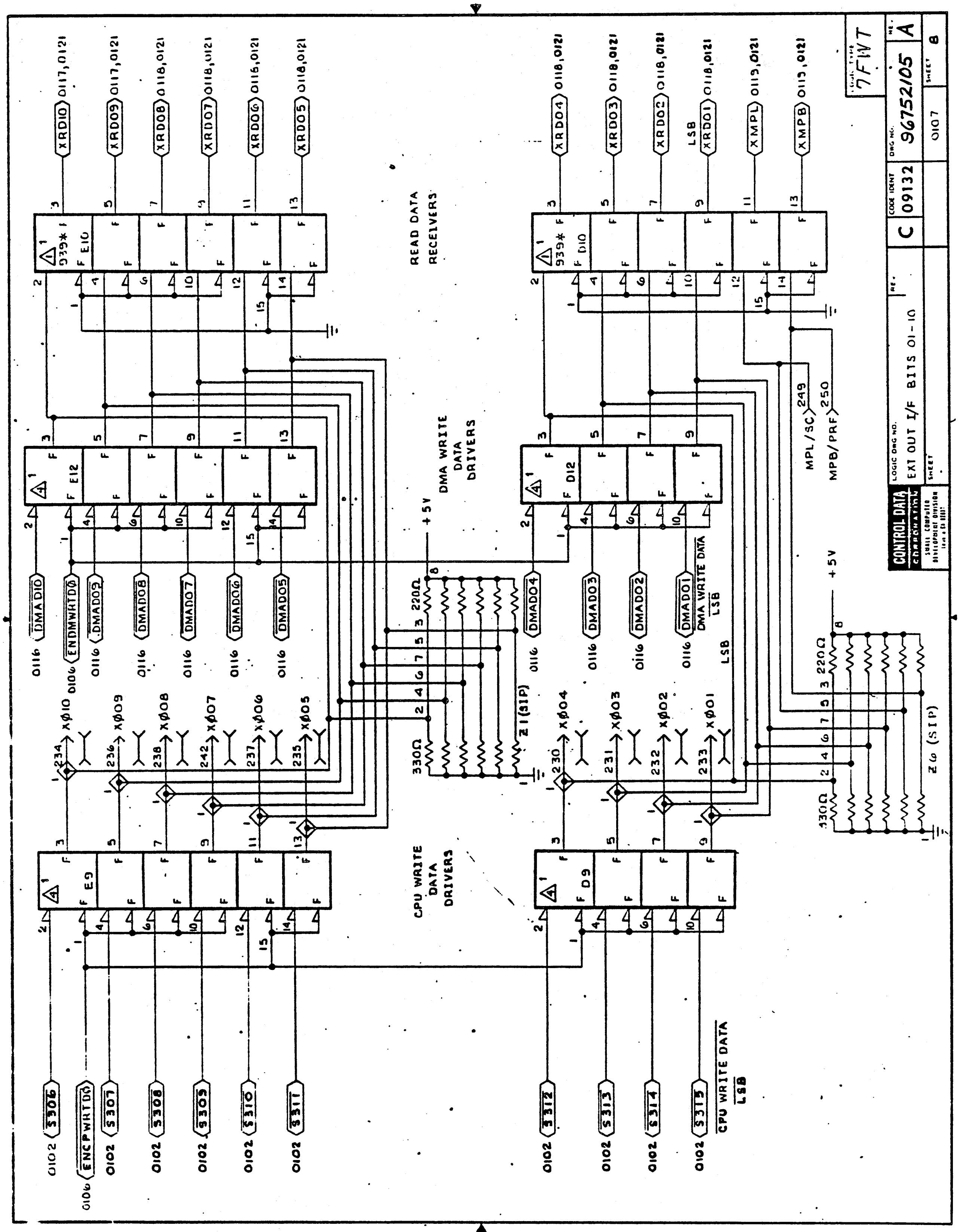

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 8 of 23)

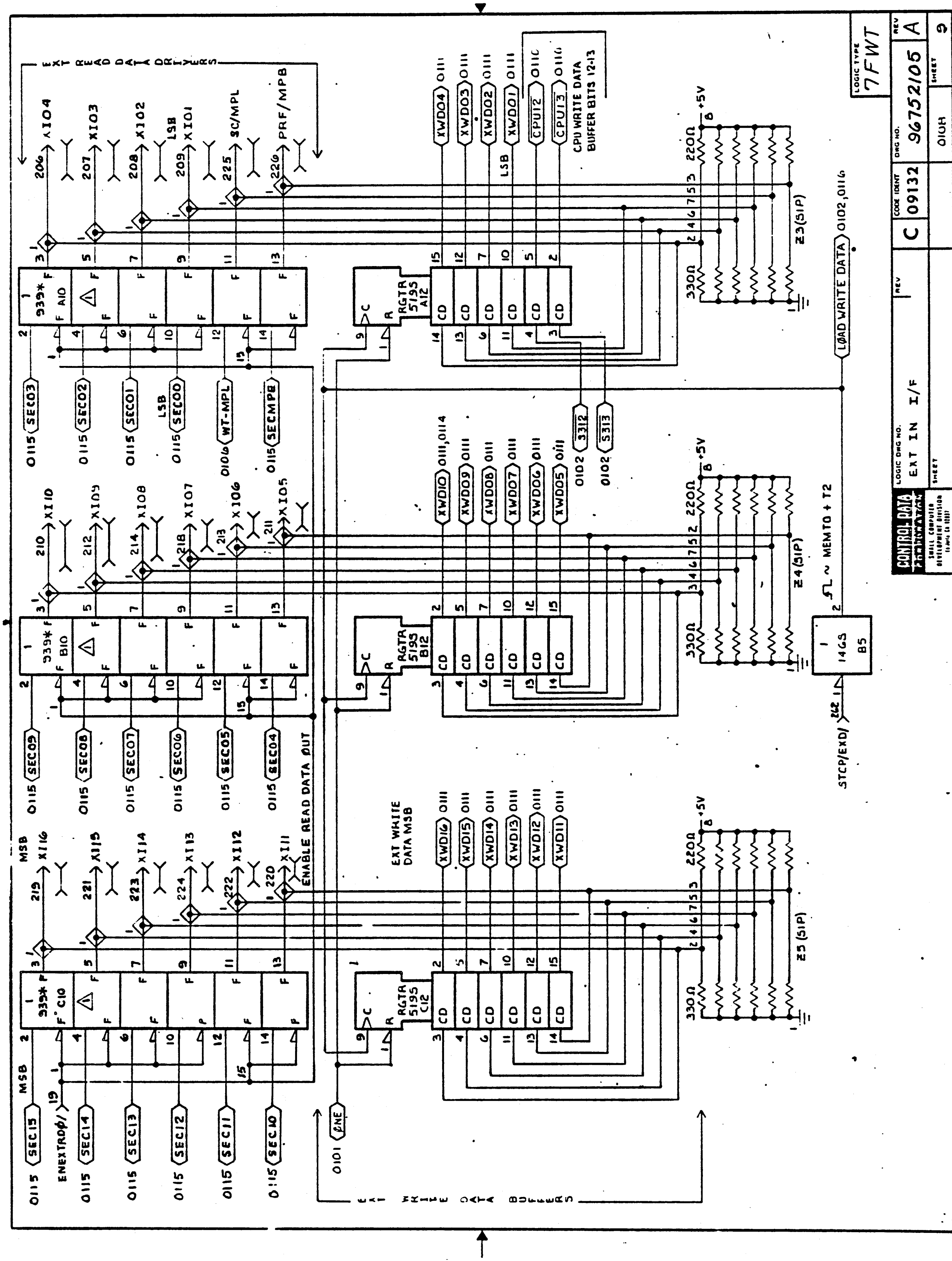

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 9 of 23)

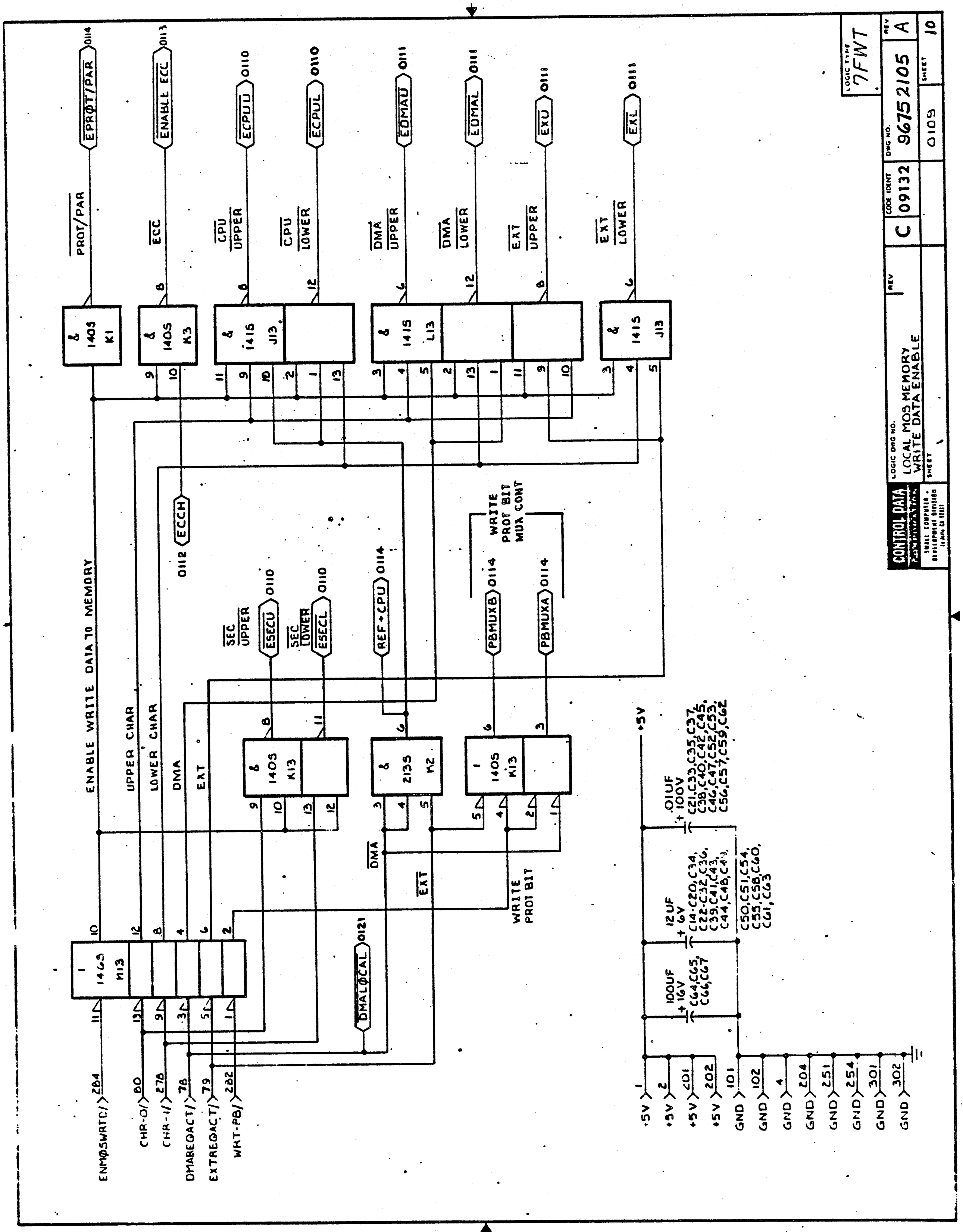

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 10 of 23)

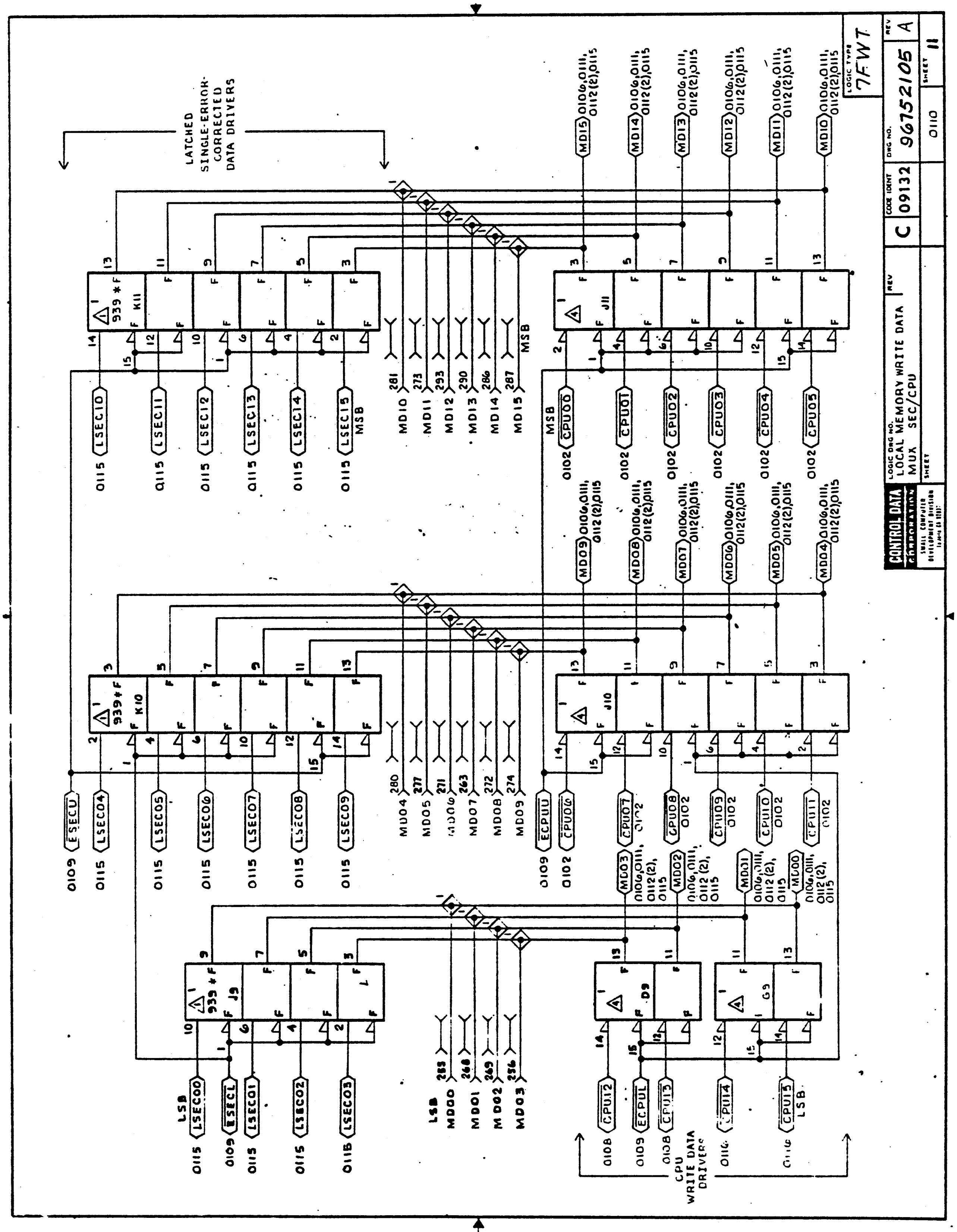

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 11 of 23)

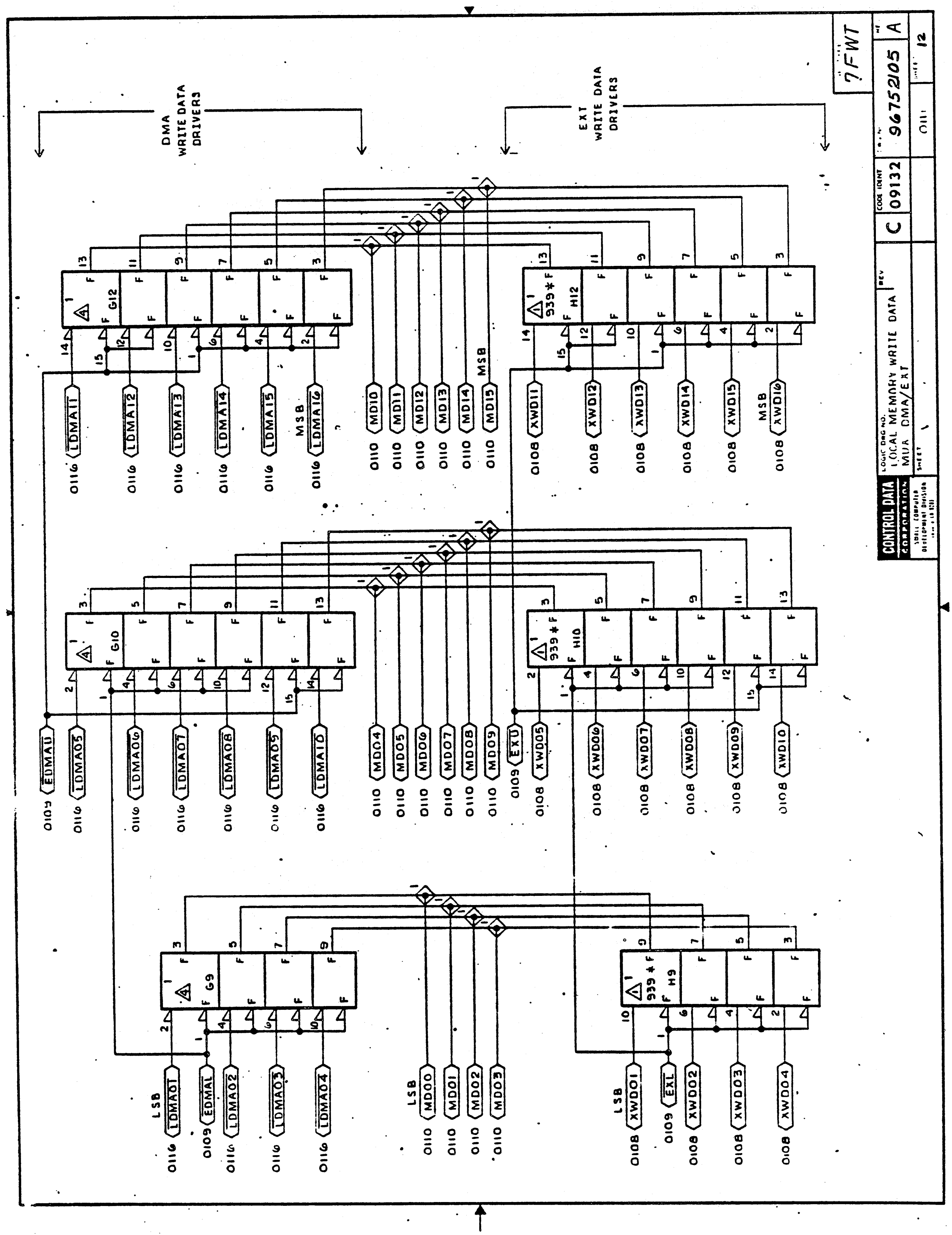

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 12 of 23)

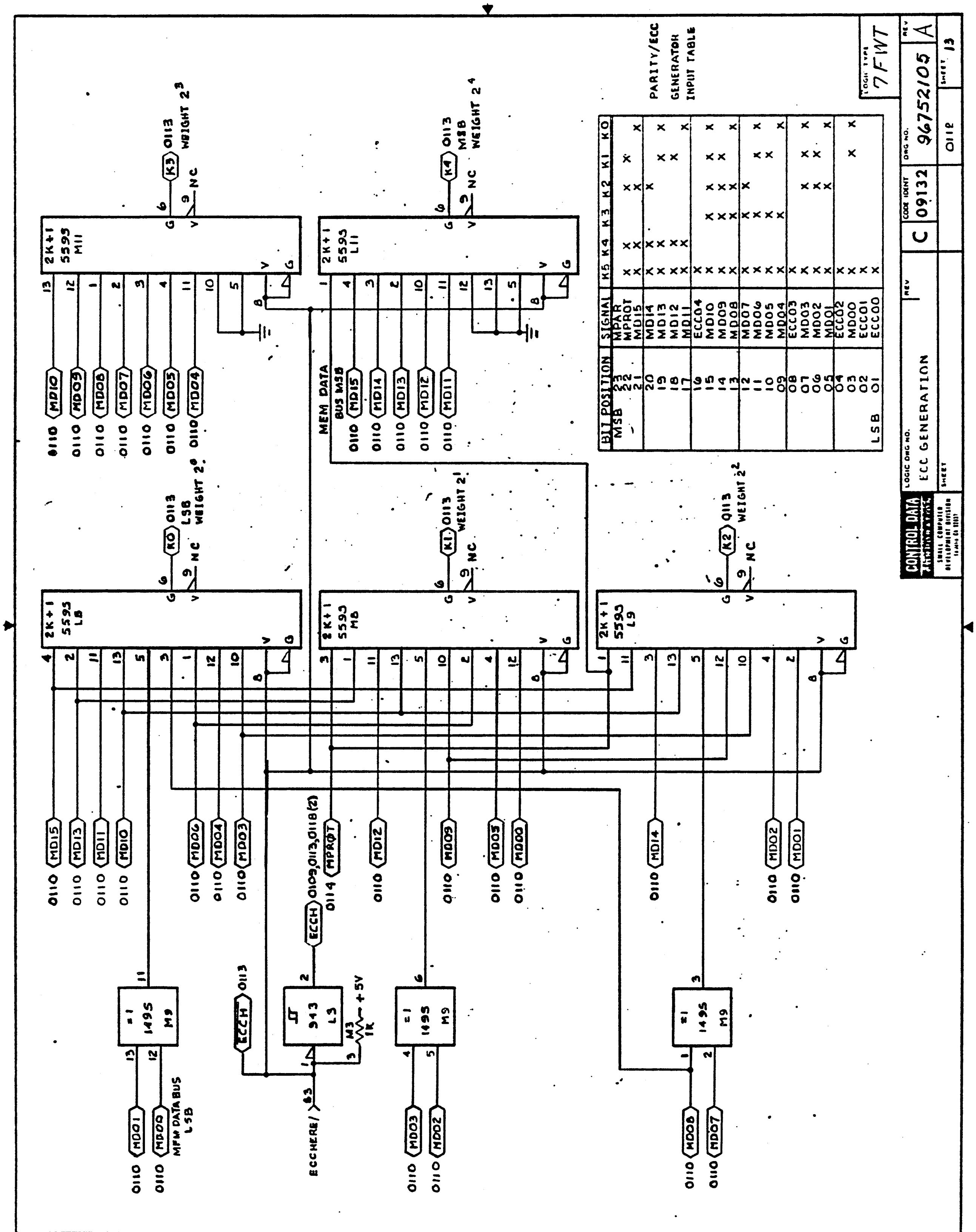

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 13 of 23)

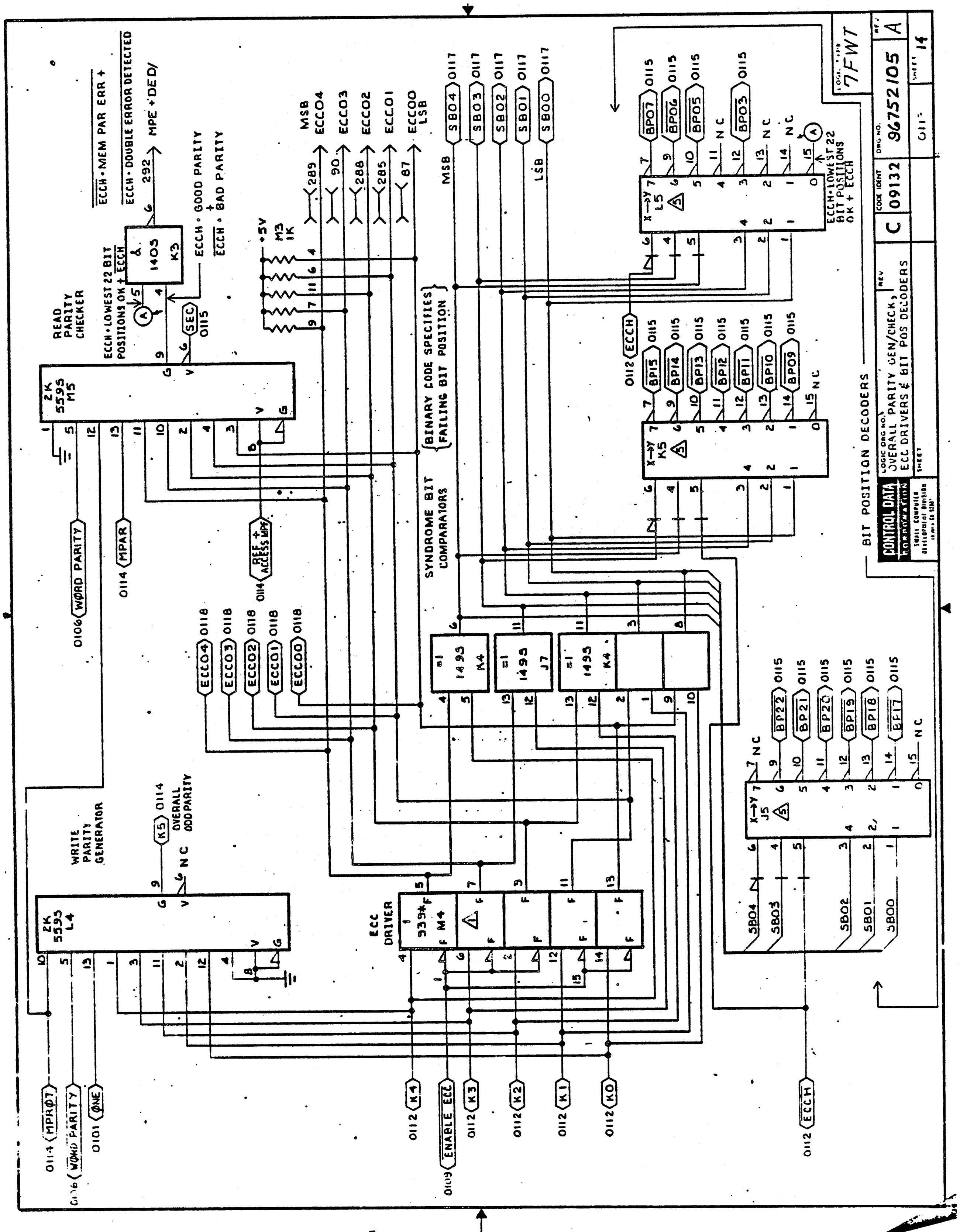

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 14 of 23)

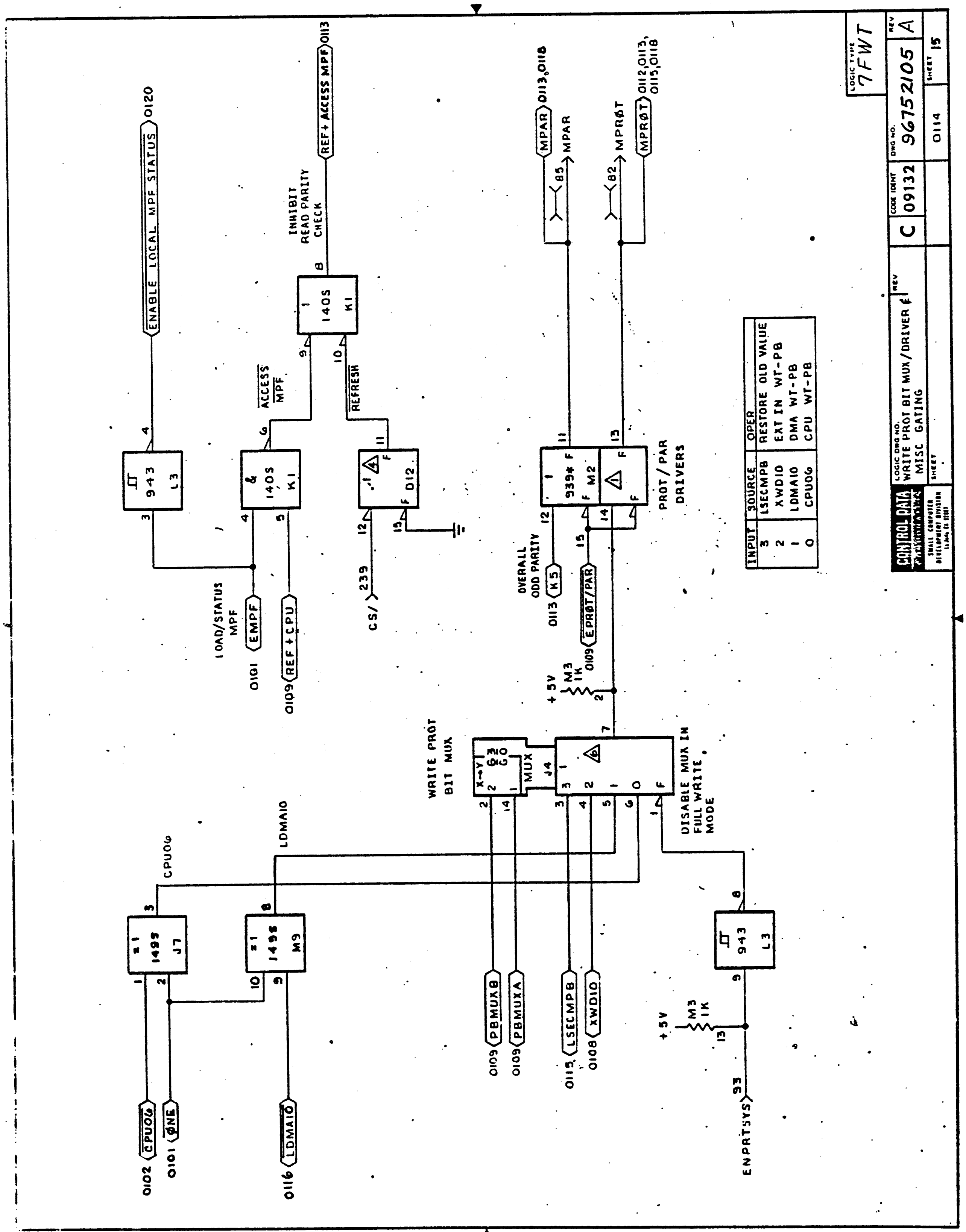

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 15 of 23)

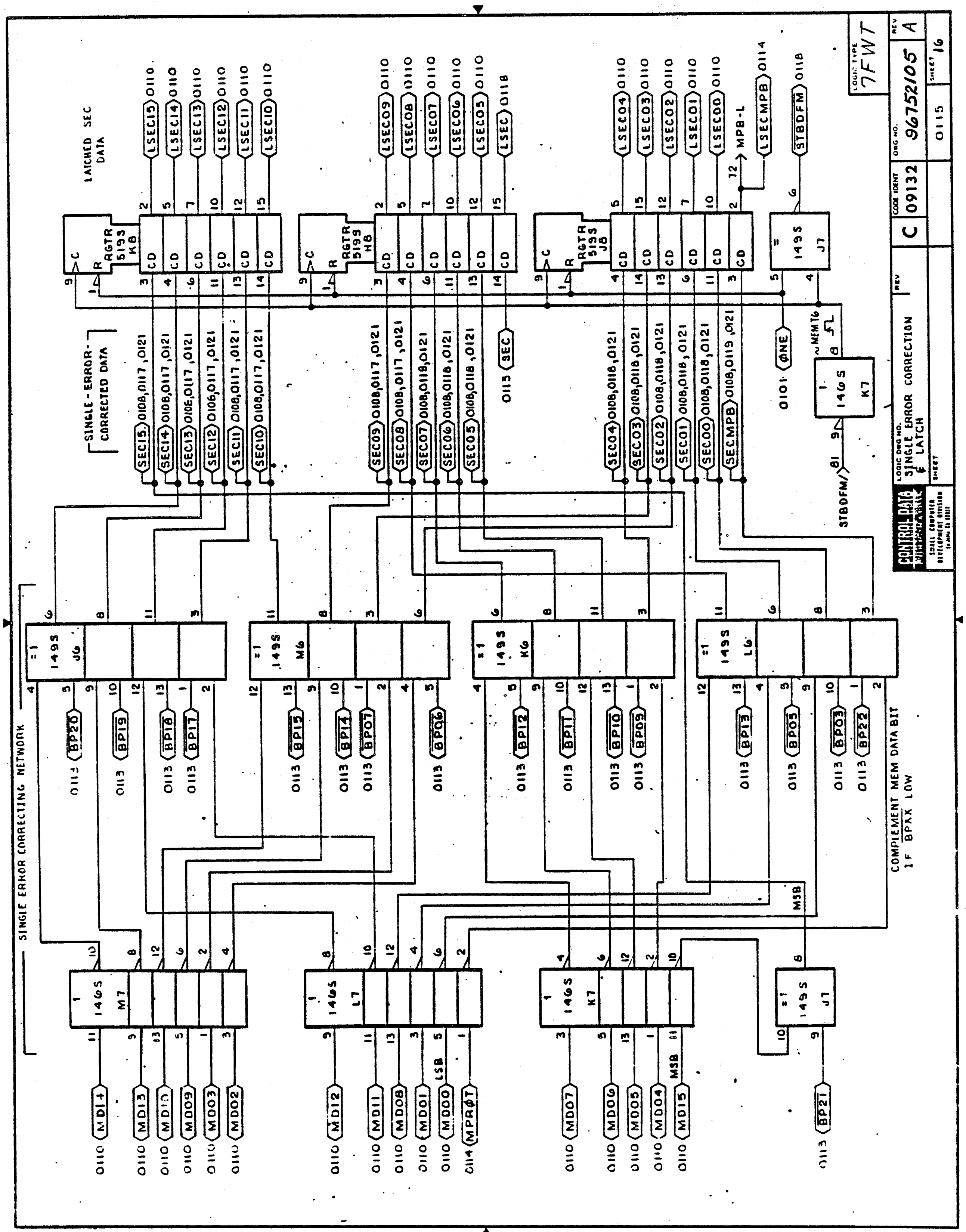

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 16 of 23)

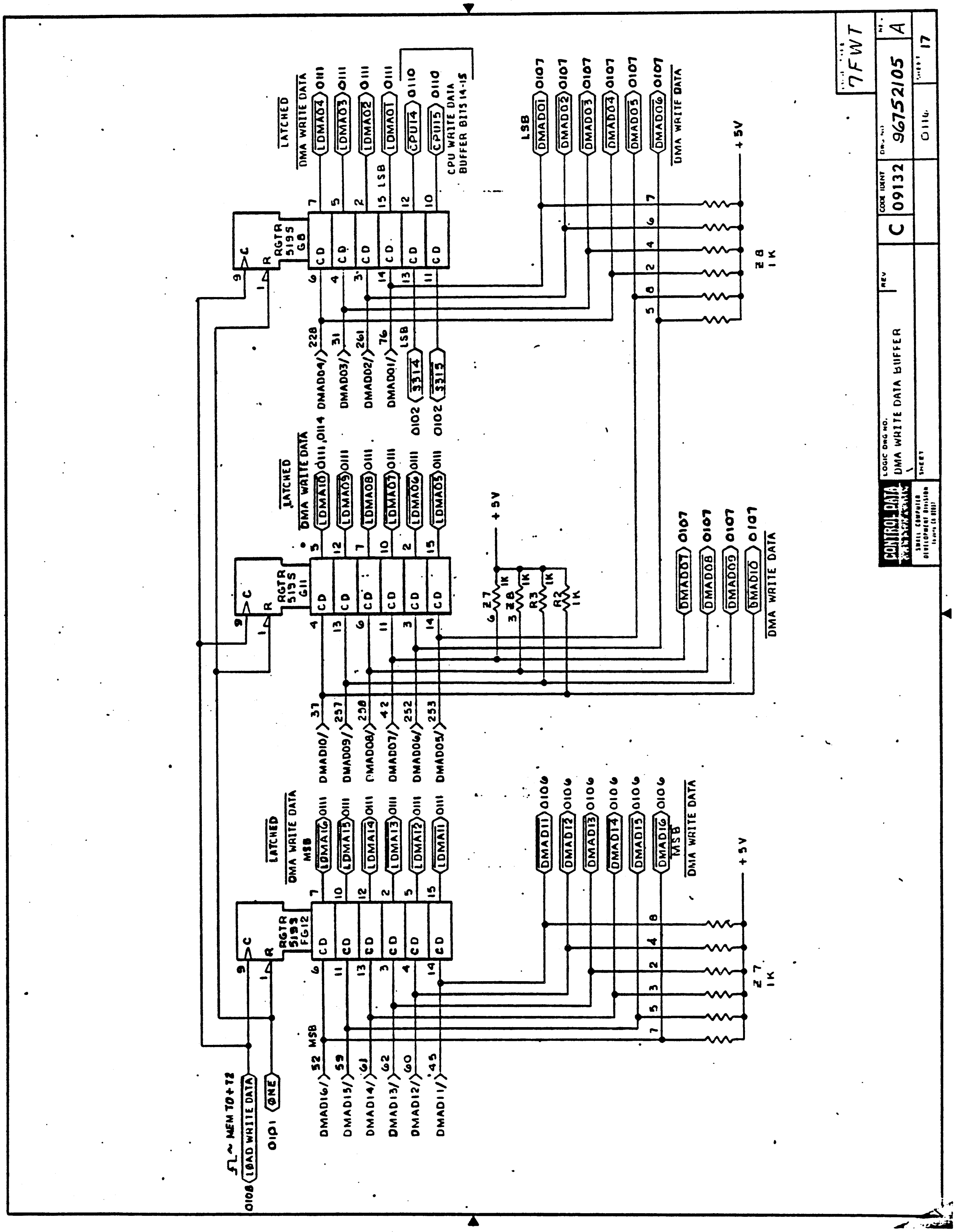

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 17 of 23)

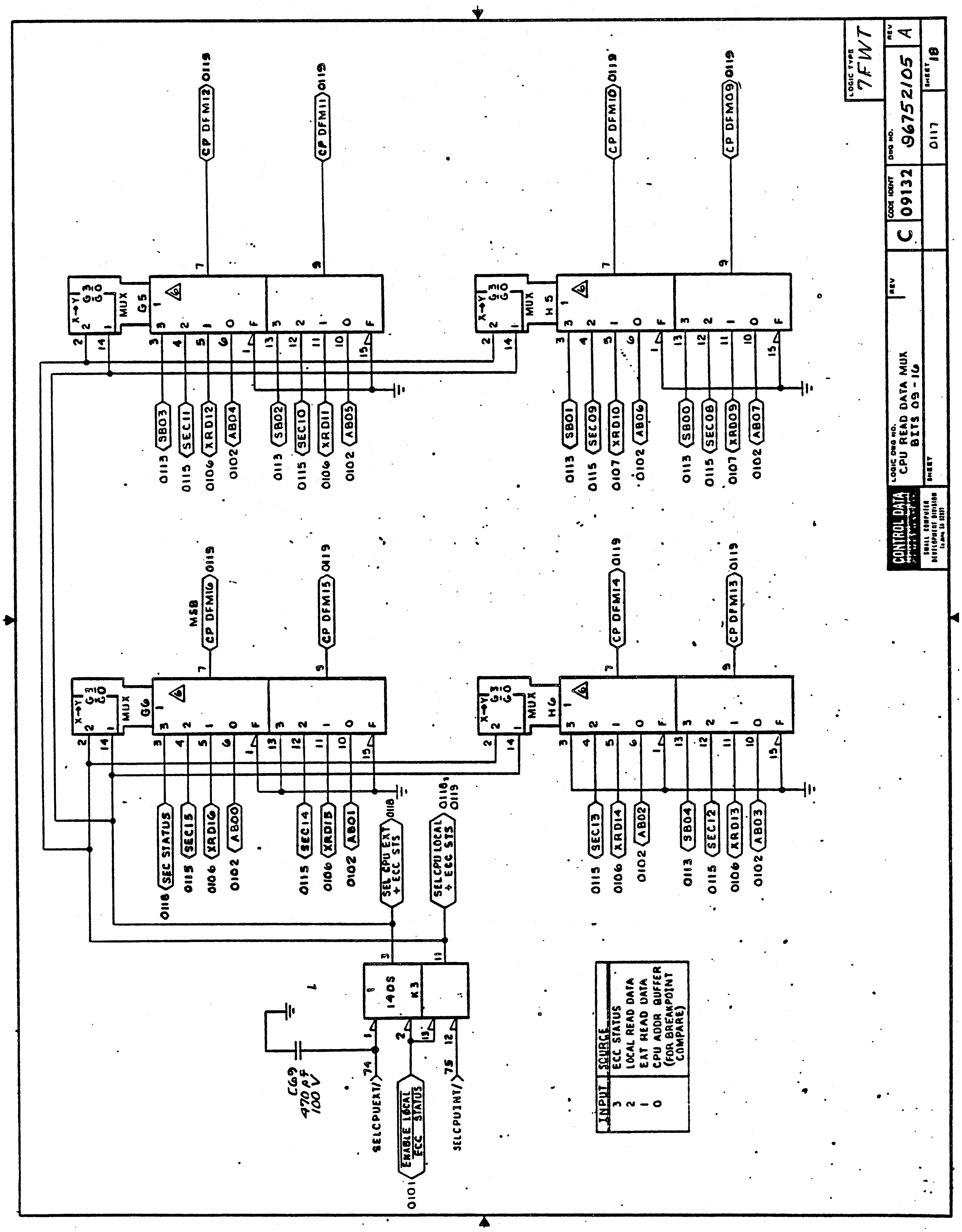

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 18 of 23)

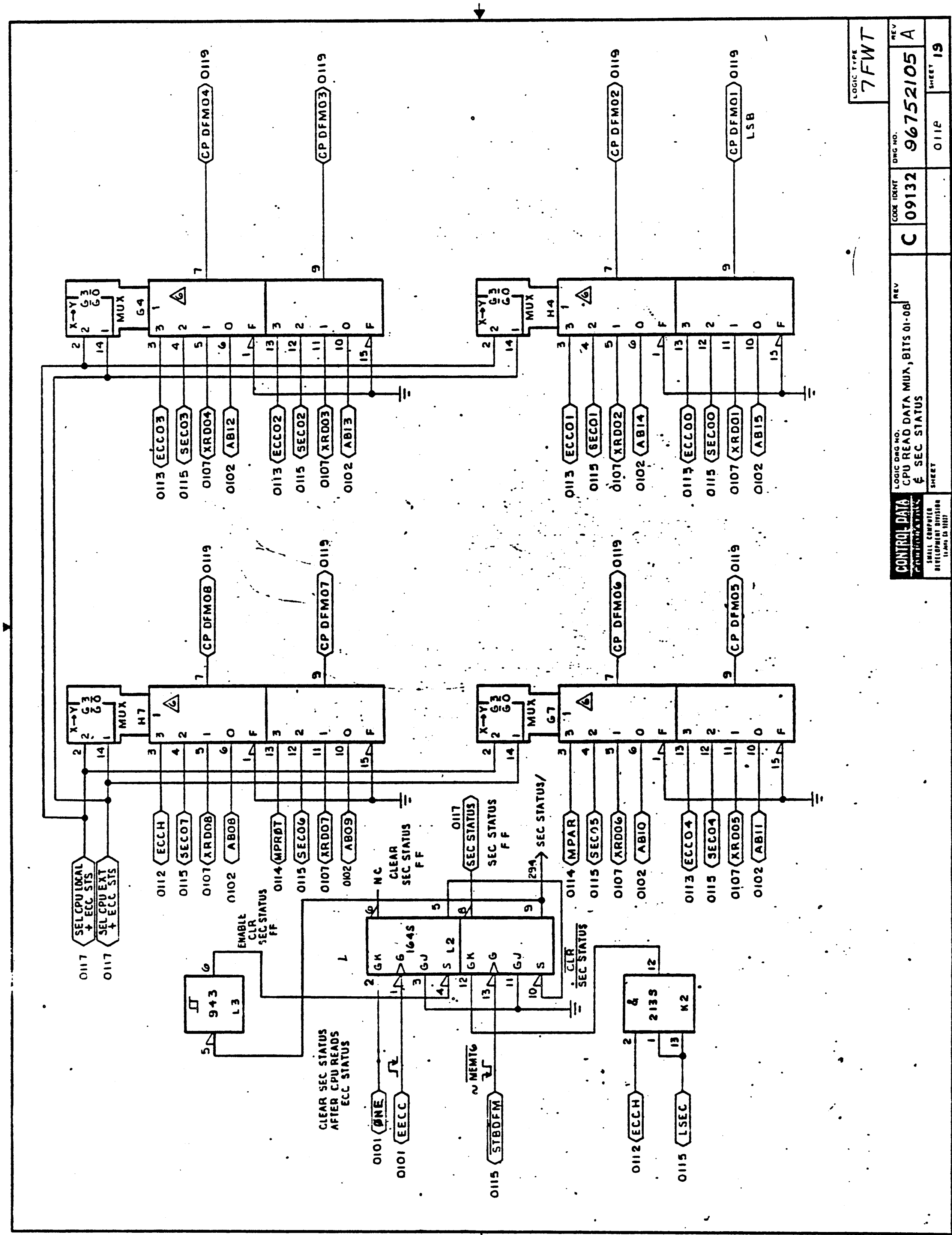

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 19 of 23)

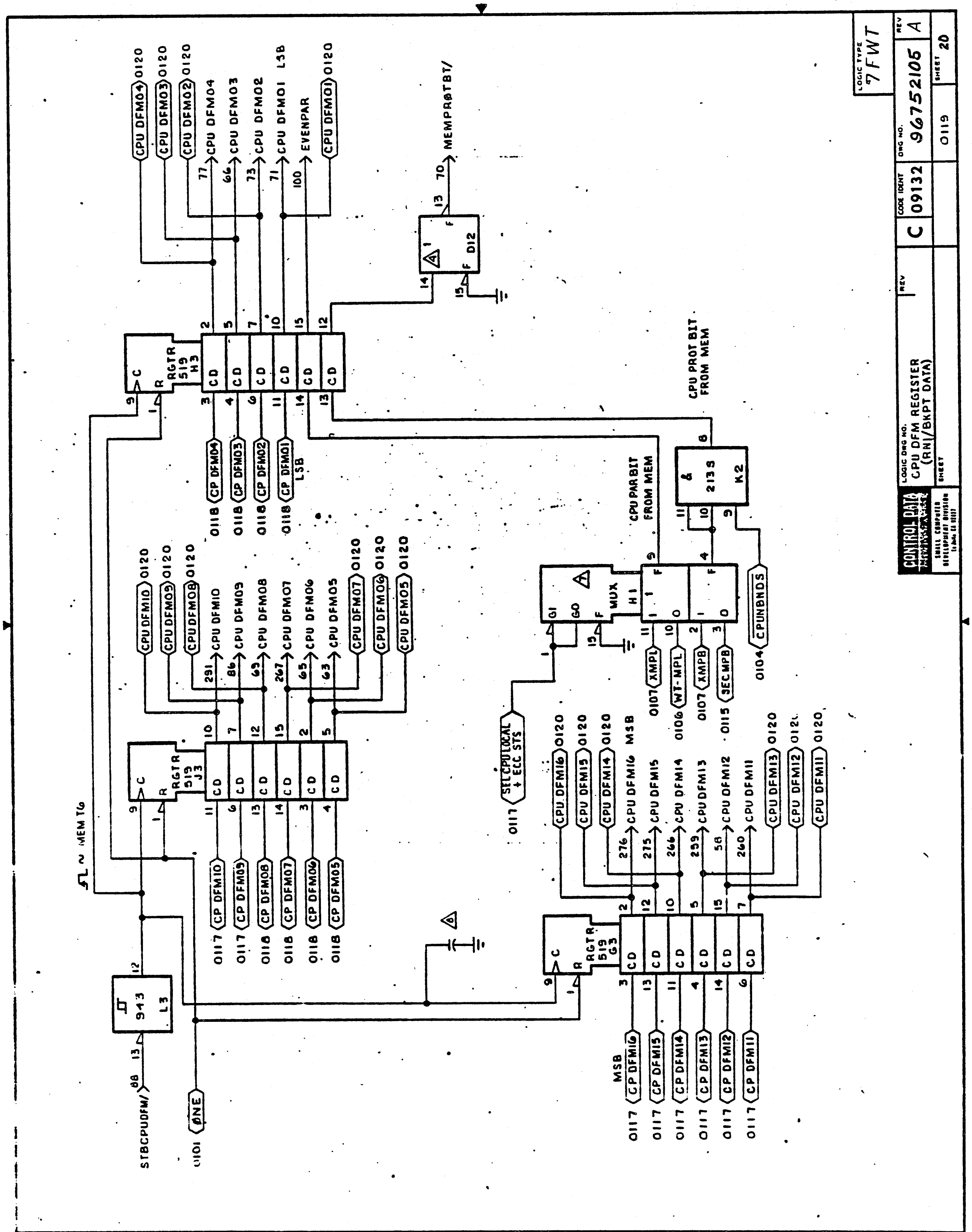

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 20 of 23)

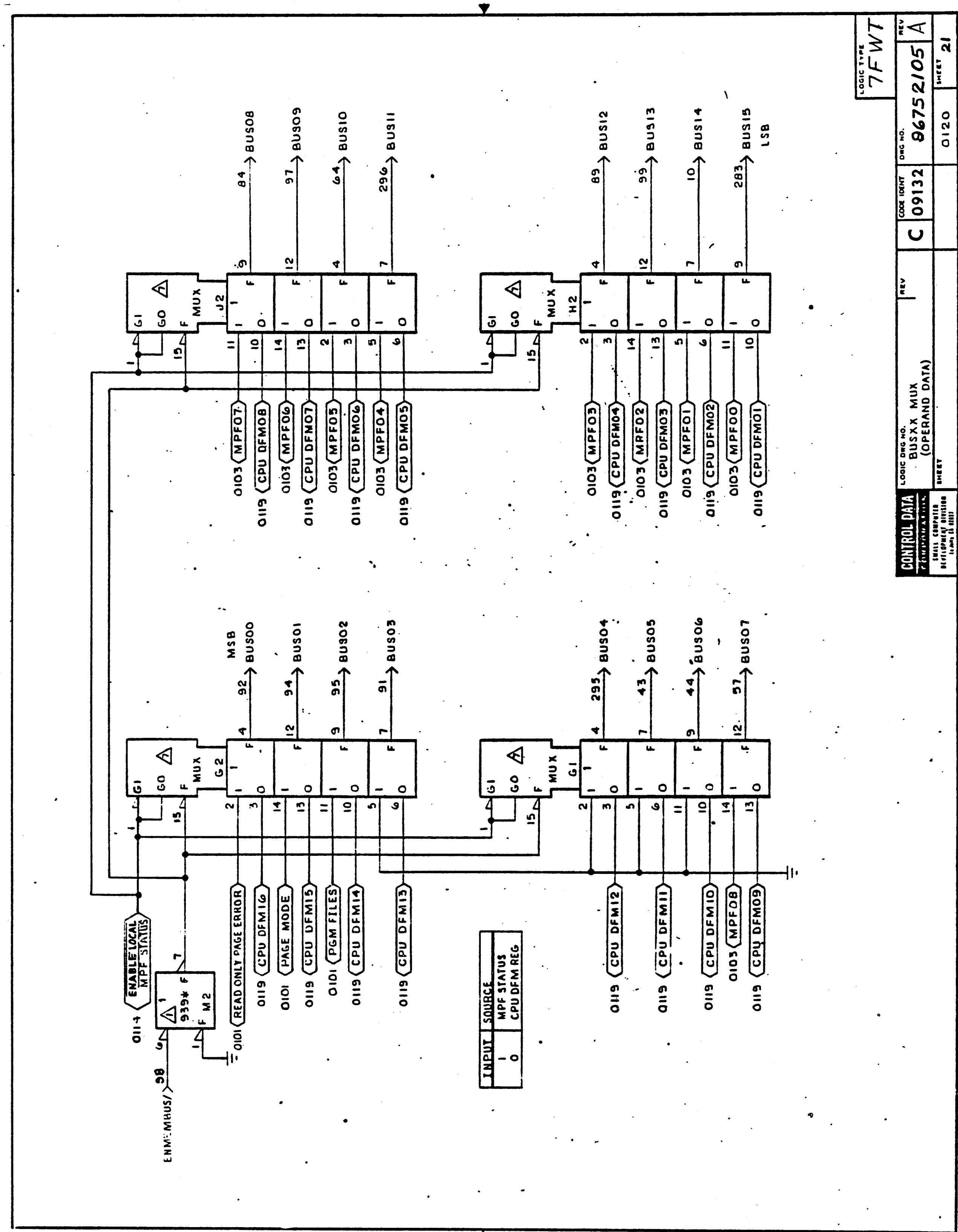

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 21 of 23)

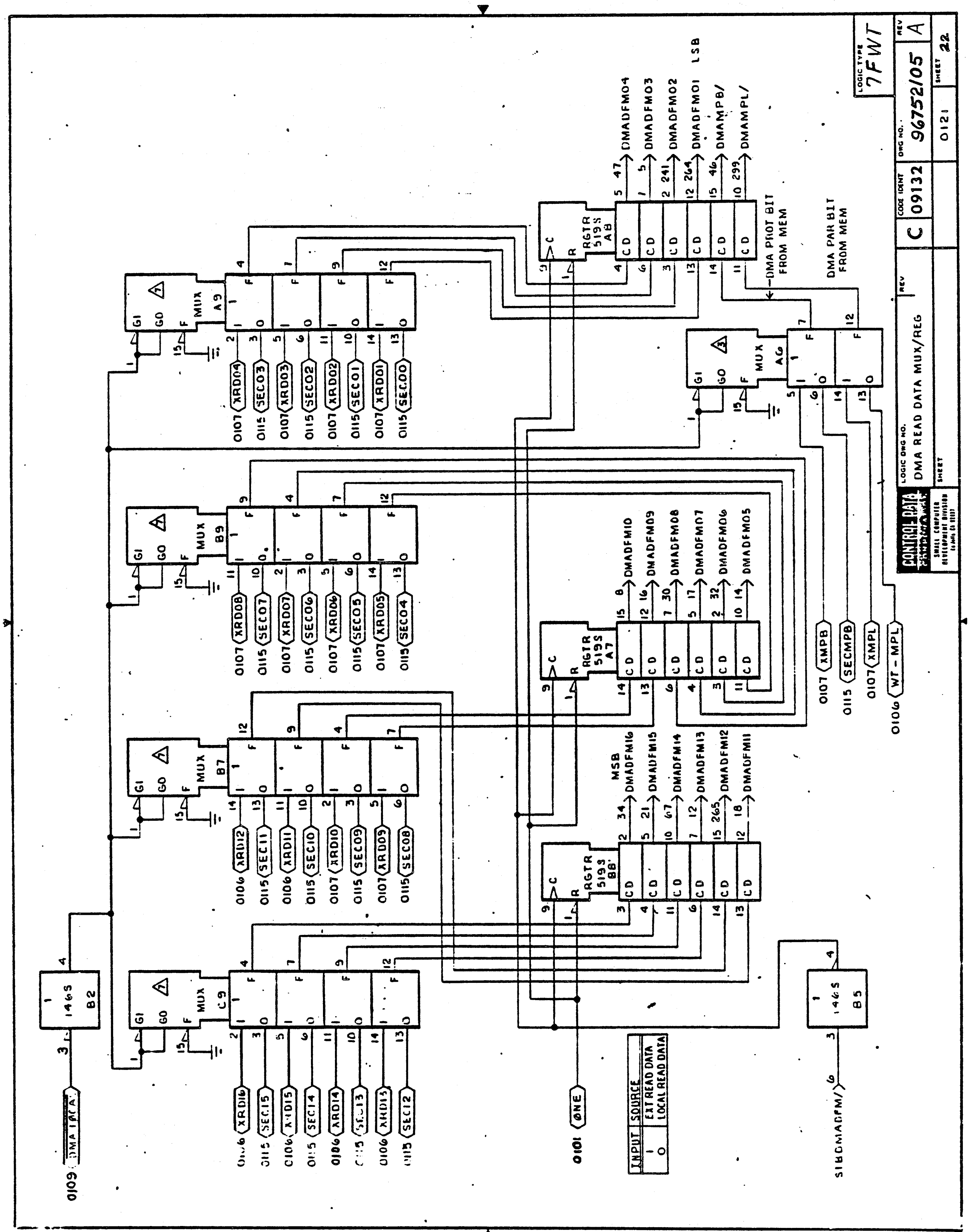

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 22 of 23)

K(CA-STA)

DWN	DSS	10-5-77	CONTROL DATA	TITLE LOGIC - MOS MEM INTFC DATA 7FWT	PREFIX DR	DOCUMENT NO. 96752105	REV. B
CHKD	[illegible]	10-17-77	DATA SYSTEMS LAJOLLA DIVISION	FIRST USED ON		SHEET 1 of 1	
ENG	[illegible]	11-24-77	CODE IDENT 09132				
MFG	R. Wilkinson	11-16-77					
APPR	A. Wede	11-29-77					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS14982	CL. A. RELEASED	DSS	11-29-77	AW
B	DS 22172	INACTIVATED REPL BY NONE	BR	4-2-82	AW

INACTIVE

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
AA6030

NOTES:

DETACHED LISTS

E
B

AA3180 REV. 8/71

PRINTED IN U.S.A.

Figure 5-13. MOS Memory Interface Data (PWA 96752104) Logic Diagram (Sheet 23 of 23)

SIGNAL	PIN	CROSS REF NO
BLKAB/	229	0101
BUS 00	92	0120
BUS 01	94	0120
BUS 02	95	0120
BUS 03	91	0120
BUS 04	295	0120
BUS 05	45	0120
BUS 06	44	0120
BUS 07	57	0120
BUS 08	84	0120
BUS 09	97	0120
BUS 10	64	0120
BUS 11	296	0120
BUS 12	89	0120
BUS 13	99	0120
BUS 14	10	0120
BUS 15	283	0120
CHR-0/	80	0109
CHR-1/	278	0109
CPUDFM01	71	0119
CPUDFM02	73	0119
CPUDFM03	66	0119
CPUDFM04	77	0119
CPUDFM05	63	0119
CPUDFM06	65	0119
CPUDFM07	267	0119
CPUDFM08	69	0119
CPUDFM09	86	0119
CPUDFM10	291	0119
CPUDFM11	260	0119
CPUDFM12	58	0119
CPUDFM13	259	0119
CPUDFM14	266	0119
CPUDFM15	275	0119
CPUDFM16	276	0119
CPUNBNDS/	216	0106
CPUMAB 12/	50	0103
CPUMAB 13/	48	0103
CPUMAB 14/	49	0103
CPUMAB 15/	51	0103
CPUMAB 16/	270	0103
CPUMAB 17/	26	0103

SIGNAL	PIN	CROSS REF NO
CPUMAB 18/	68	010
CS/	239	0114
DMAD01/	76	0116
DMAD02/	261	0116
DMAD03/	31	0116
DMAD04/	228	0116
DMAD05/	255	0116
DMAD06/	252	0116
DMAD07/	42	0116
DMAD08/	258	0116
DMAD09/	257	0116
DMAD10/	37	0116
DMAD11/	45	0116
DMAD12/	60	0116
DMAD13/	62	0116
DMAD14/	61	0116
DMAD15/	59	0116
DMAD16/	52	0116
DMADFM01	264	0121
DMADFM02	241	0121
DMADFM03	5	0121
DMADFM04	47	0121
DMADFM05	14	0121
DMADFM06	32	0121
DMADFM07	17	0121
DMADFM08	30	0121
DMADFM09	16	0121
DMADFM10	8	0121
DMADFM11	18	0121
DMADFM12	265	0121
DMADFM13	12	0121
DMADFM14	67	0121
DMADFM15	21	0121
DMADFM16	34	0121
DMAMPB/	46	0121
DMAMPL/	299	0121
DMAREQACT/	78	0109
ECC 00	87	0113
ECC 01	285	0113
ECC 02	288	0113
ECC 03	90	0113
ECC 04	289	0113

SIGNAL	PIN	CROSS REF NO
ECC HERE/	83	0112
EMPF	298	0101
ENCPWRTDØ/	227	0106
ENDMWRTDØ/	36	0106
ENEXTRDØ/	19	0118
ENMEMBUS/	98	0120
ENMØSWRTD/	284	0109
ENPRTSYS	93	0114
EVENPAR	100	0119
EXTREQACT/	79	0109
GATEAB/	205	0101
GATELBDS/	53	0101
GATEUBDS/	215	0101
GND	4	0109
GND	101	0109
GND	102	0109
GND	204	0109
GND	251	0109
GND	254	0109
GND	301	0109
GND	302	0109
MC/	96	0101
MD00	255	0110
MD01	268	0110
MD02	269	0110
MD03	256	0110
MD04	280	0110
MD05	277	0110
MD06	271	0110
MD07	263	0110
MD08	272	0110
MD09	274	0110
MD10	281	0110
MD11	273	0110
MD12	293	0110
MD13	290	0110
MD14	286	0110
MD15	287	0110
MEMPRØTBT/	70	0119
MIR 28'	9	0101
MIR 29'	300	0101
MIR 30'	7	0101

SIGNAL	PIN	CROSS REF NO
MIR 31'	11	0101
MPAR	85	0114
MPB-L	72	0115
MPB/PRF	250	0109
MPE+DED/	292	0113
MPL/SC	249	0109
MPRØT	82	0114
MULTIND	13	0102
PAGE MØDE/	3	0101
PGM FILES/	203	0101
PRF/MPB	226	0110
RDØ PAGE/	240	0101
RØP INT/	20	0101
S300/	54	0102
S301/	56	0102
S302/	55	0102
S303/	53	0102
S304/	39	0102
S305/	41	0102
S306/	40	0102
S307/	38	0102
S308/	23	0102
S309/	28	0102
S310/	24	0102
S311/	22	0102
S312/	29	0102
S313/	35	0102
S314/	15	0102
S315/	27	0102
SC/MPL	225	0110
SEC STATUS/	294	0118
SELCPUEXT/	74	0117
SELCPUINT/	75	0117
STBCPUDFM/	88	0119
STBDFM/	81	0115
STBDMADFM/	6	0121
STCP/EXD/	262	0108
TO'/	25	0101
TO-MEM/	297	0106
WRT-MPF/	217	0101
WRT-PB/	282	0109
XI01	209	0110

SIGNAL	PIN	CROSS REF NO
XI02	208	0110
XI03	207	0110
XI04	206	0110
XI05	211	0110
XI06	213	0110
XI07	218	0110
XI08	214	0110
XI09	212	0110
XI10	210	0110
XI11	220	0110
XI12	222	0110
XI13	224	0110
XI14	223	0110
XI15	221	0110
XI16	219	0110
XØ01	233	0109
XØ02	232	0109
XØ03	231	0109
XØ04	230	0109
XØ05	235	0109
XØ06	237	0109
XØ07	242	0109
XØ08	238	0109
XØ09	236	0109
XØ10	234	0109
XØ11	244	0108
XØ12	246	0108
XØ13	248	0108
XØ14	247	0108
XØ15	245	0108
XØ16	243	0108
+5V	1	0109
+5V	2	0109
+5V	201	0109
+5V	202	0109

1. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S257.
2. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S253.
3. NO ELEMENT IDENTIFIER AVAILABLE FOR 74S138.
4. 8T98 IS SIMILAR TO 939
5. CAPACITOR PROVISIONAL NOT ON PWA
6. 74S258 IS SIMILAR TO 74S257.
7. NO ELEMENT IDENTIFIER AVAILABLE FOR 82S09.
8. 8T97 IS SIMILAR TO 939.

NOTES: UNLESS OTHERWISE SPECIFIED

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.034.

	DETACHED LIST	A	B	C	D	E	F
96890066	1						
	2						
	3						
	4						
	5						
	6						
	7						

LOGIC TITLE

LOGIC DWG. NO / REV.

PWA NO 96890065 | PWB NO. 96740700

CONTROL DATA — SMALL COMPUTER DEVELOPMENT DIVISION

FIRST USED ON		
DR	B. Roberts	1-18-82
CHK	S. Fye	1-27-82
ENGR		2-1-82
MFG		
APPD	A. Wal	4-2-82

TITLE: LOGIC DIAGRAM – MOS MEMORY INTERFACE (DATA)

LOGIC TYPE 81PTT

SIZE C | CODE IDENT NO. 09132 | DRAWING NO. 96890066 | REV A

SHEET 1

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 1 of 23)

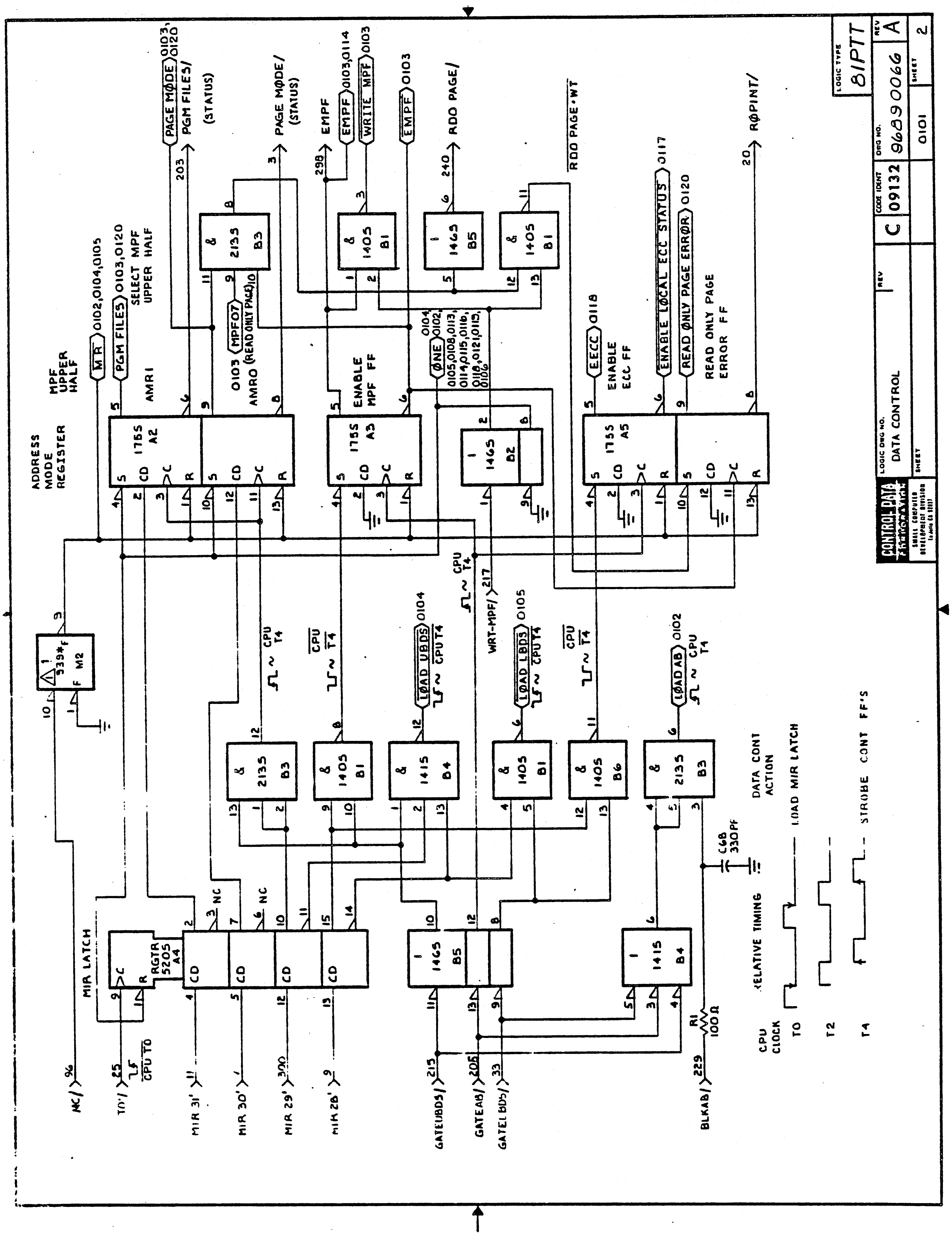

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 2 of 23)

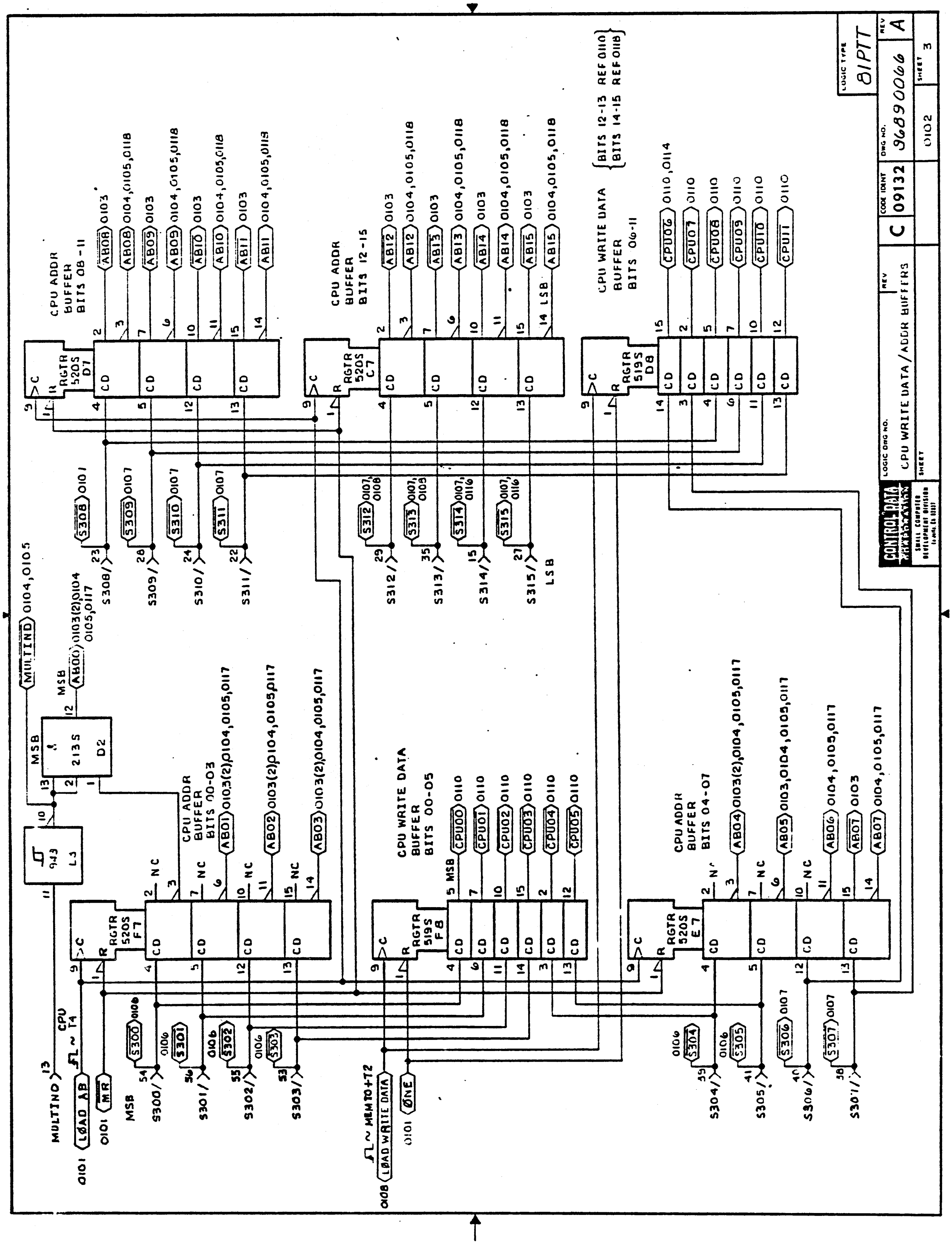

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 3 of 23)

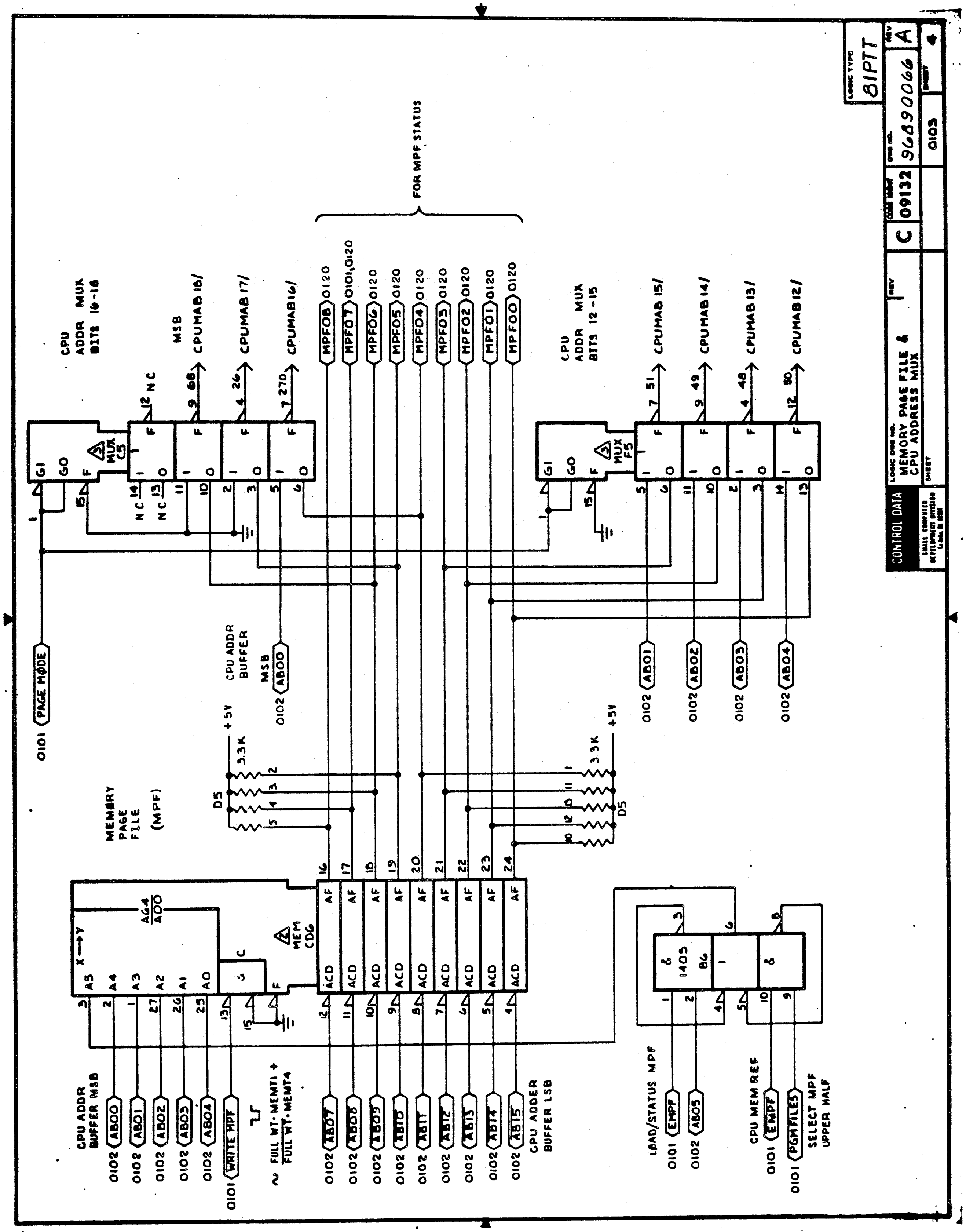

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 4 of 23)

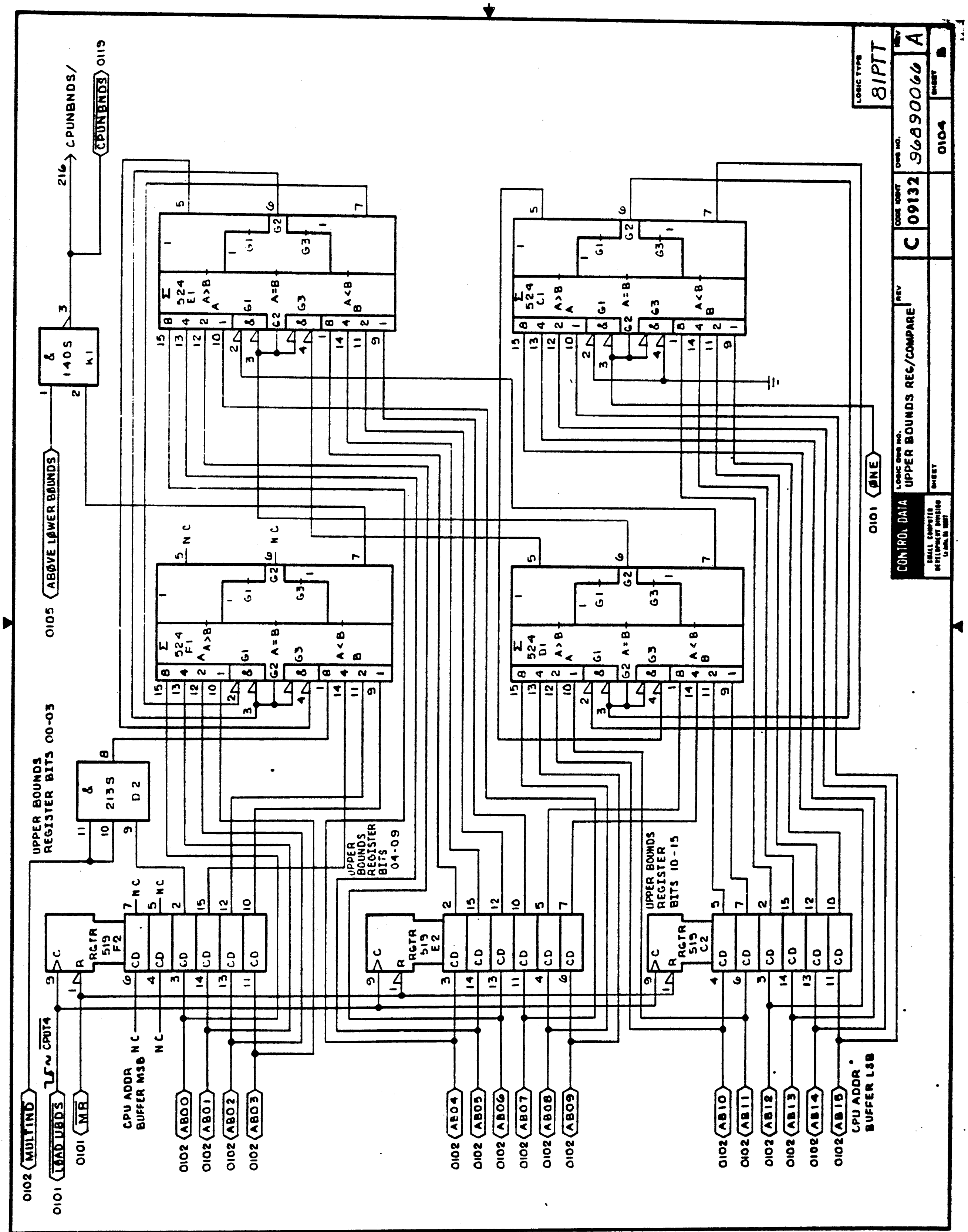

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 5 of 23)

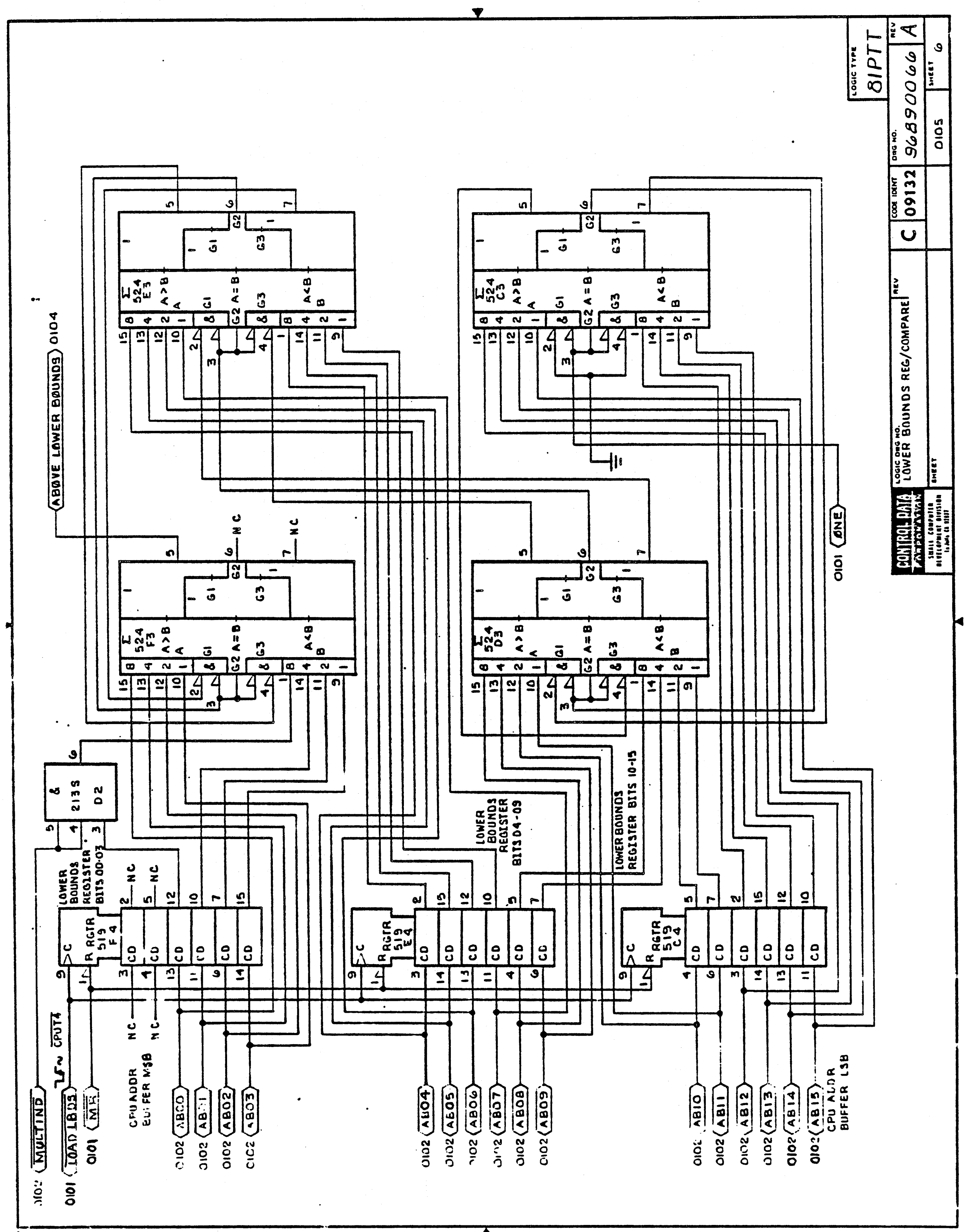

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 6 of 23)

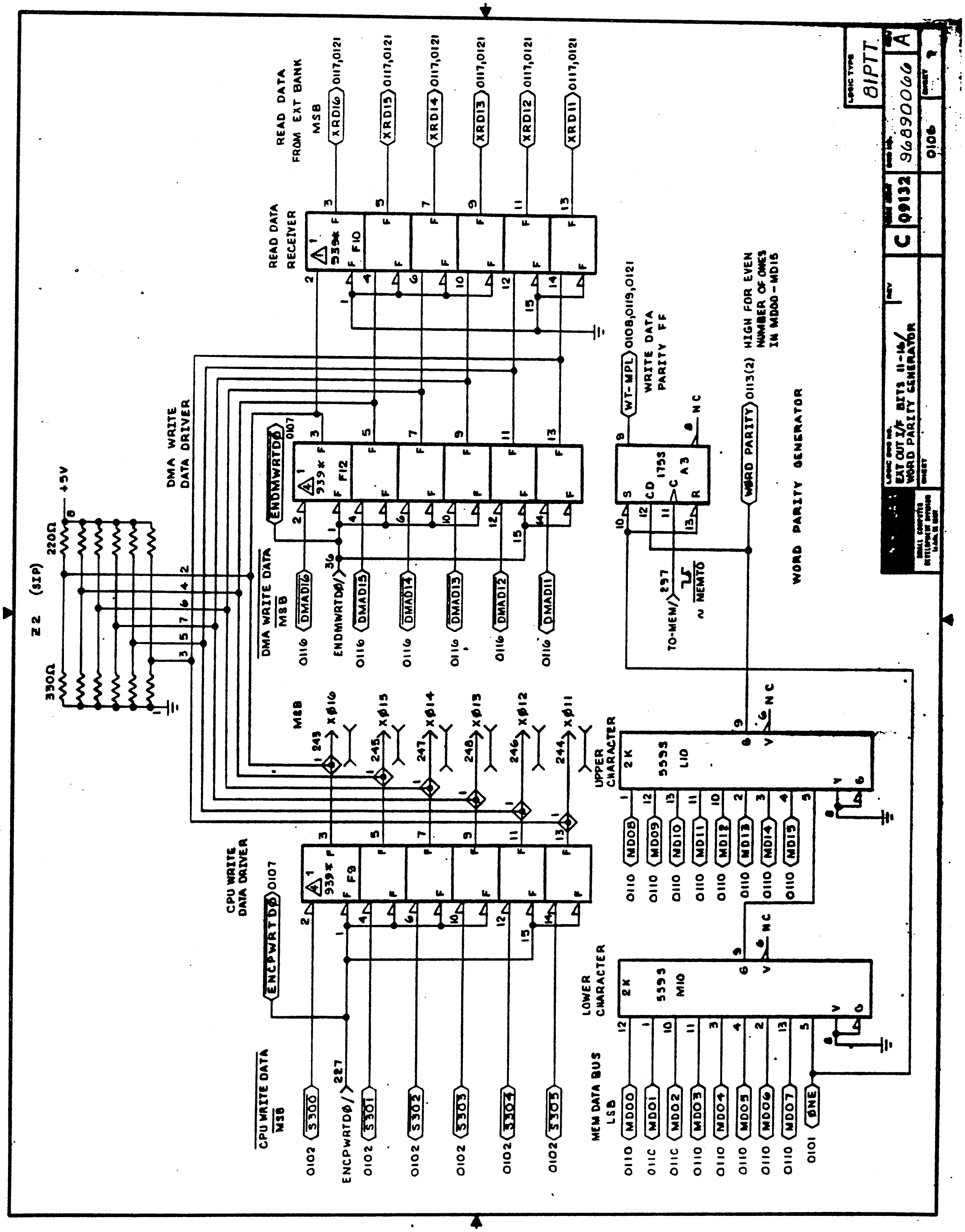

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 7 of 23)

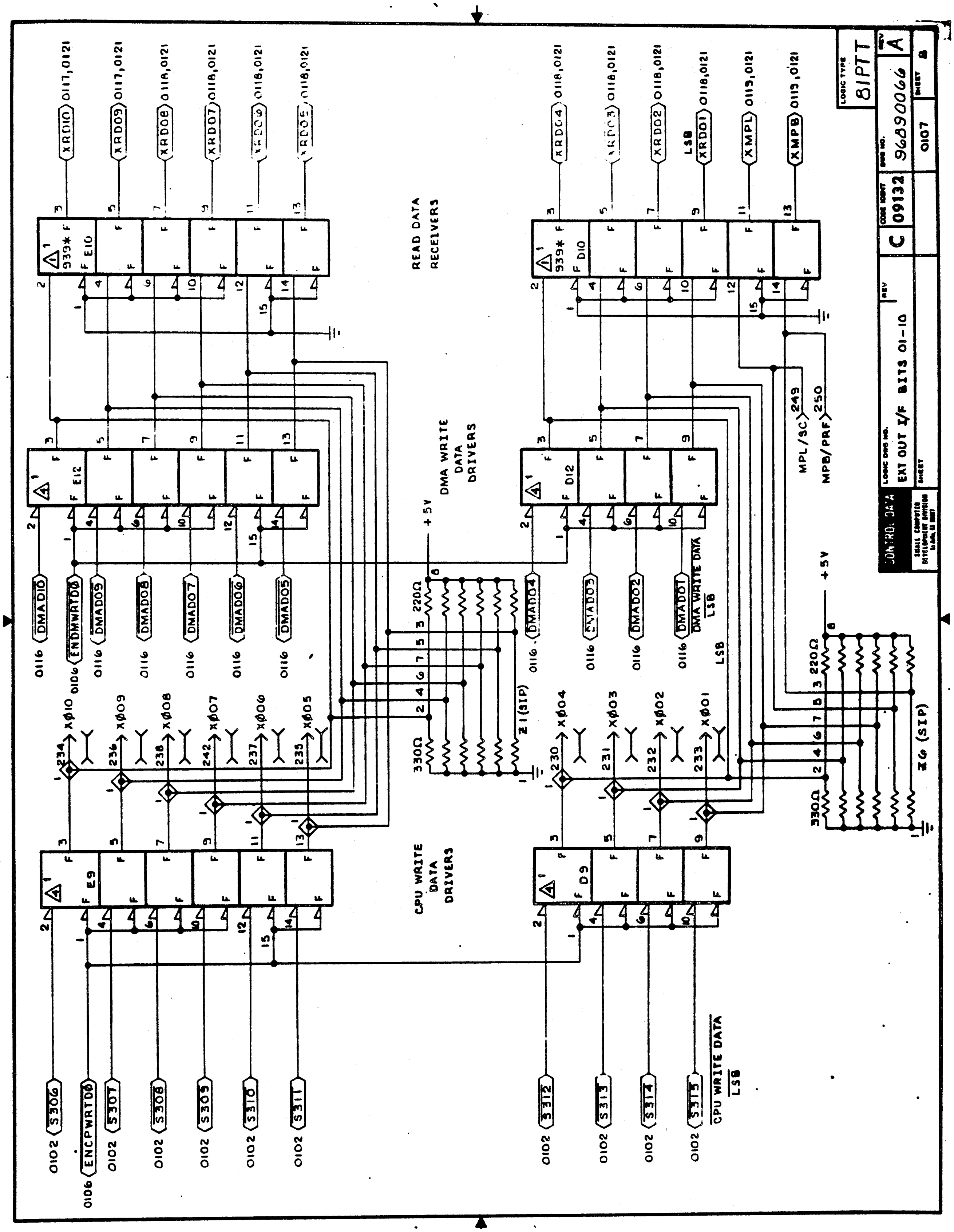

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 8 of 23)

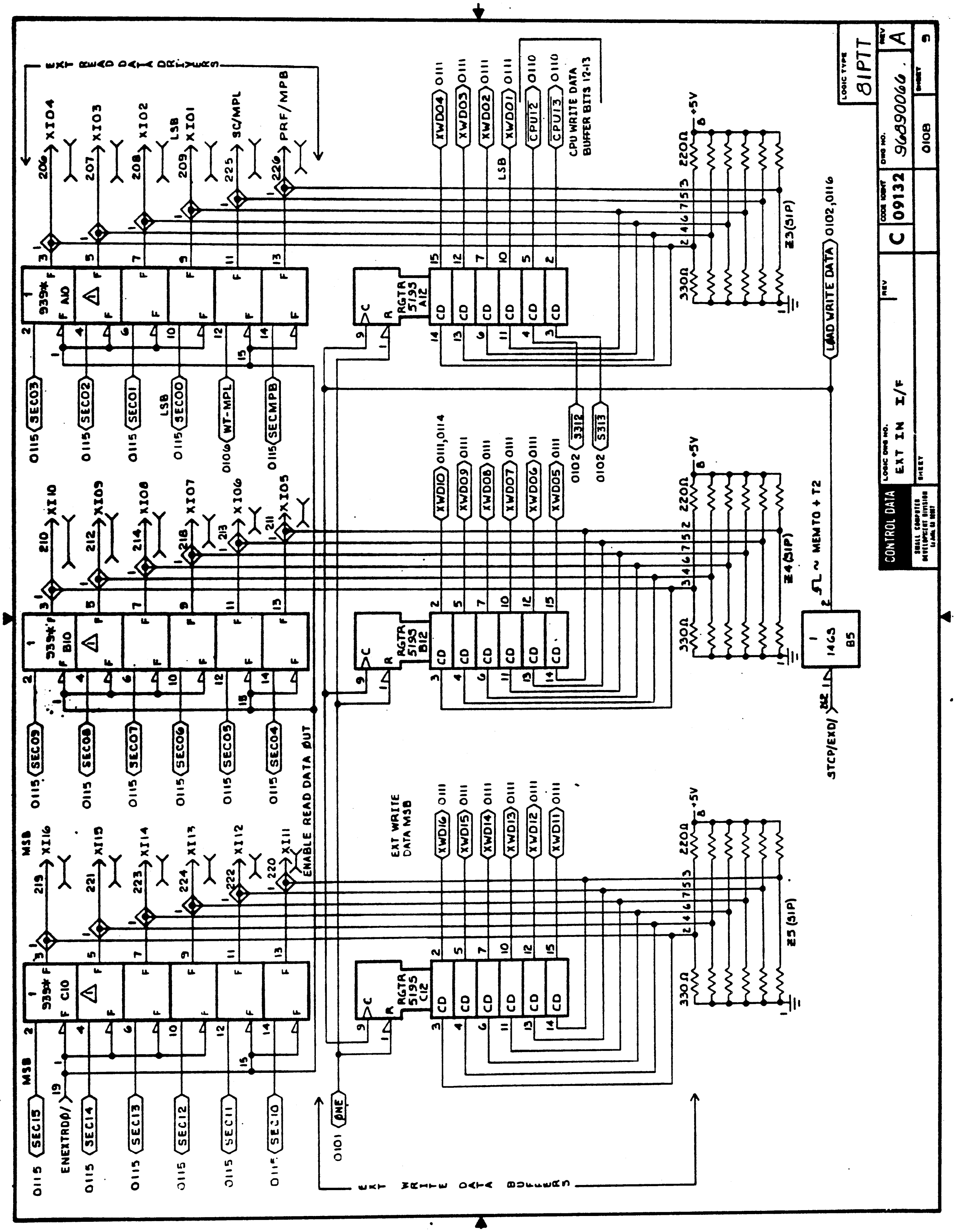

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 9 of 23)

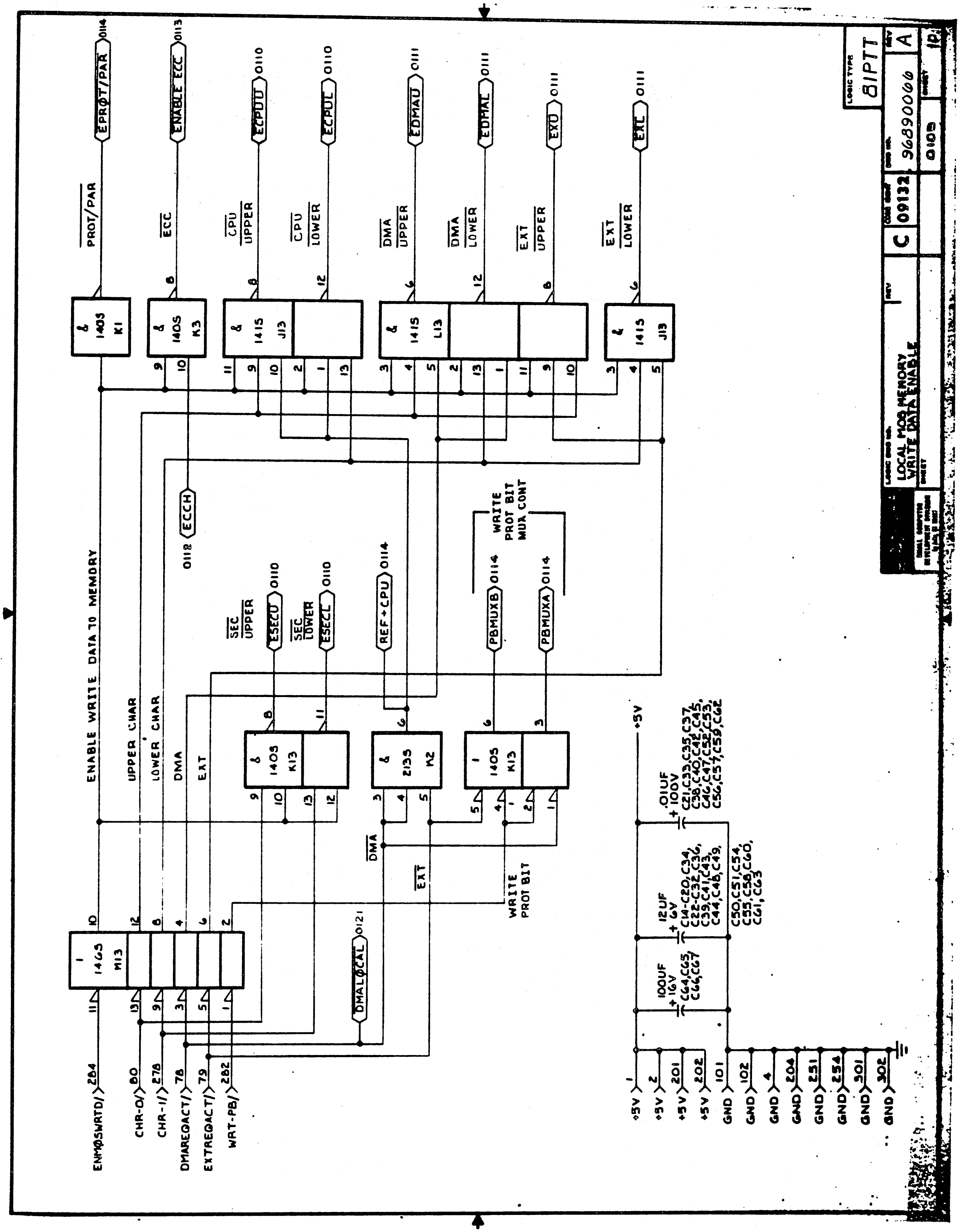

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 10 of 23)

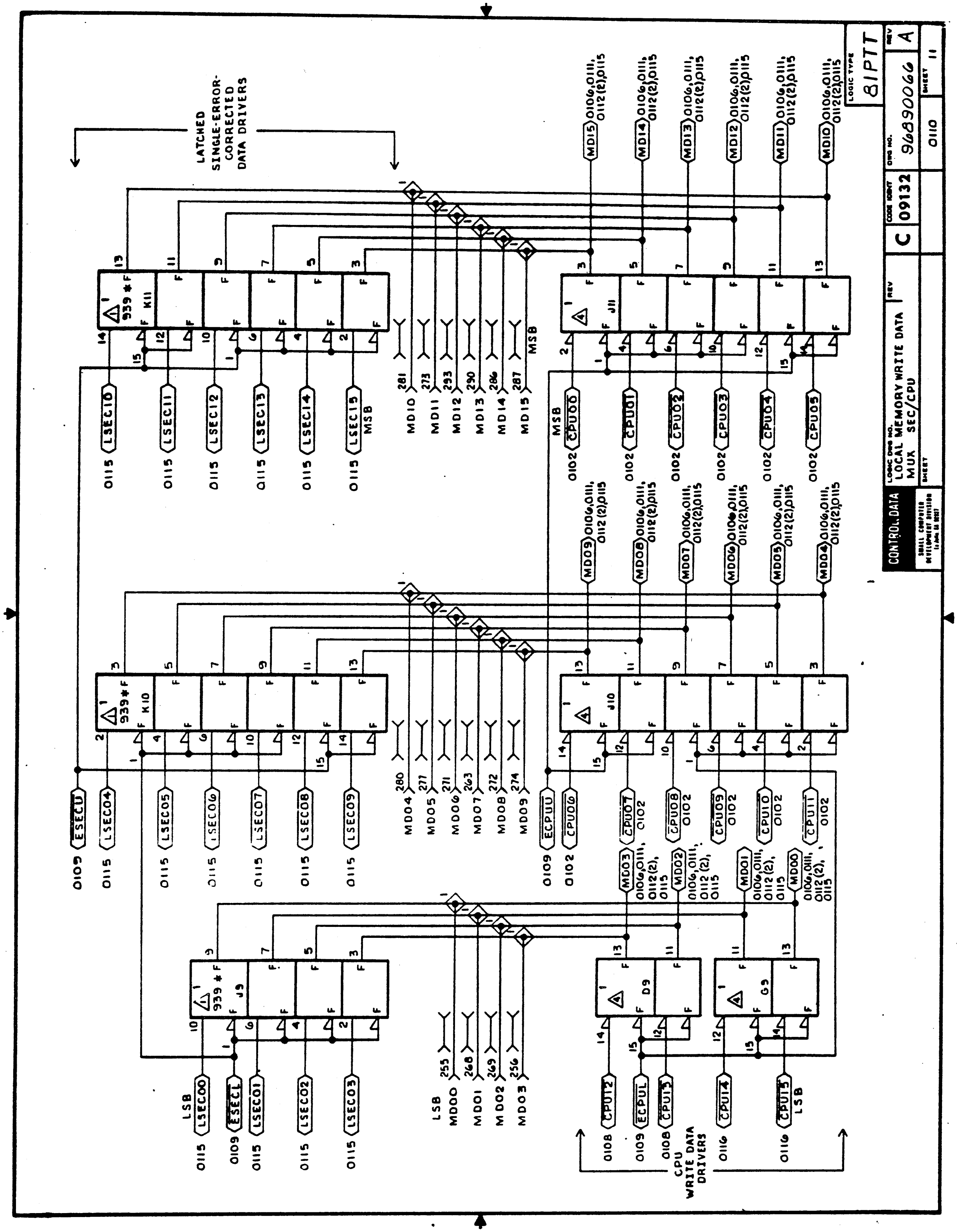

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 11 of 23)

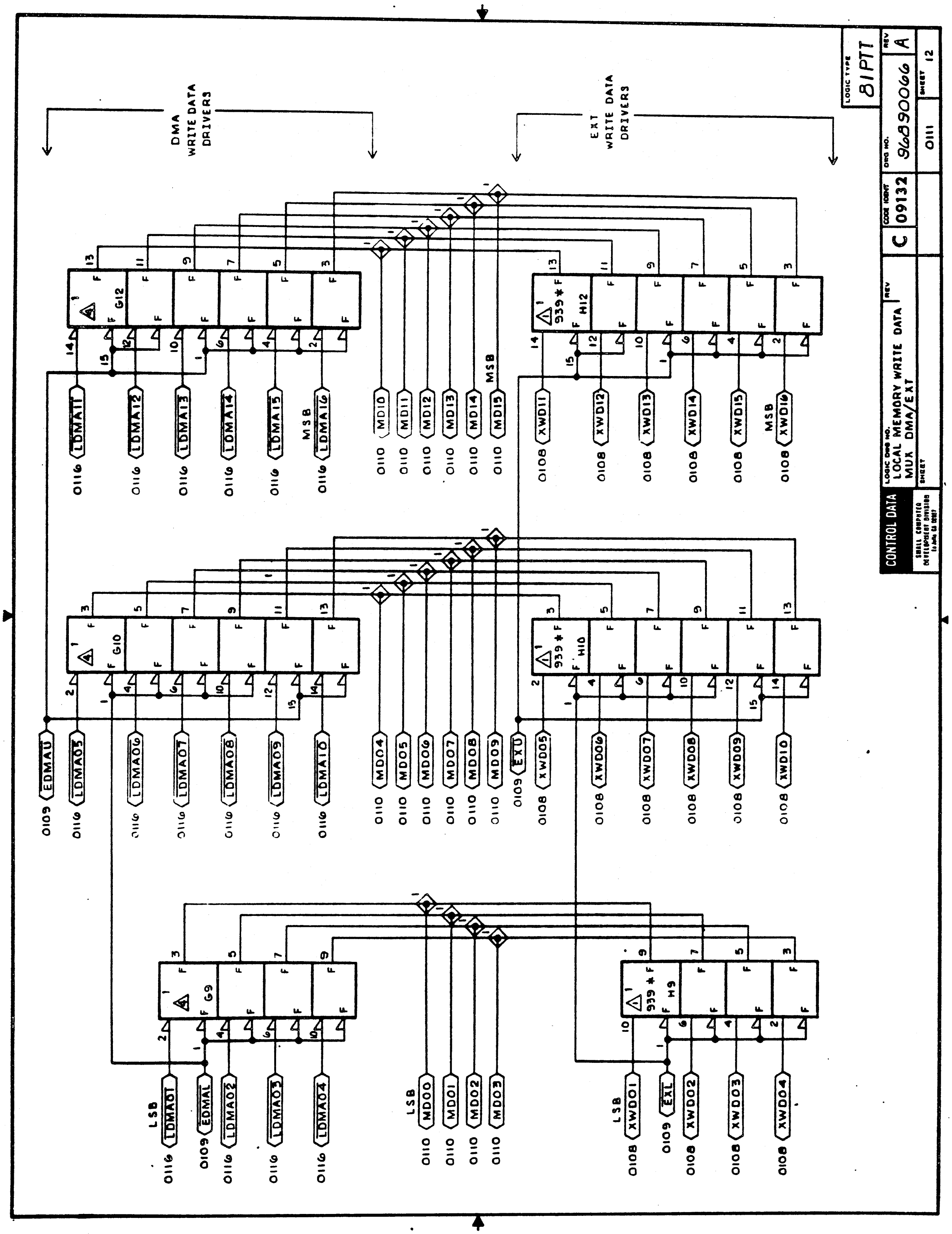

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 12 of 23)

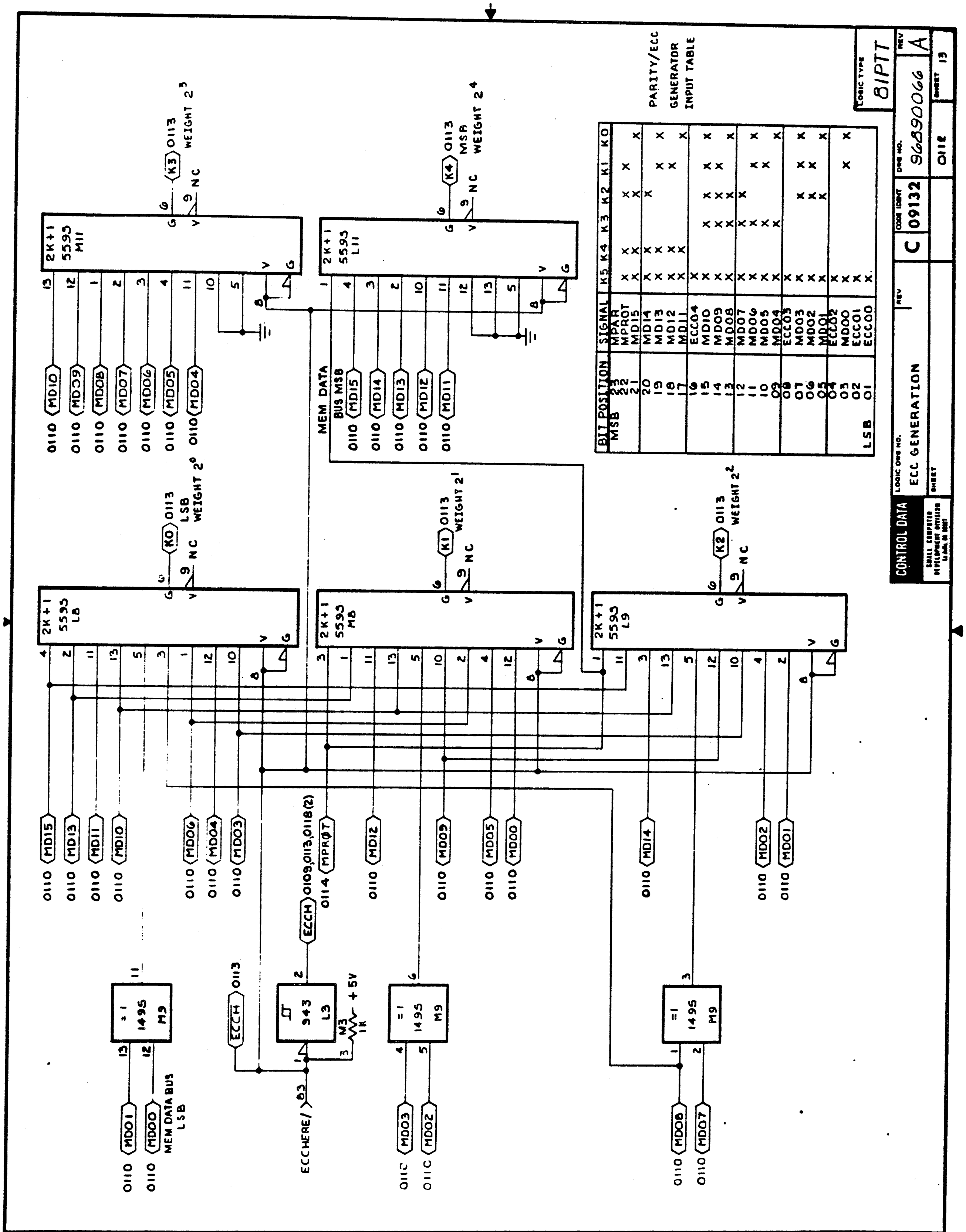

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 13 of 23)

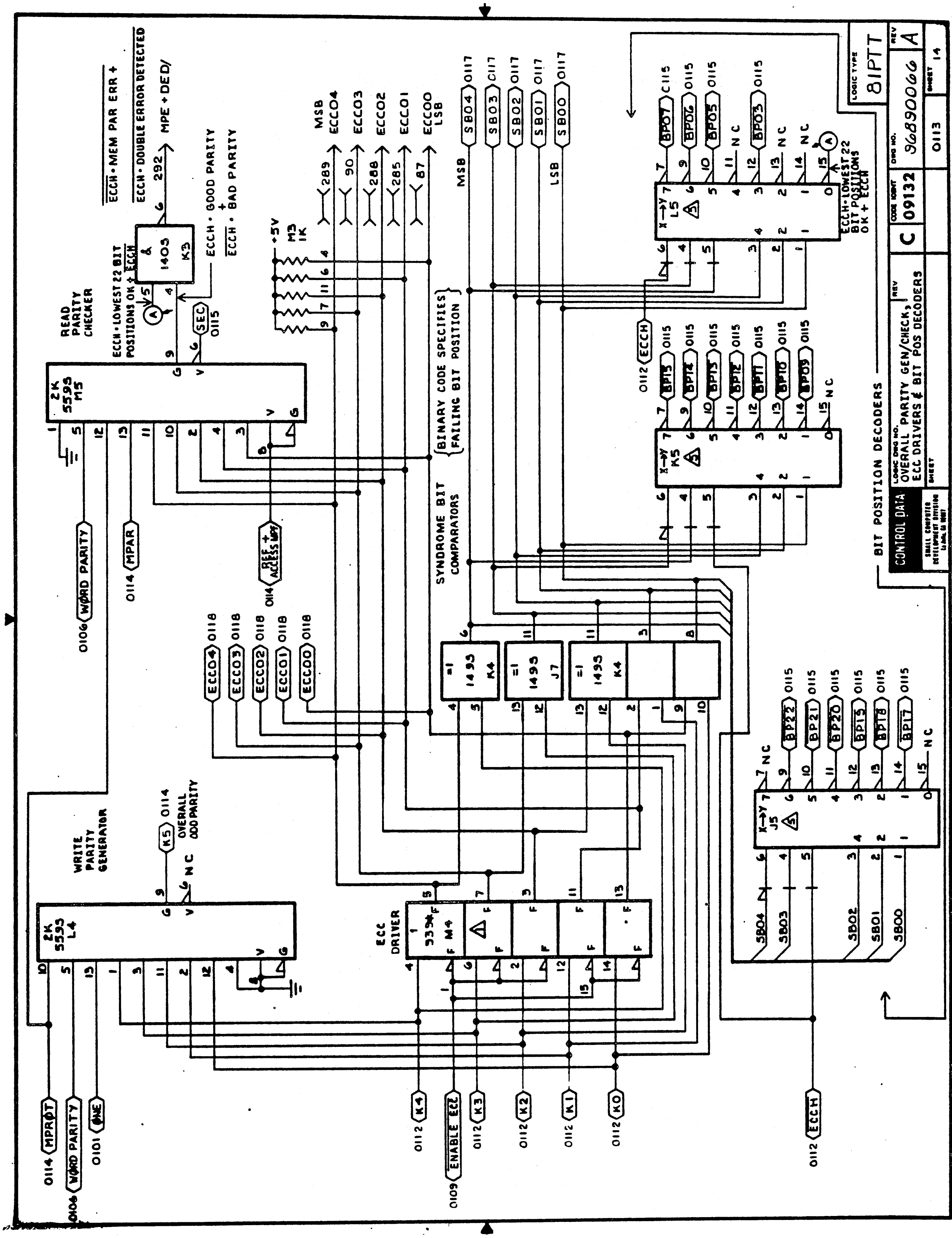

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 14 of 23)

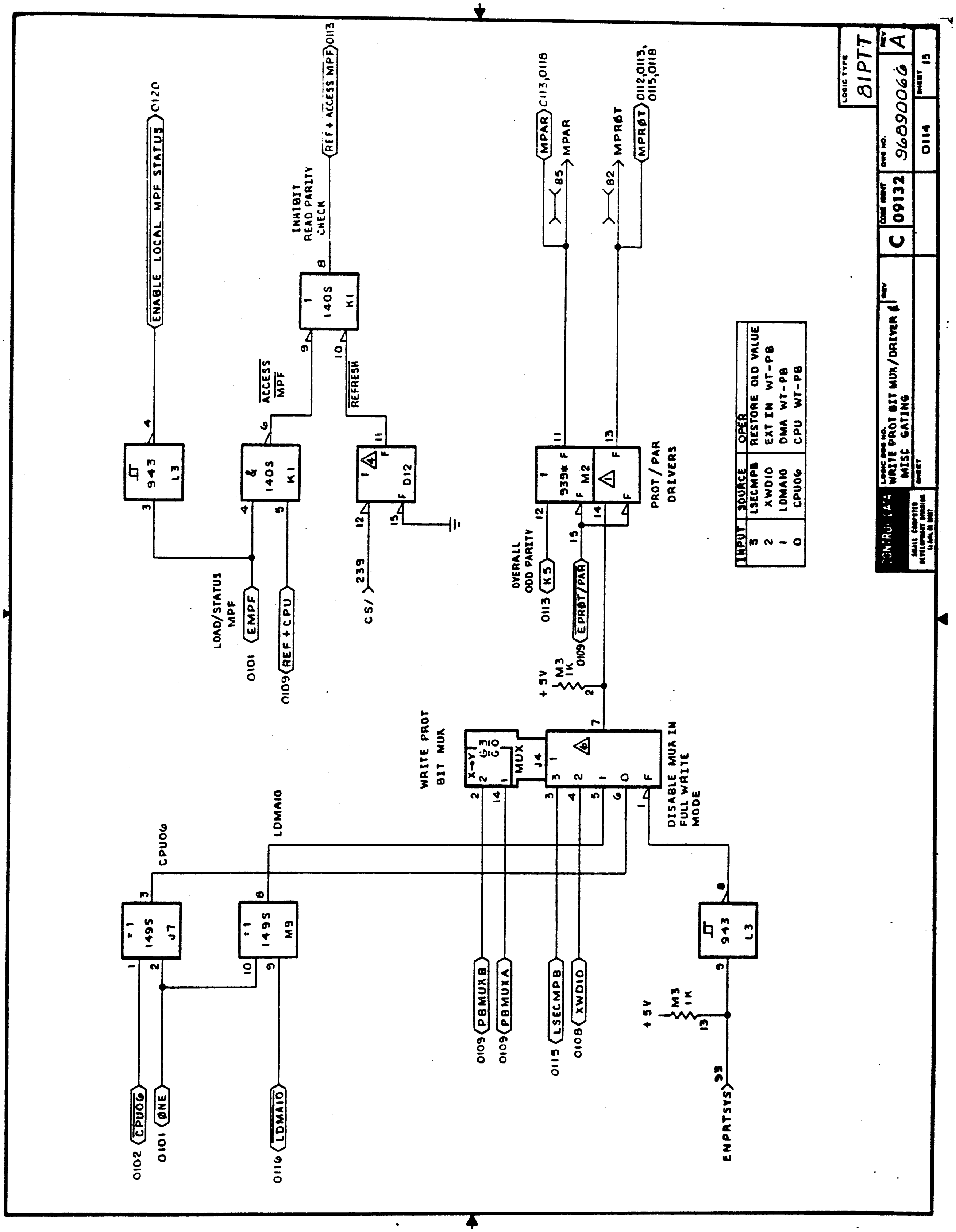

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 15 of 23)

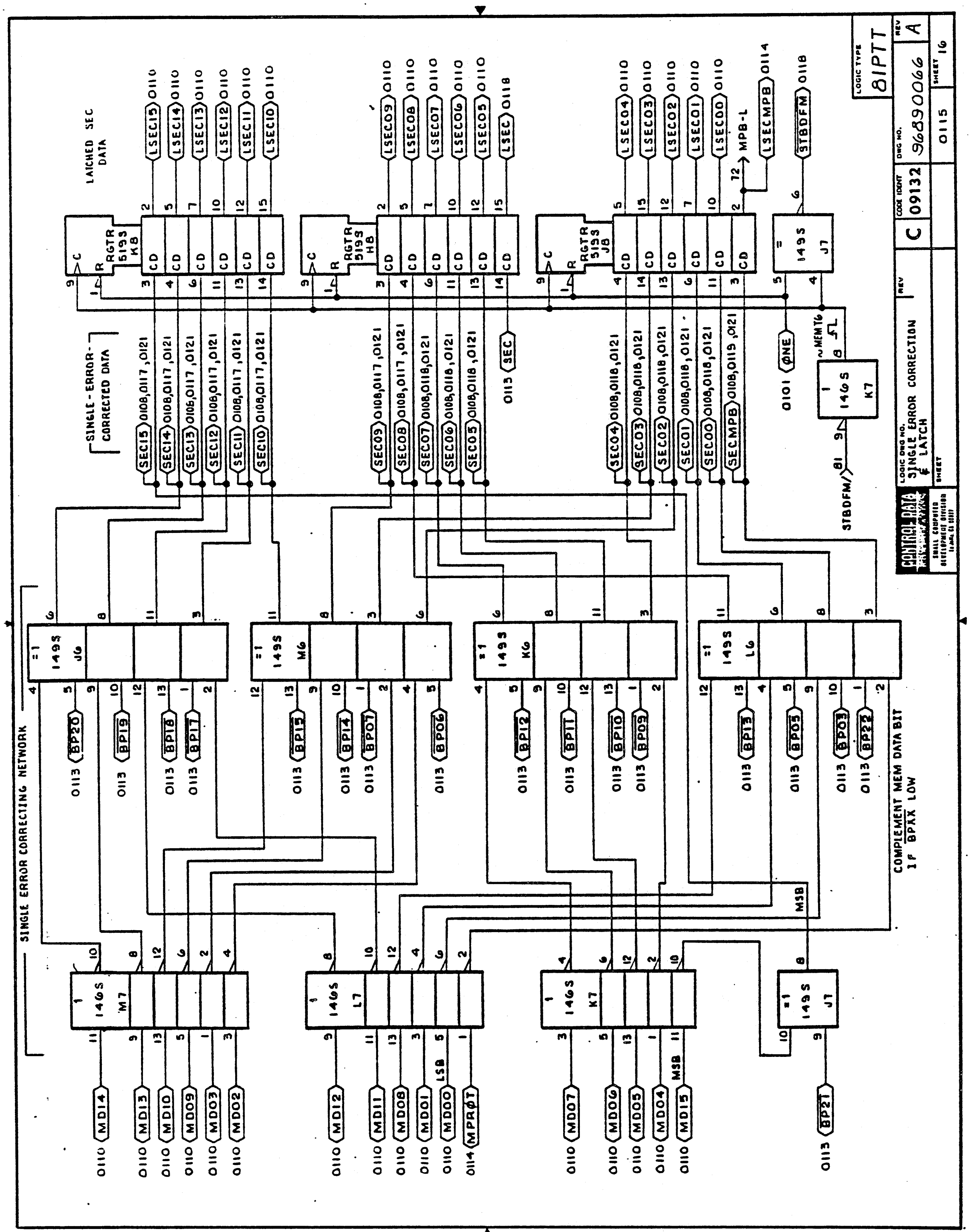

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 16 of 23)

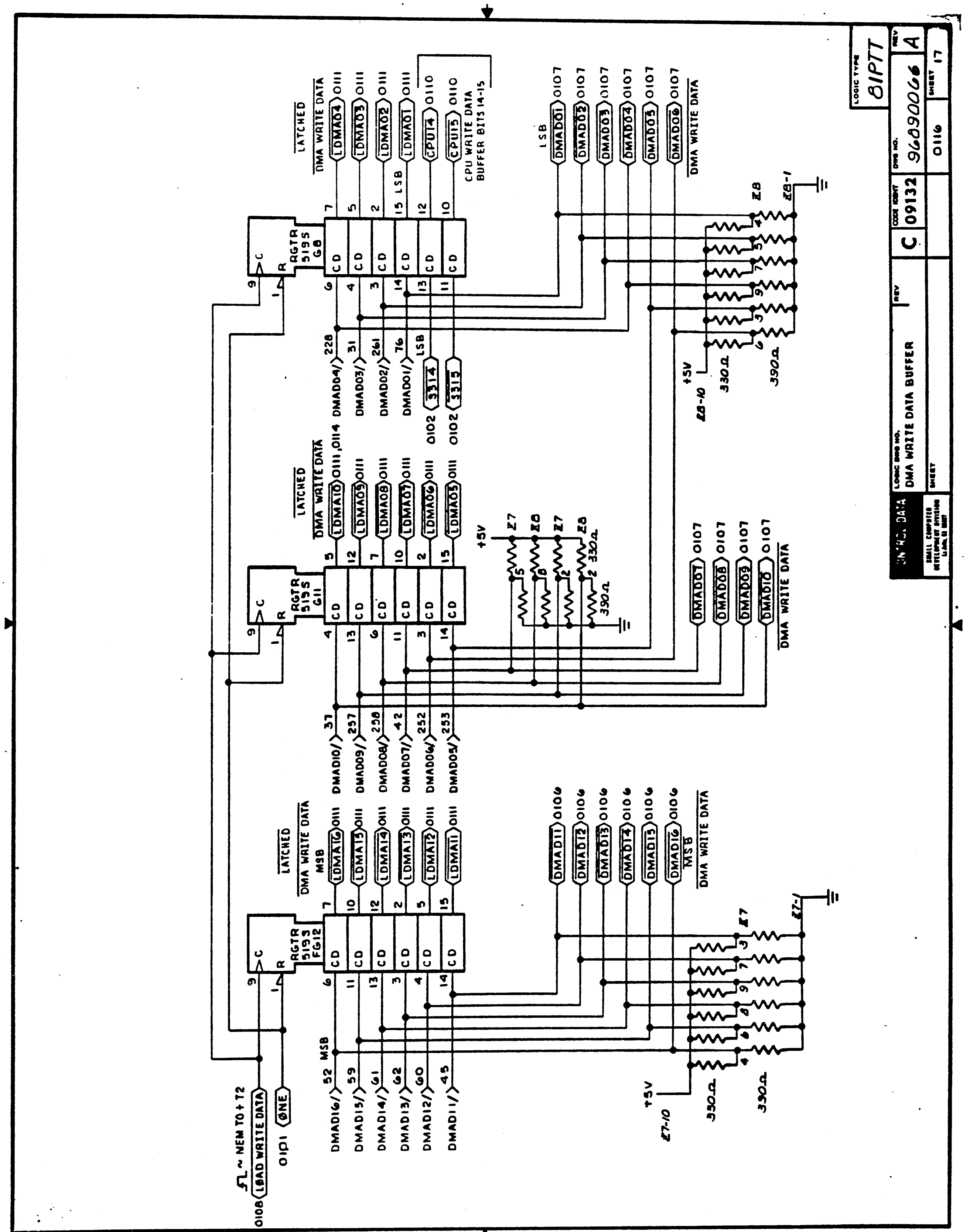

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 17 of 23)

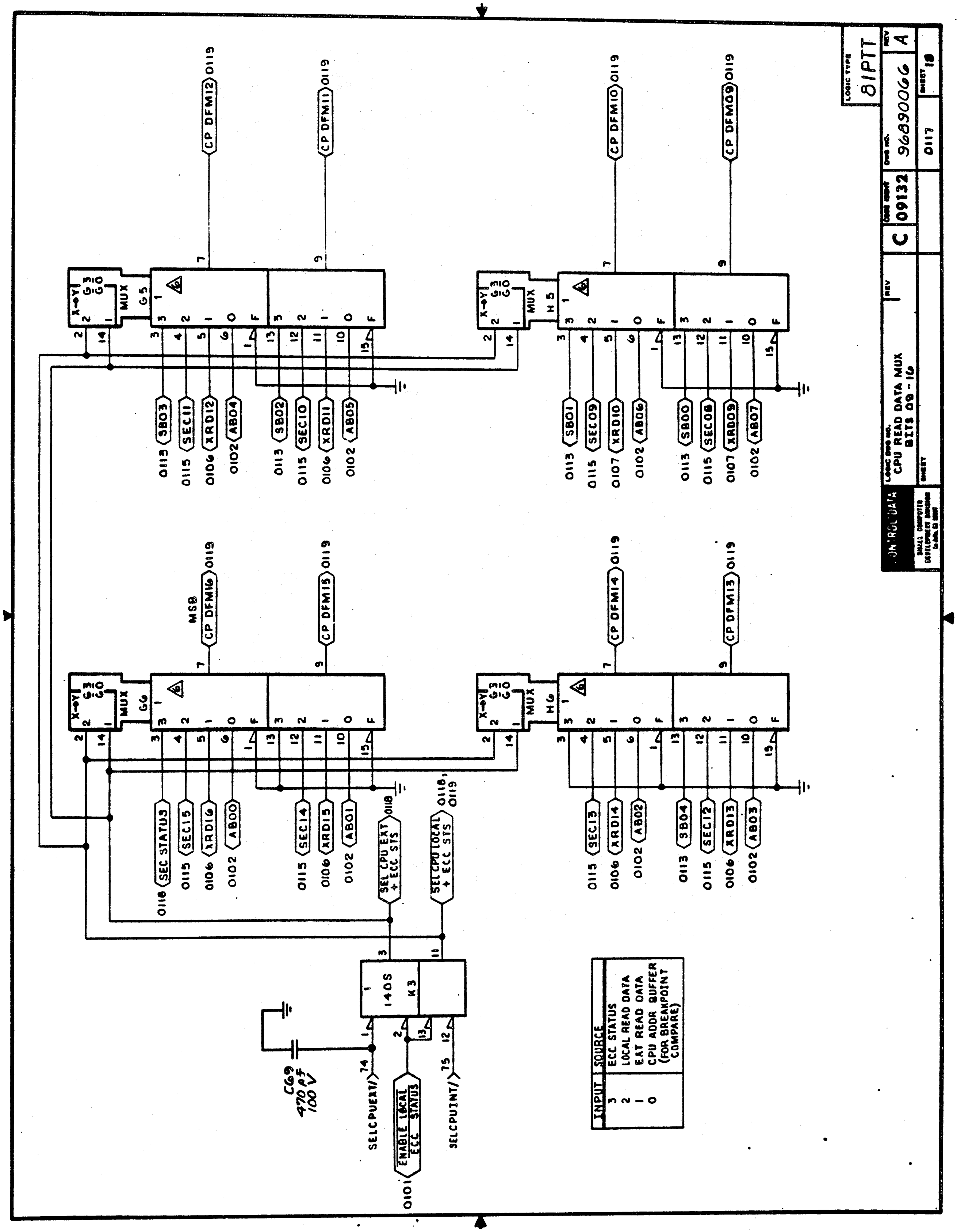

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 18 of 23)

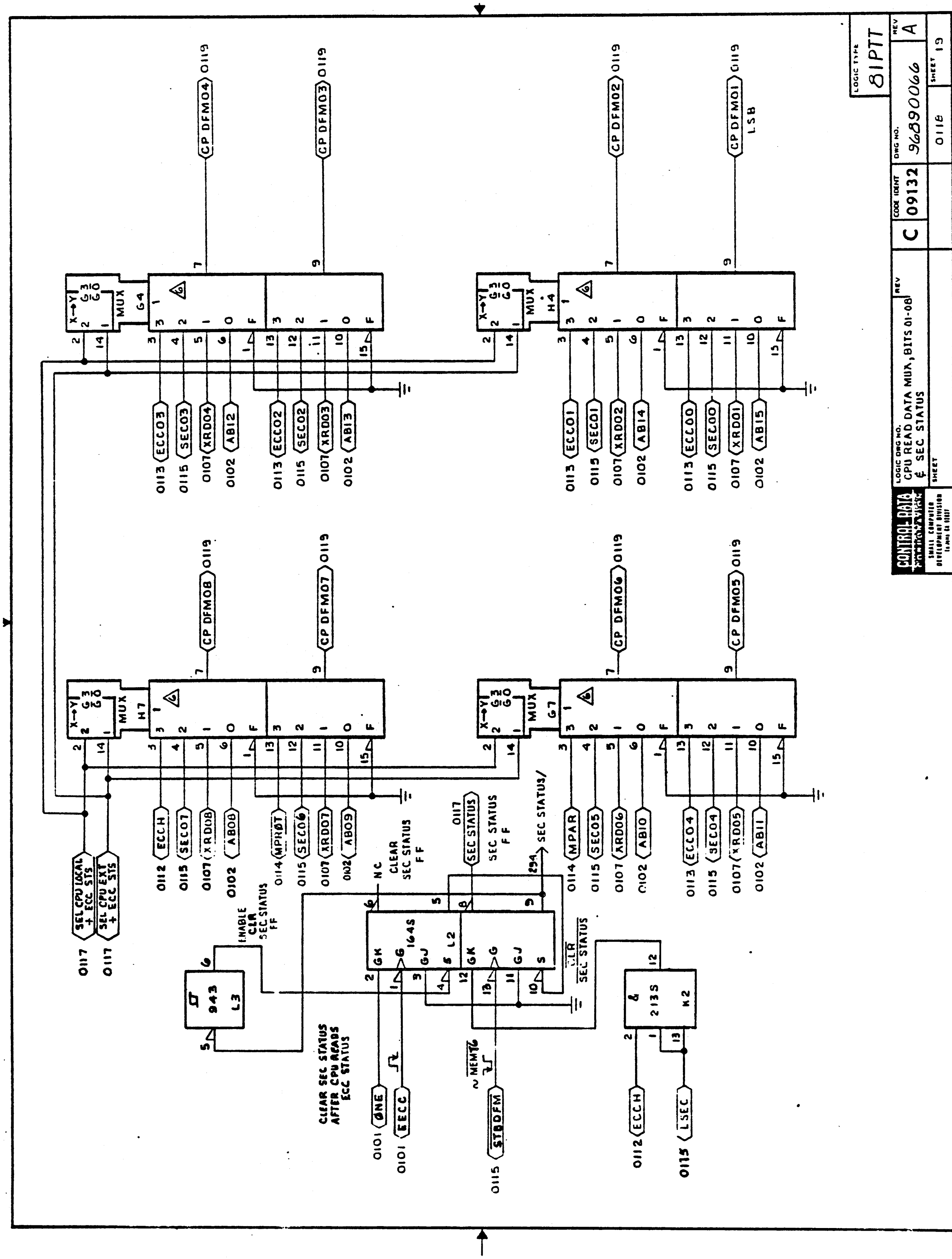

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 19 of 23)

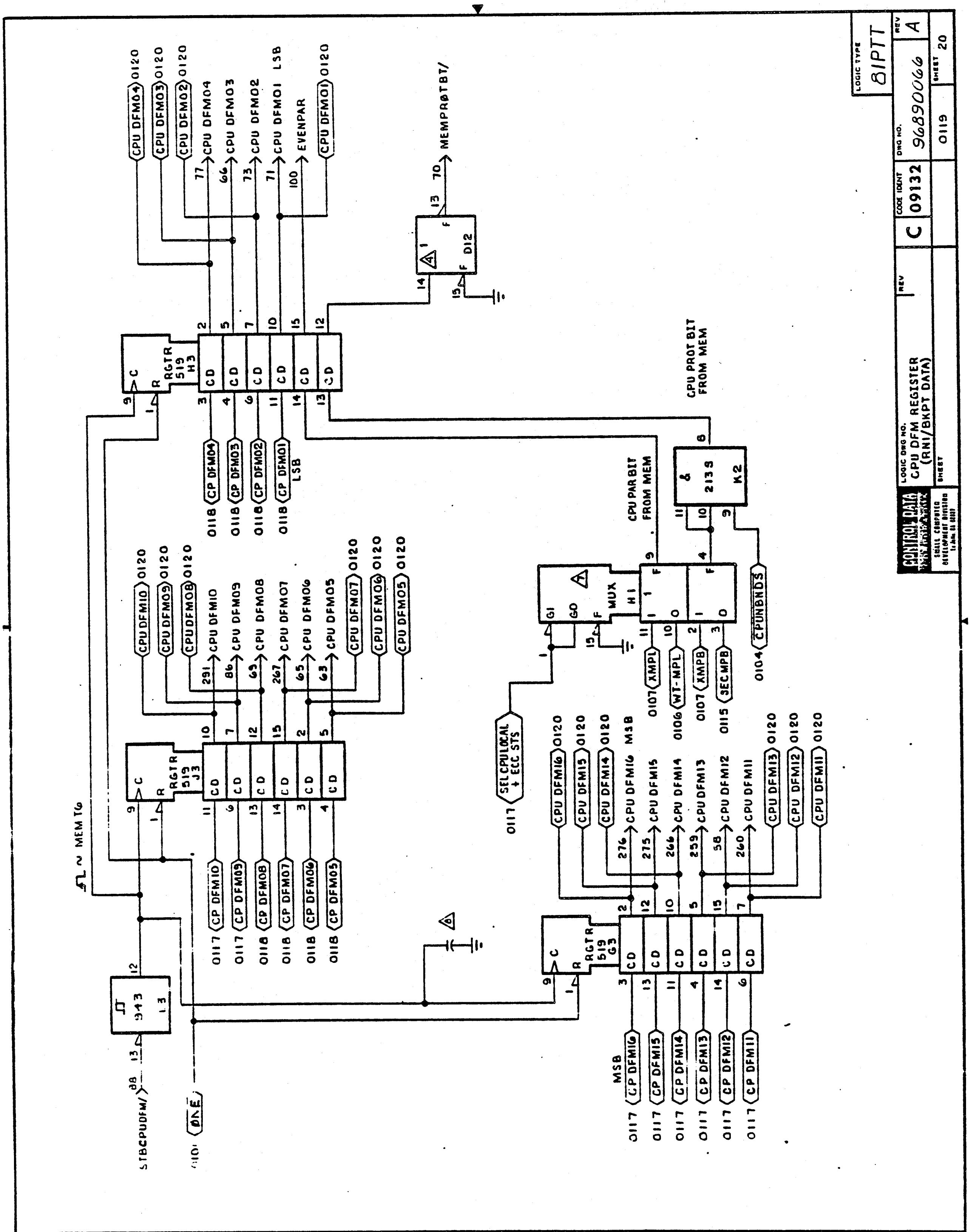

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 20 of 23)

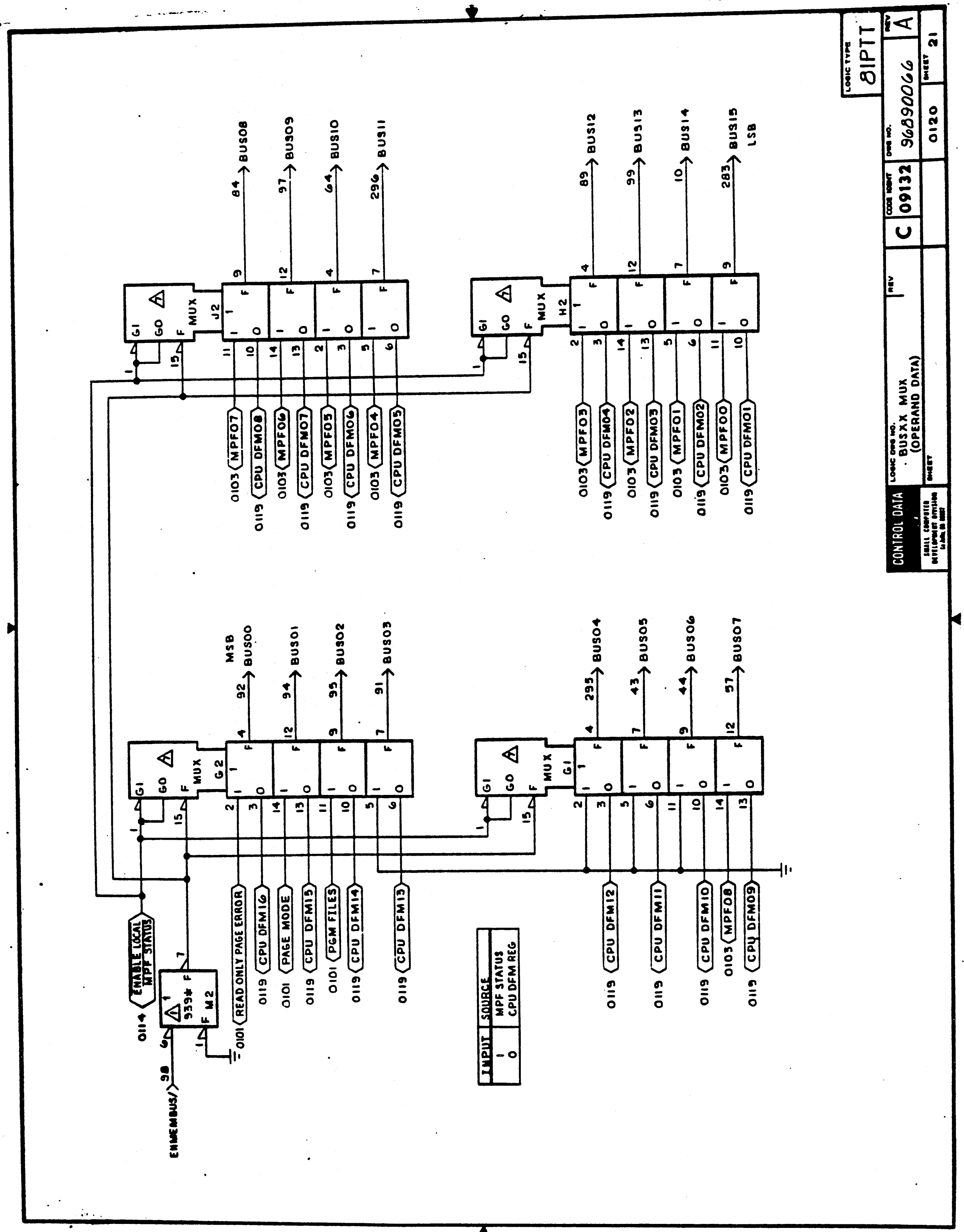

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 21 of 23)

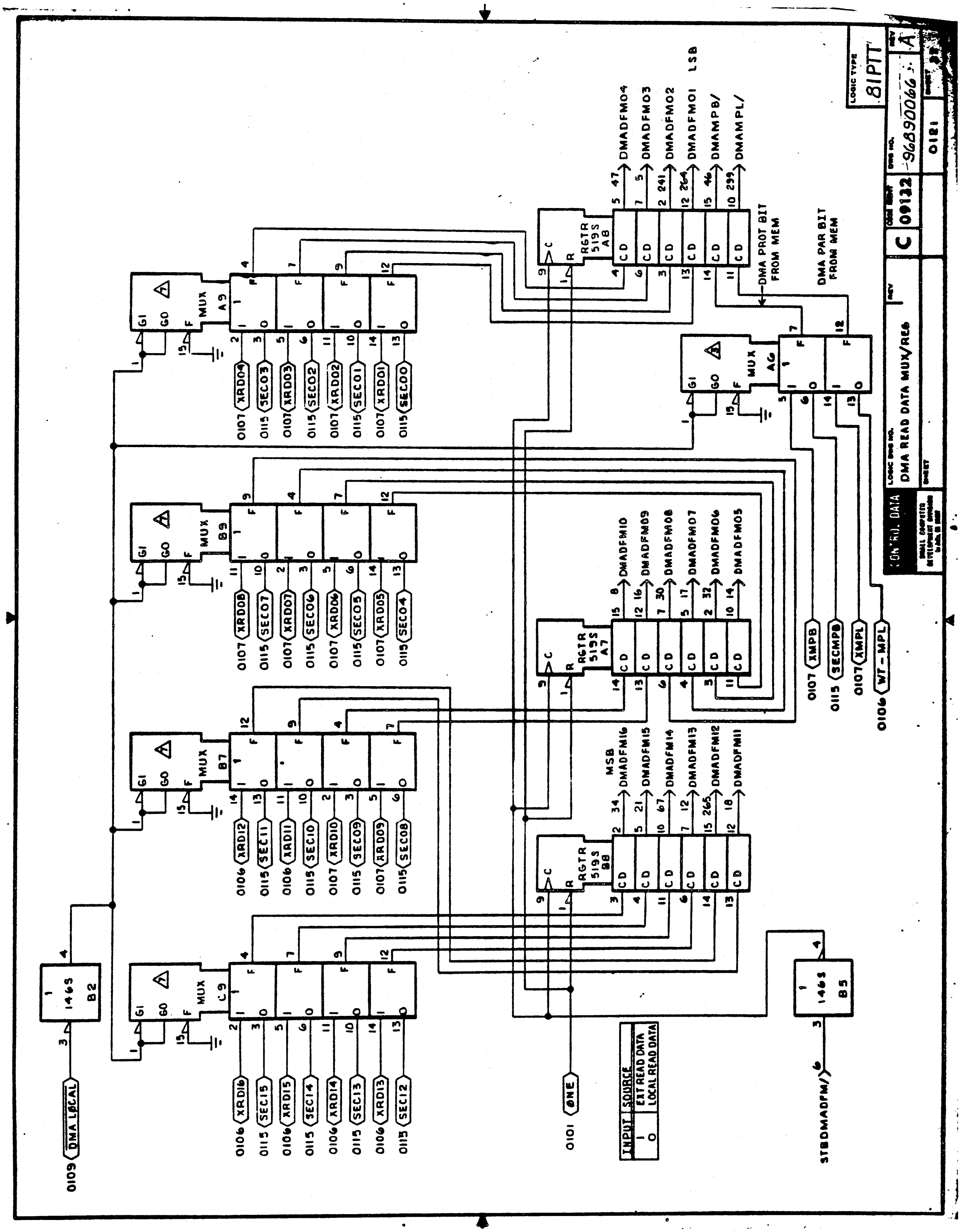

Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 22 of 23)

ITD STD 1

DWN	Ben Roberts	1-27-82	CONTROL DATA CORPORATION	TITLE LOGIC DIAGRAM - MOS MEMORY INTF (DATA)
CHKD	B. Gage	1-27-82	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA. 92037	
ENG				FIRST USED ON
MFG				
APPR		4-7-82	CODE IDENT 09132	

PREFIX	DOCUMENT NO.	REV.
DR	96890066	A
	SHEET 1 OF 1	

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS22172	CL. A. RELEASED	BR	4-2-82		AW

NOTES:

DETACHED LISTS

AA3100 REV. 8/71

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Figure 5-14. MOS Memory Interface Data (PWA 96890065) Logic Diagram (Sheet 23 of 23)

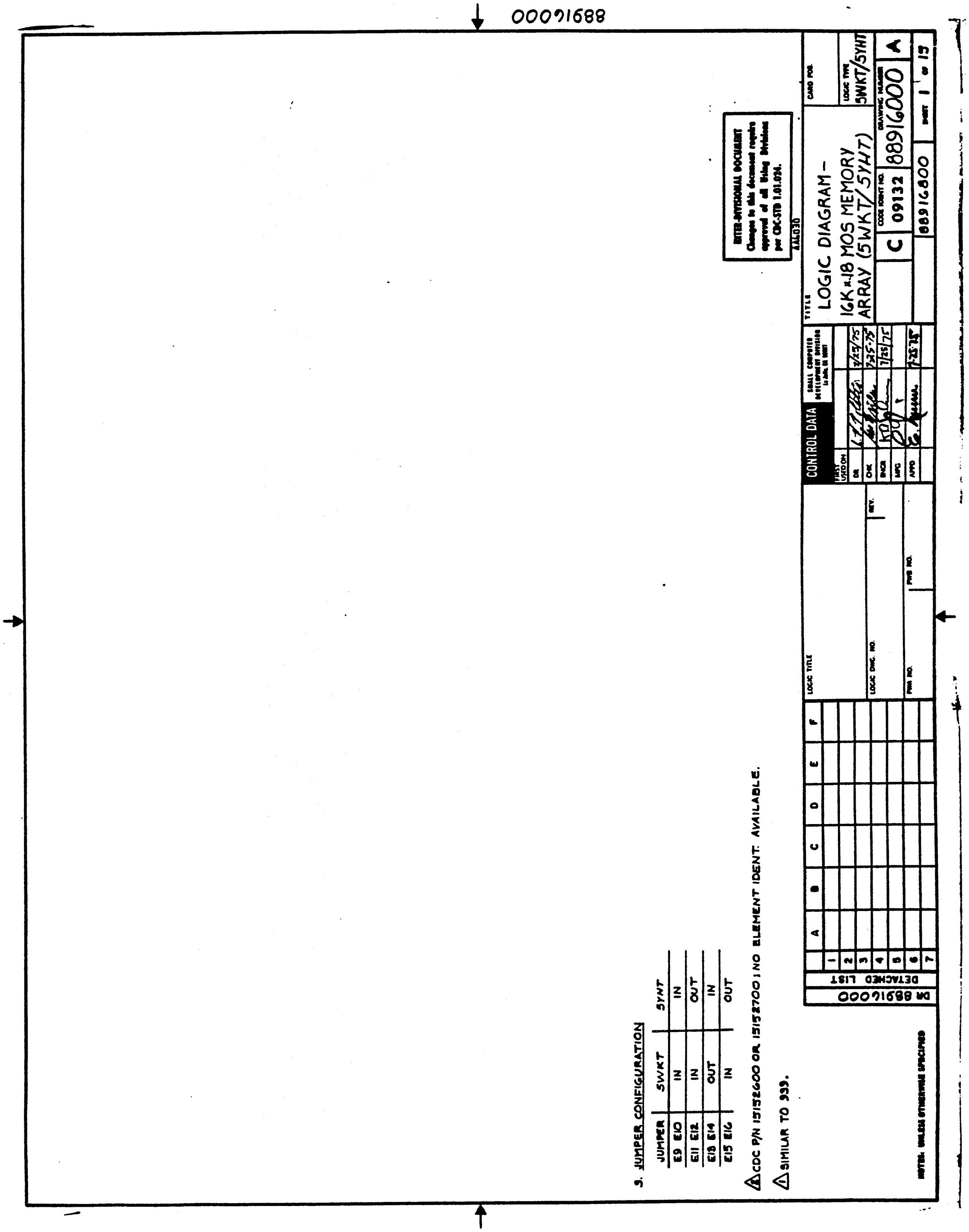

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 1 of 16)

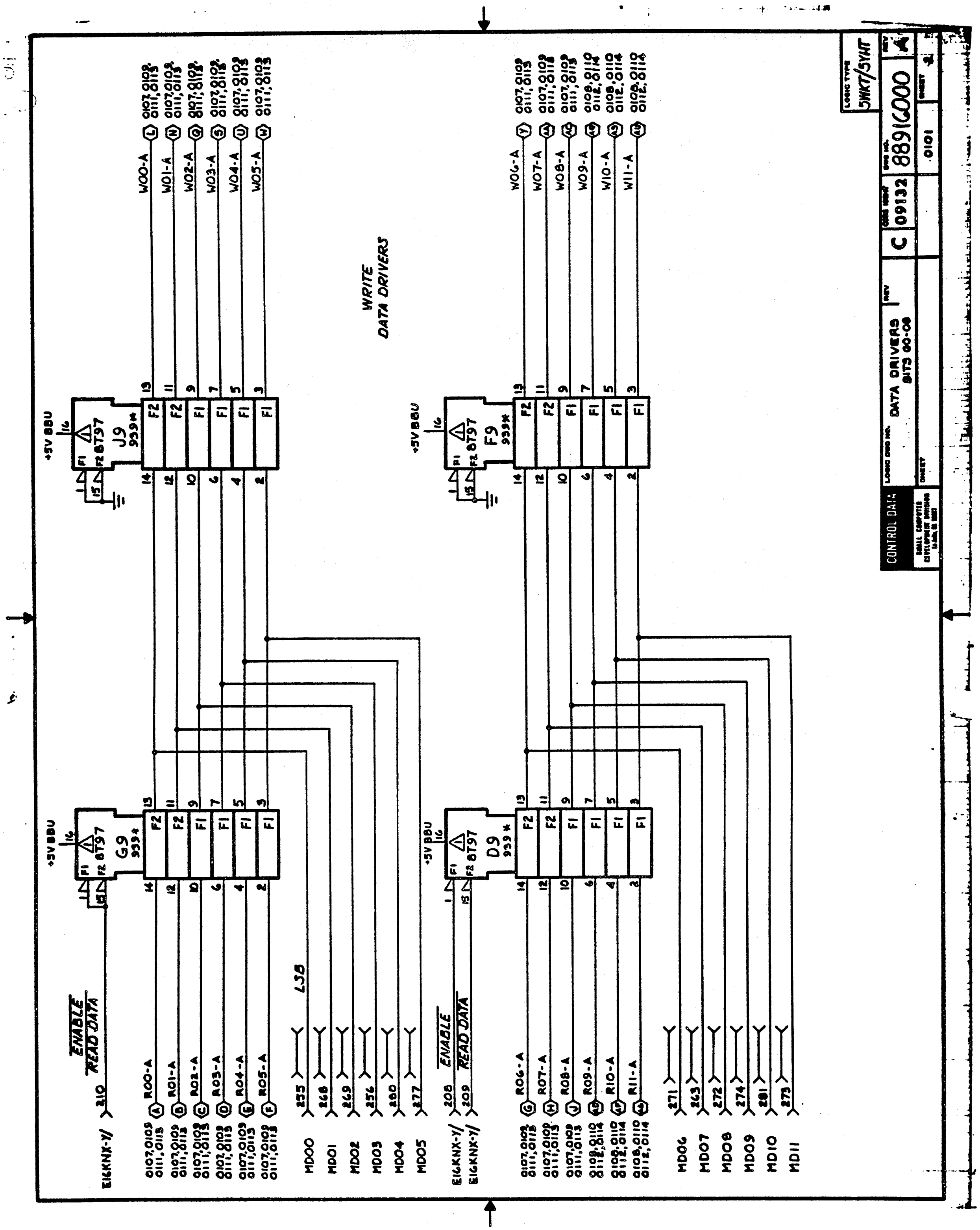

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 2 of 16)

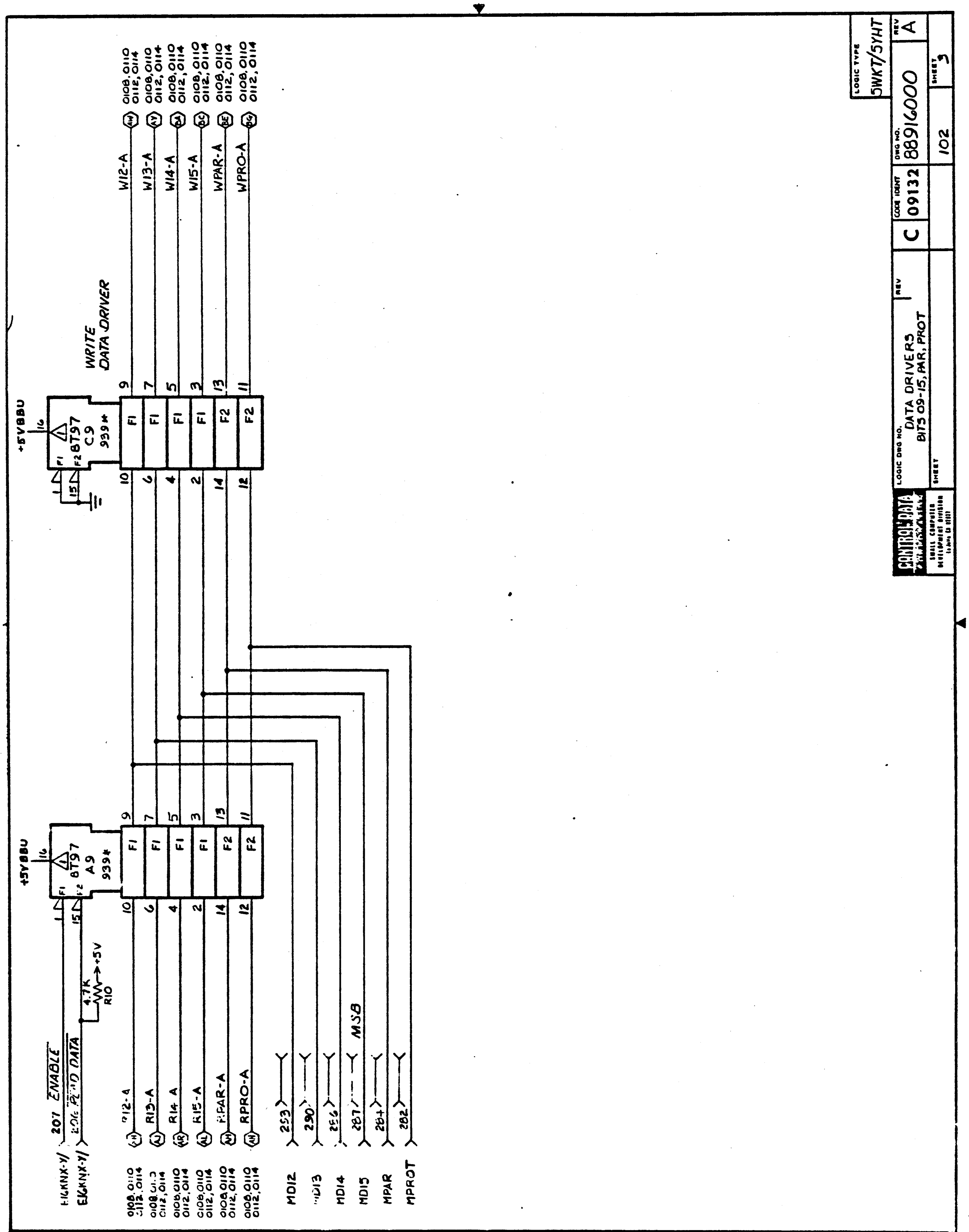

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 3 of 16)

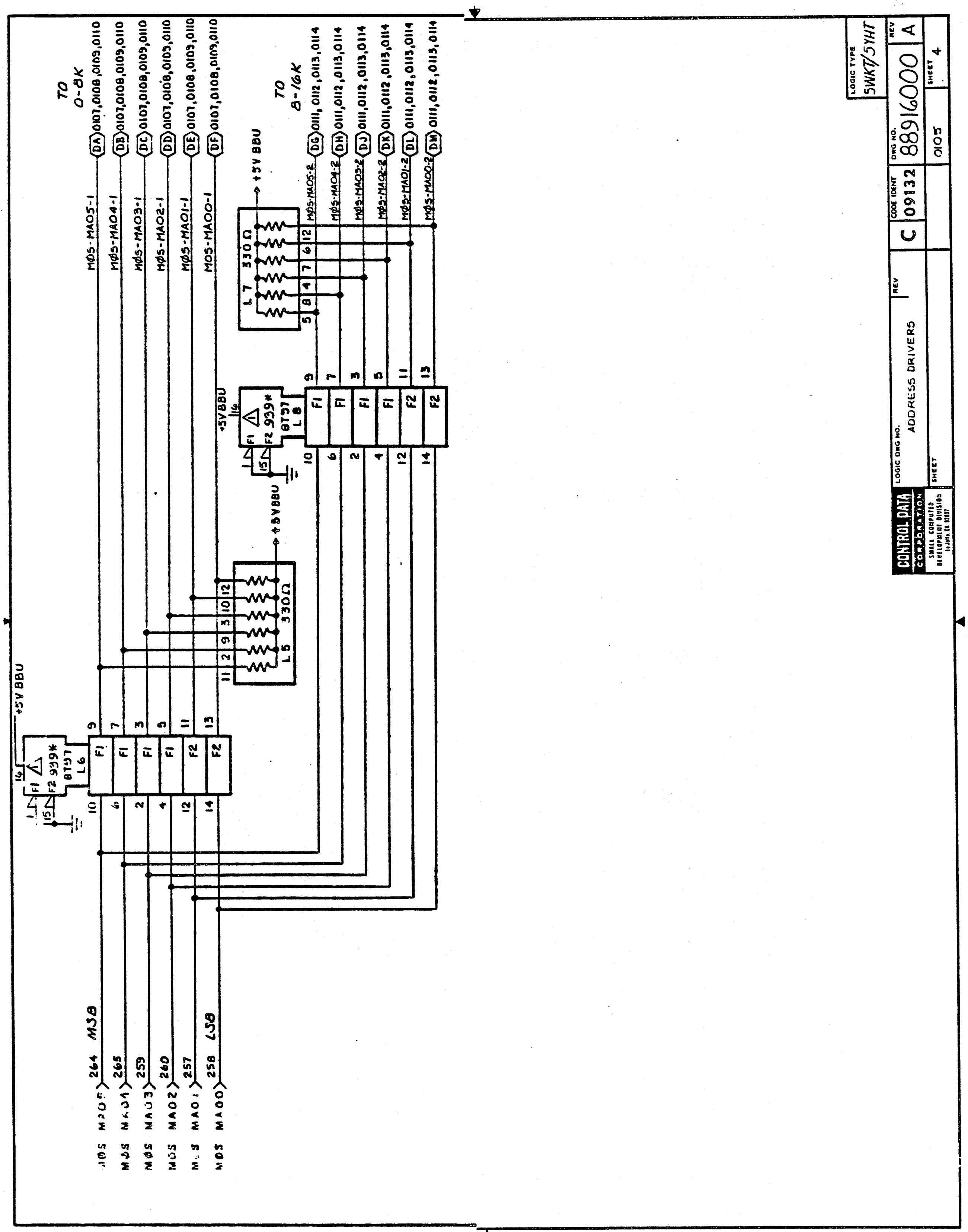

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 4 of 16)

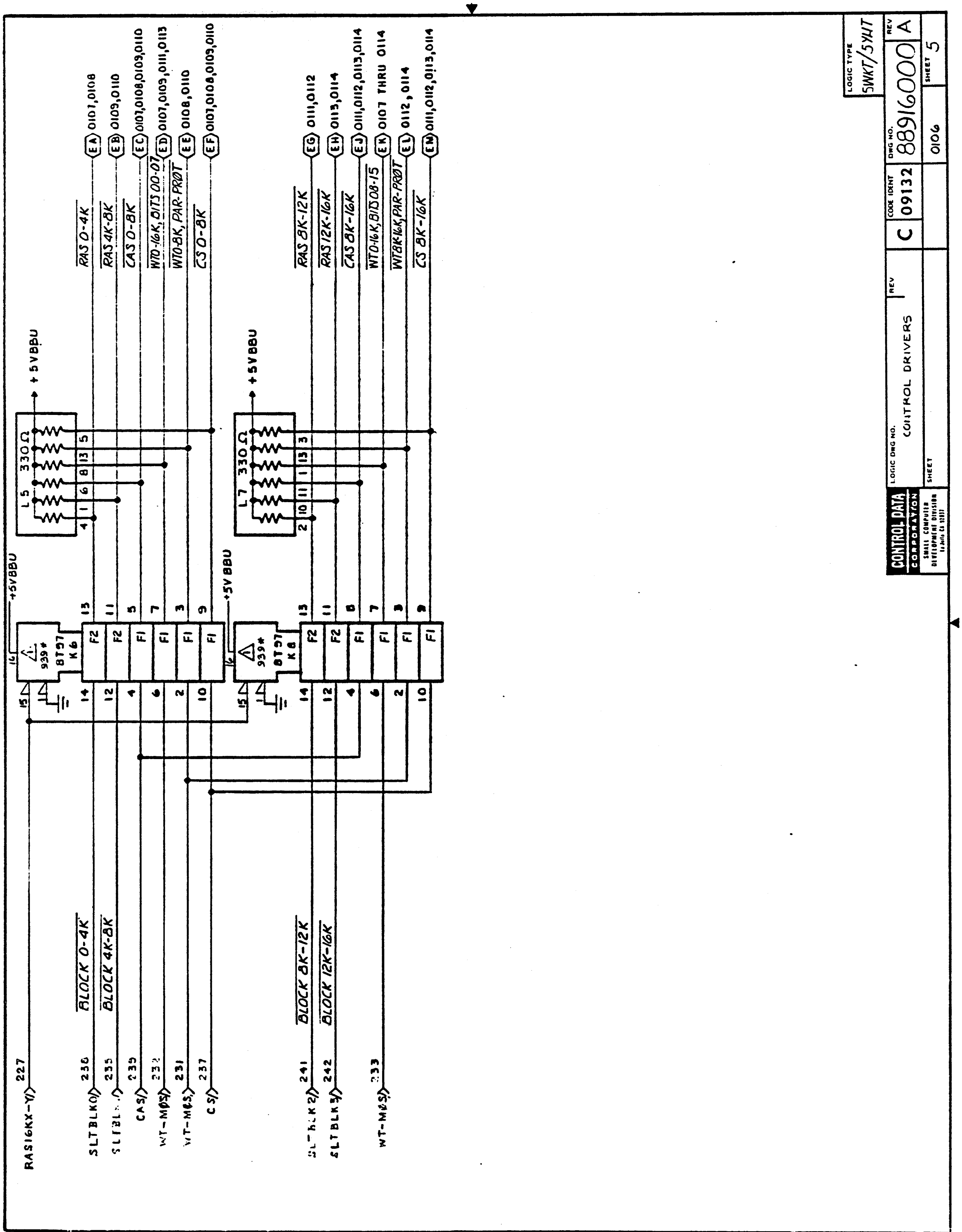

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 5 of 16)

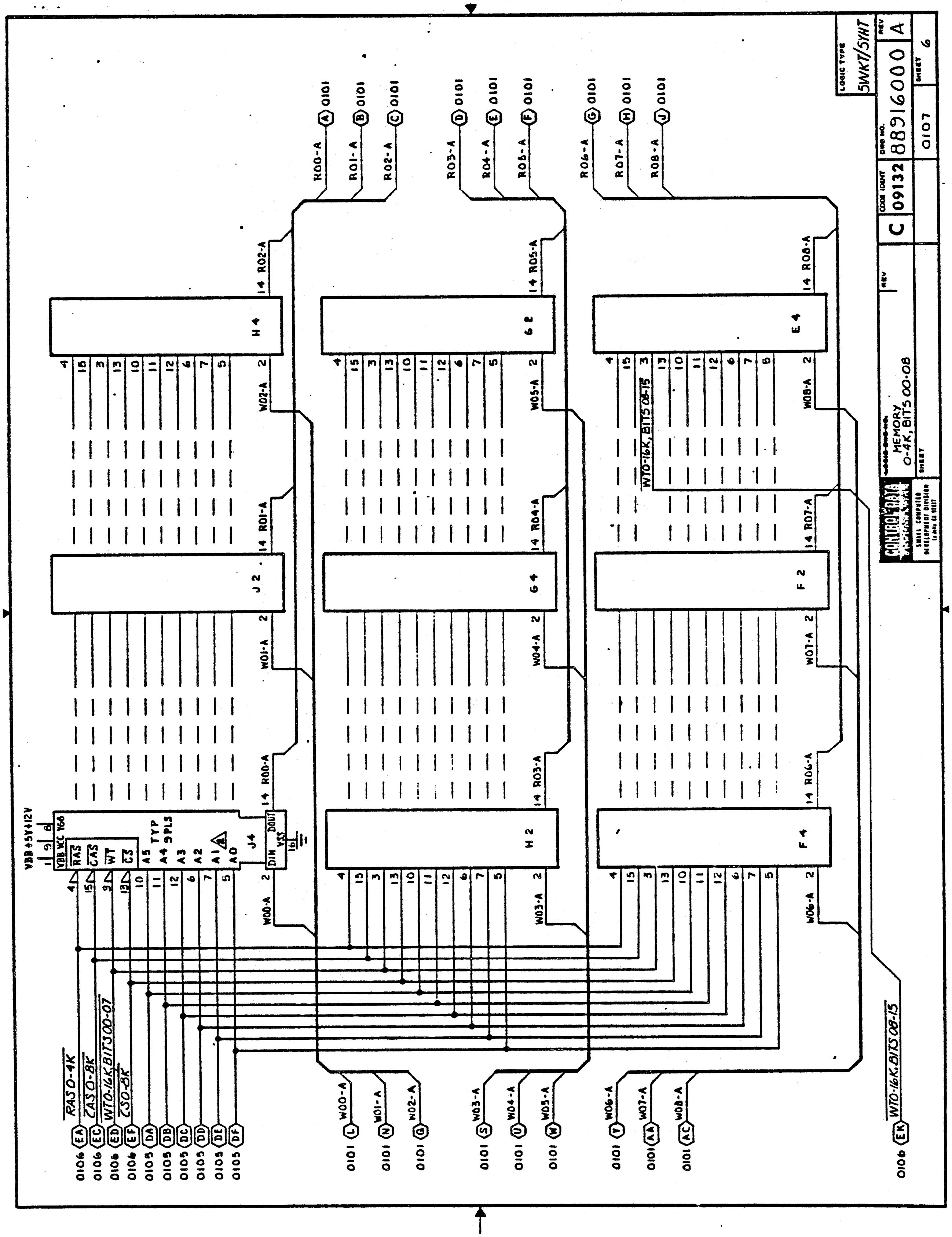

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 6 of 16)

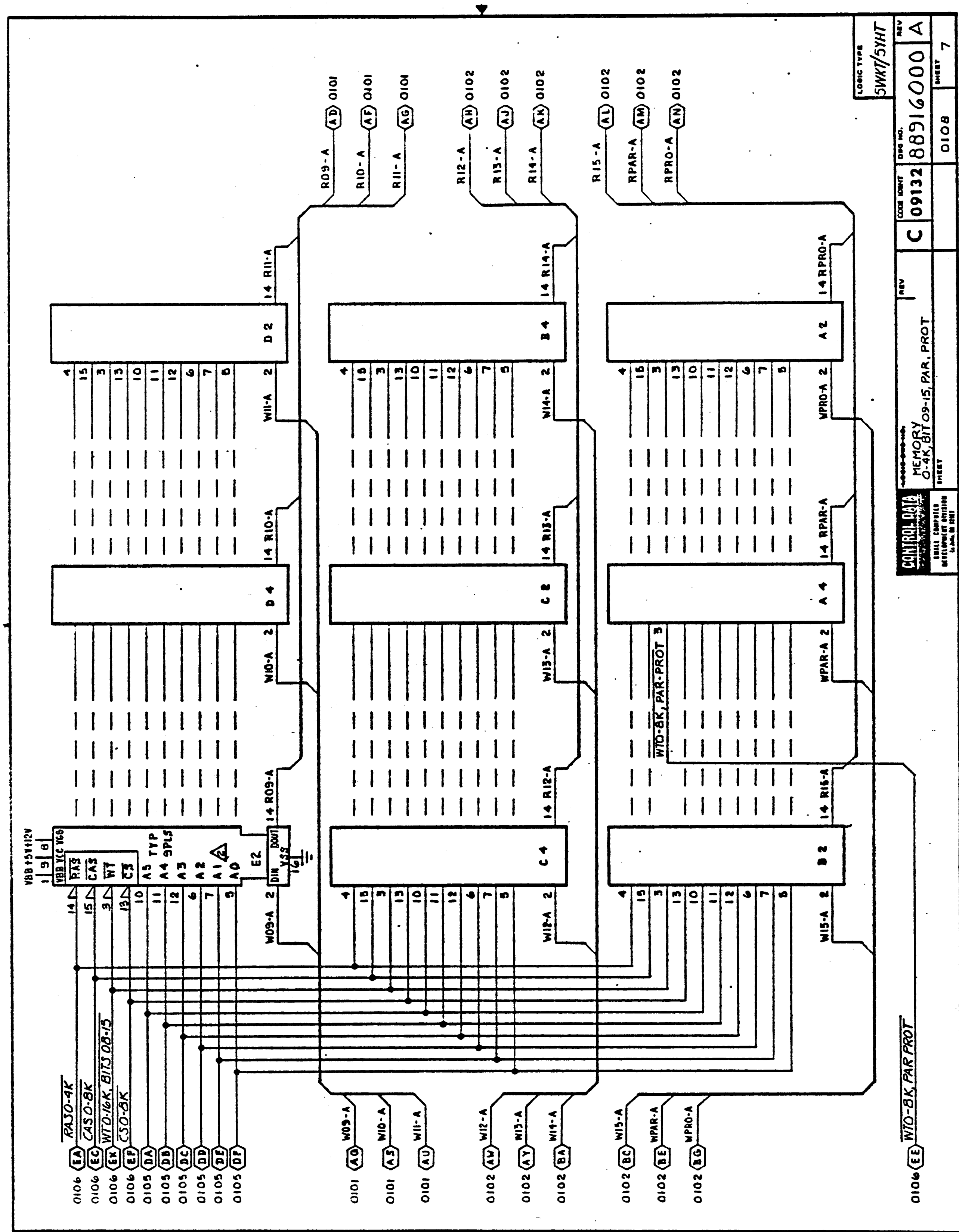

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 7 of 16)

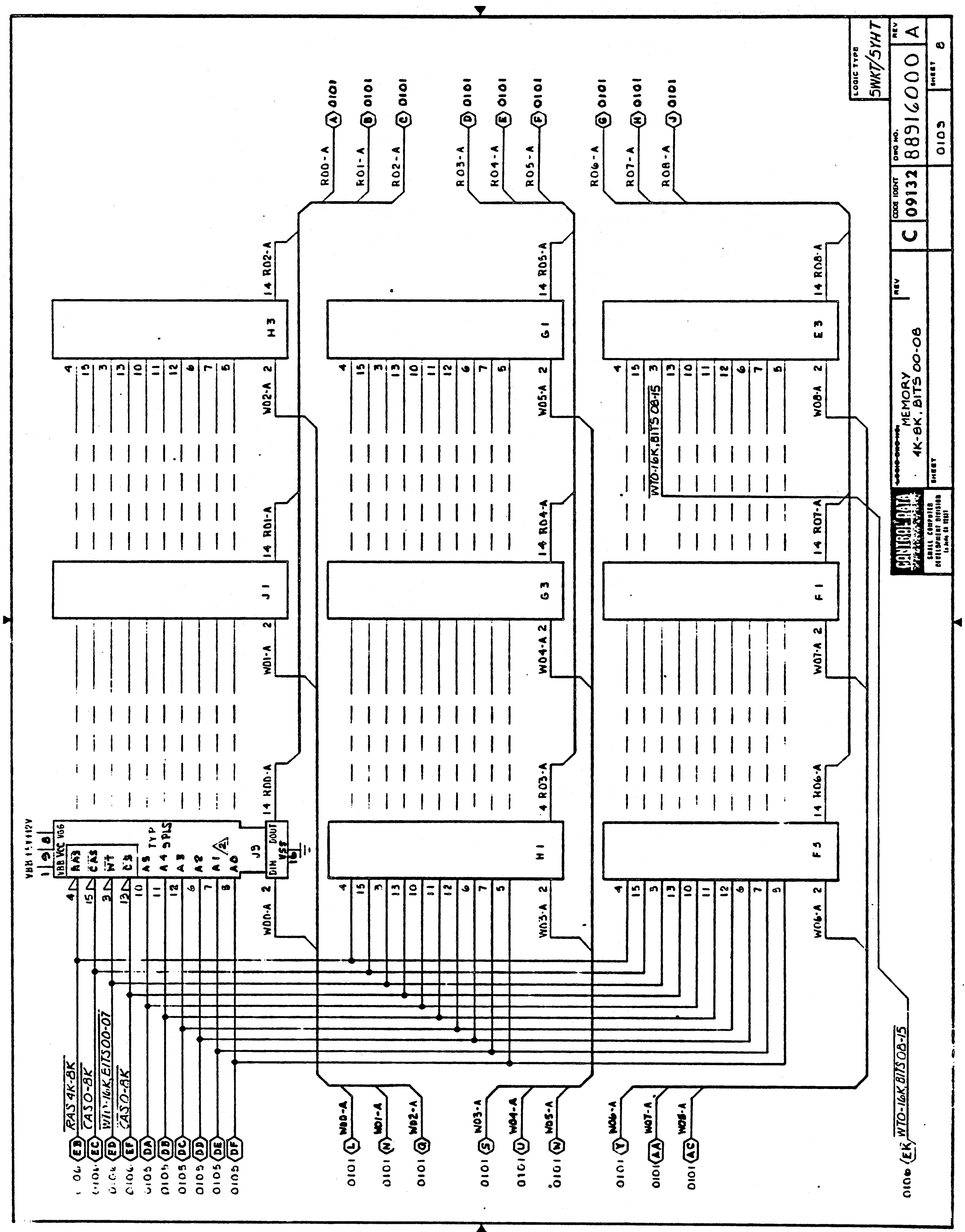

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 8 of 16)

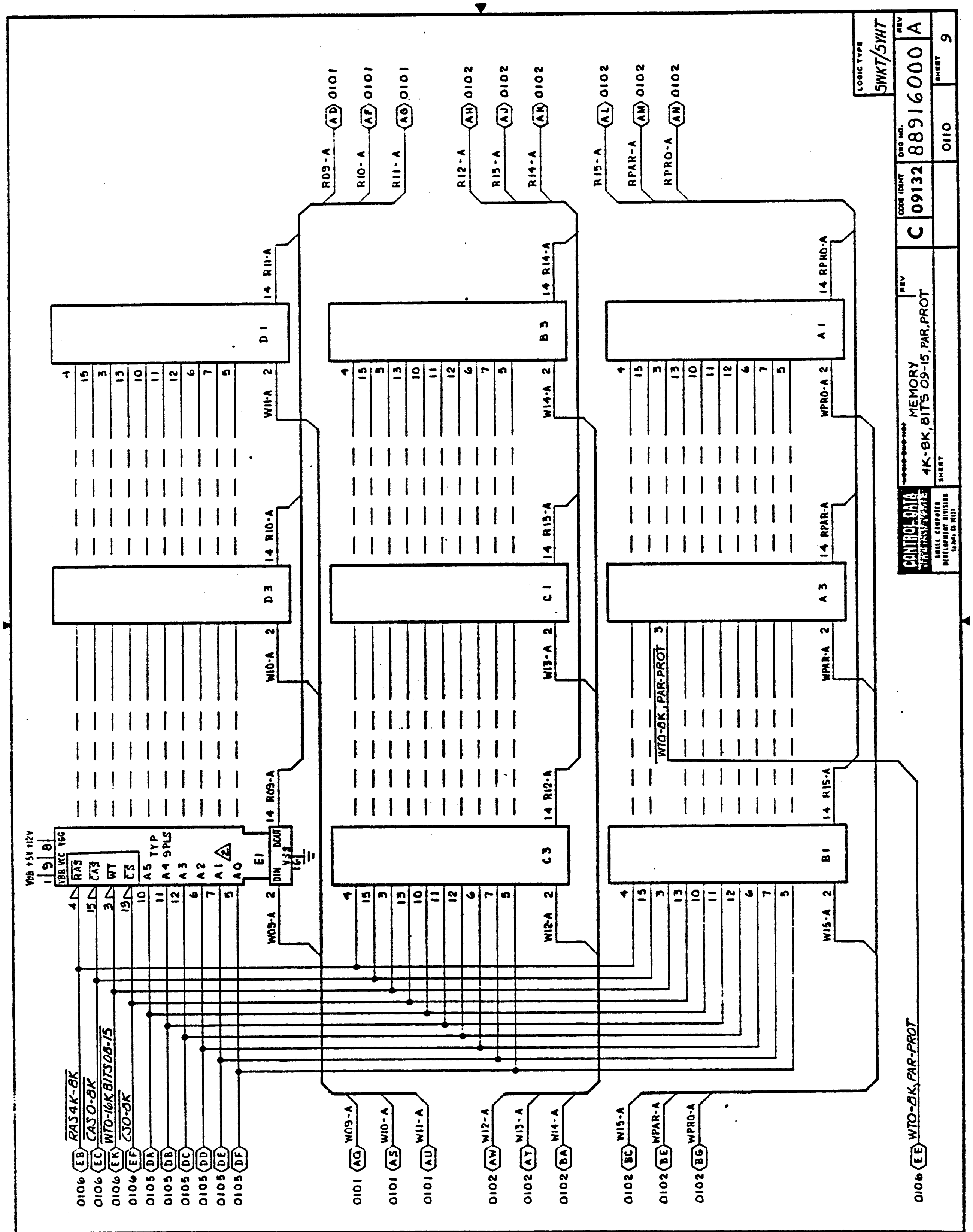

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 9 of 16)

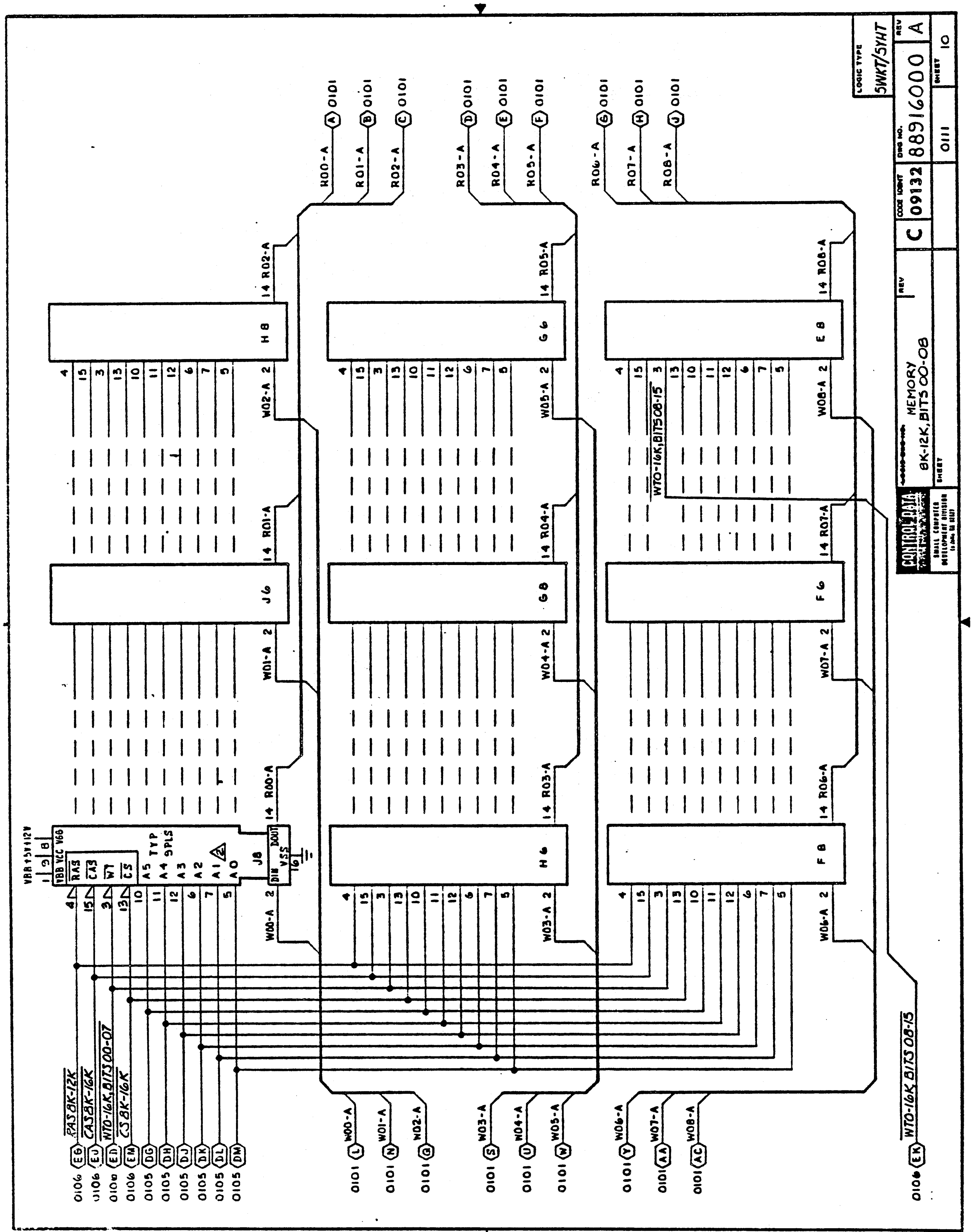

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 10 of 16)

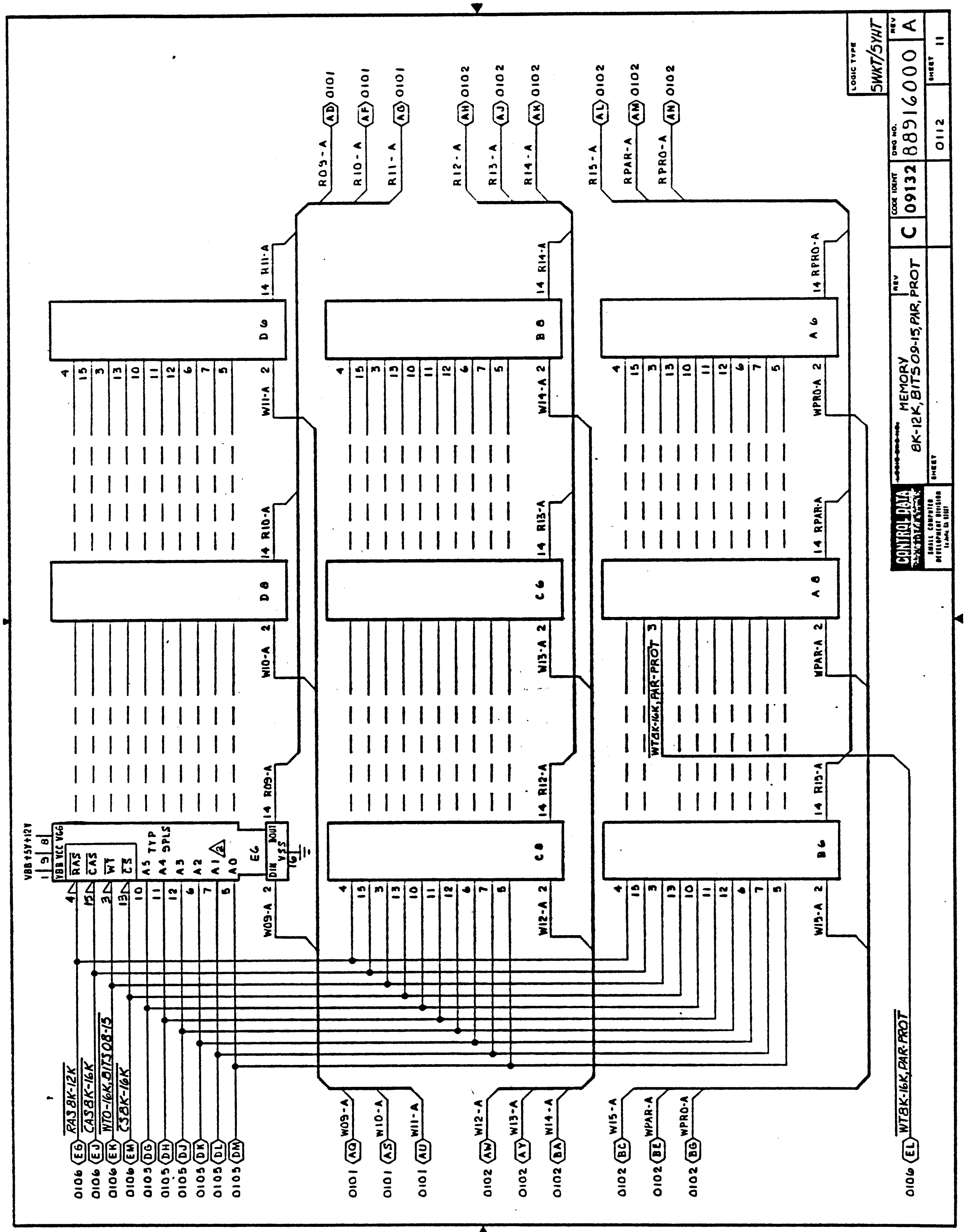

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 11 of 16)

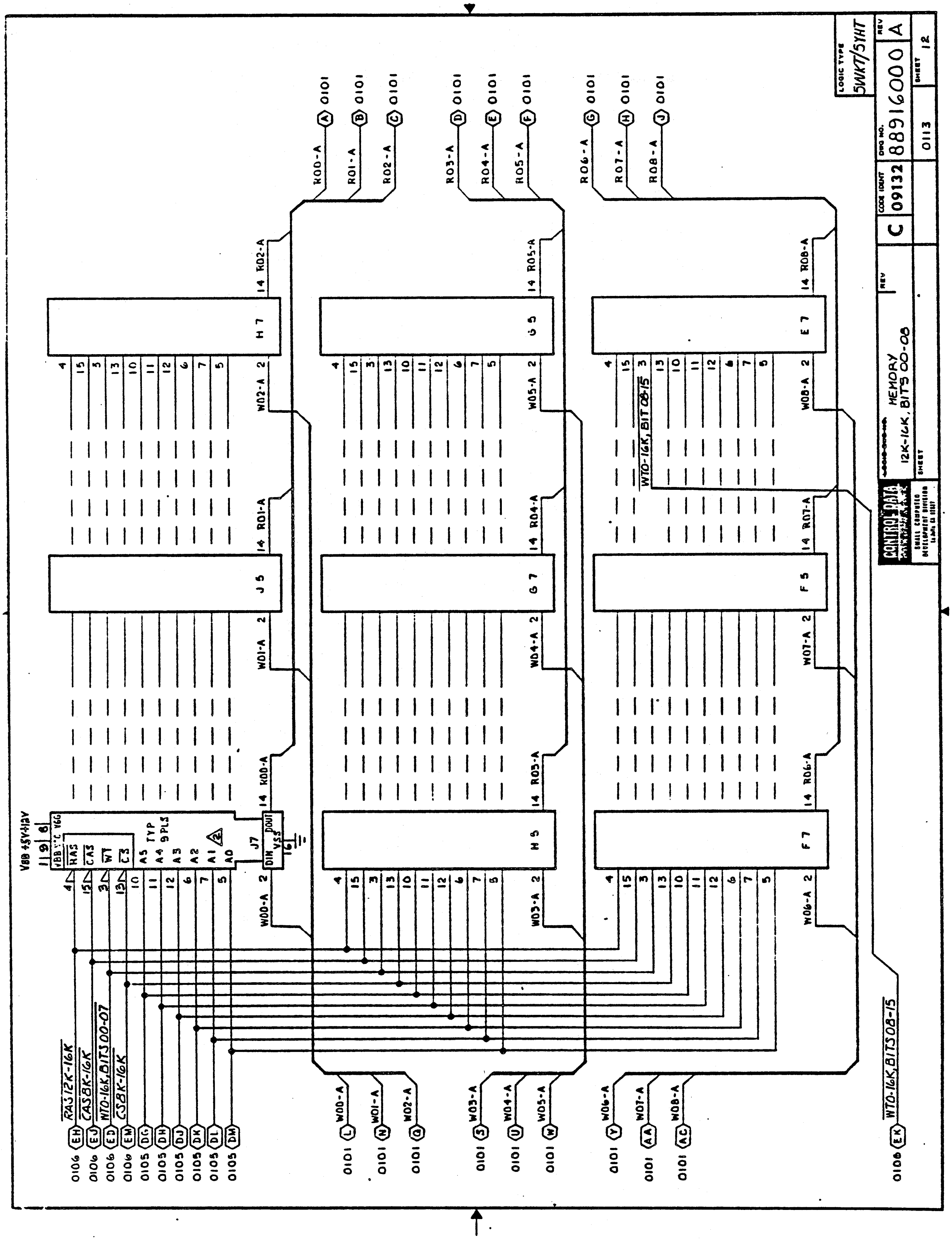

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 12 of 16)

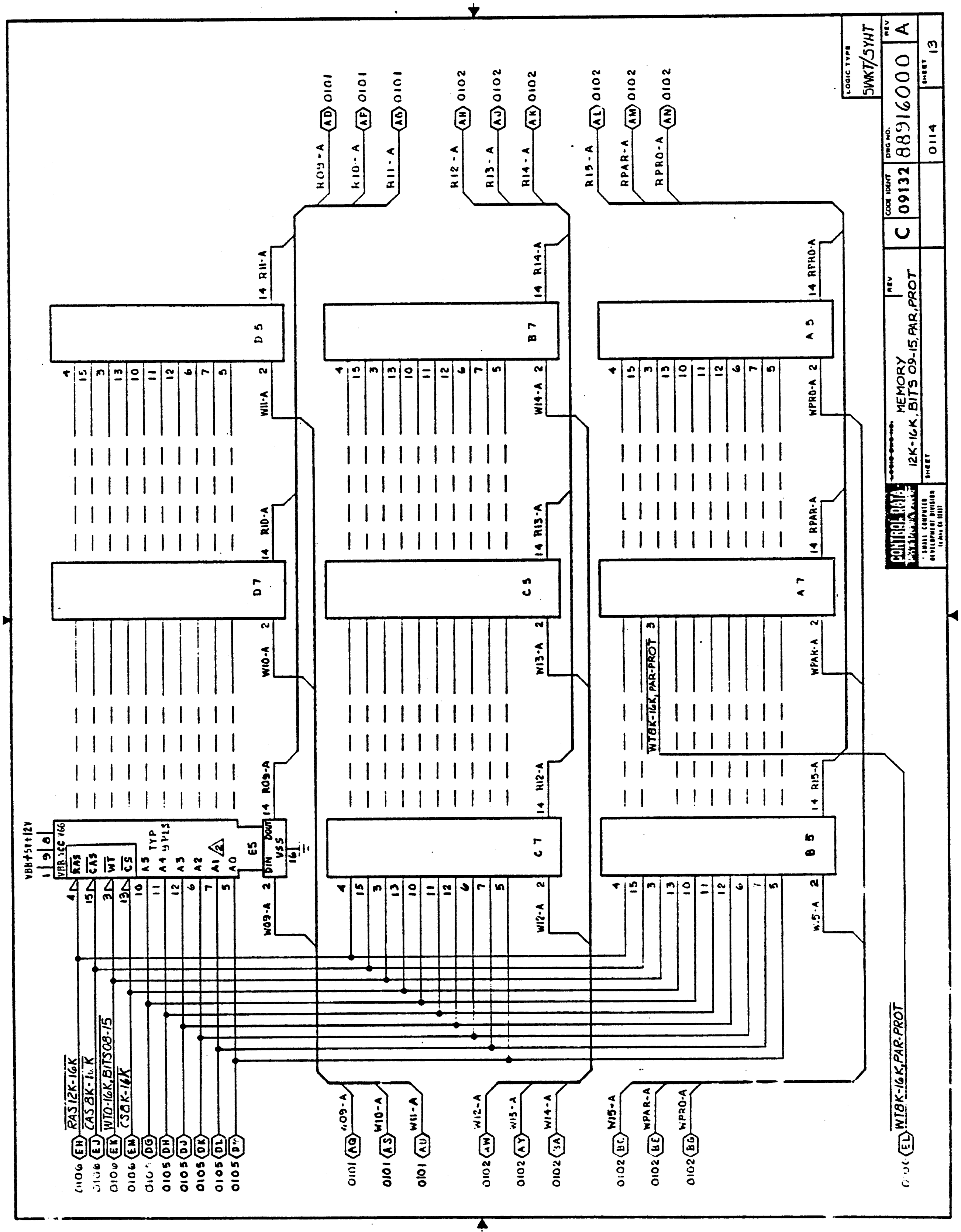

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 13 of 16)

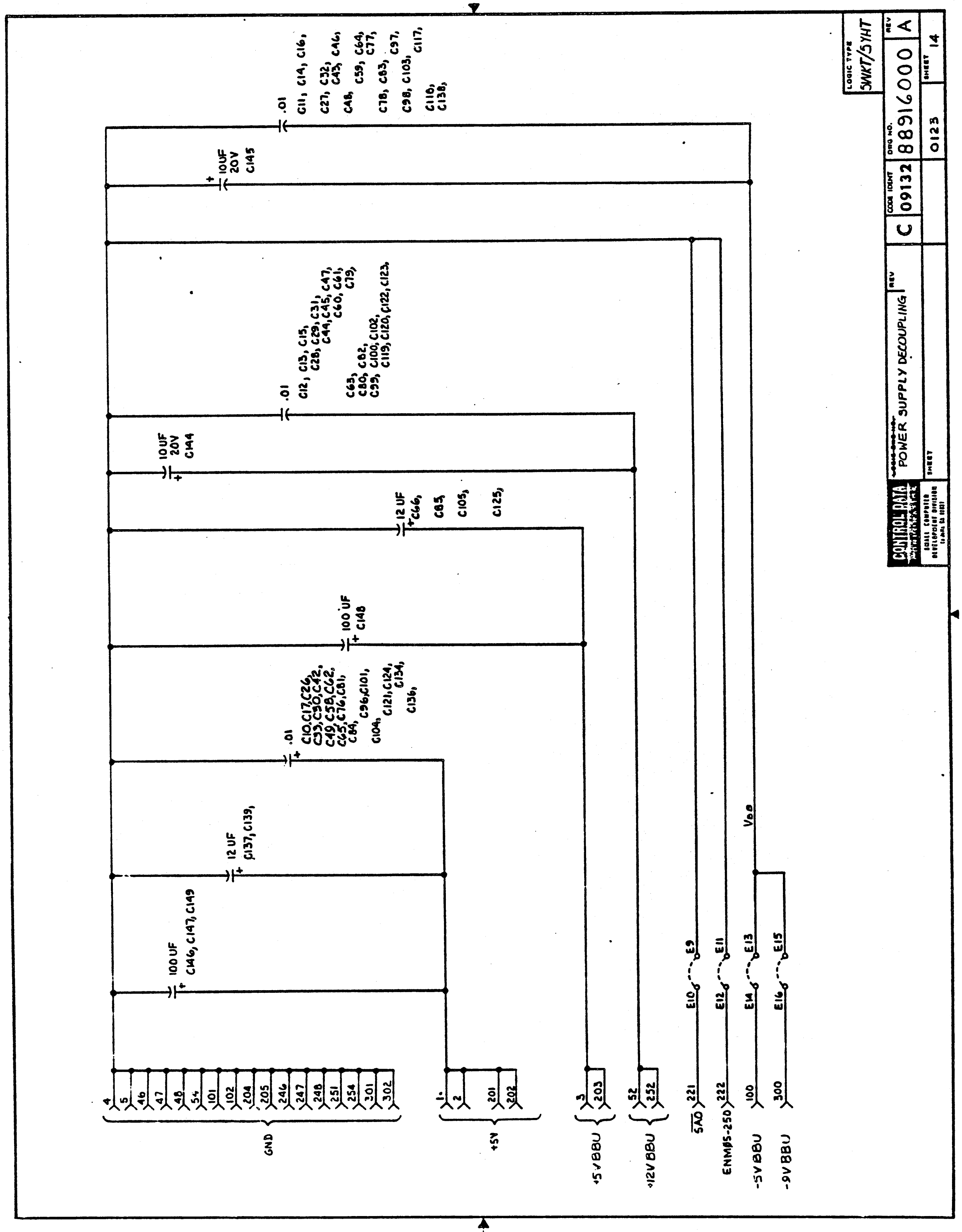

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 14 of 16)

PIN	CROSS REF. NO.	SIGNAL	X	Y	Z	AC
1	0123	+5V				
2	0123	+5V				
3	0123	+5V BBU				
4	0123	GND				
5	0123	GND				
6		BACKPLANE NOTES	X	Y	Z	AC
7		JUMPER TO 207 FOR	32K	32K	32K	32K/16K
8		JUMPER TO 208 FOR	32K	32K	16K	16K
9		JUMPER TO 209 FOR	32K	16K	16K	16K
10		JUMPER TO 210 FOR	16K	16K	16K	16K
11		SPARE				
12						
13						
14						
15						
16						
17						
18						
19						
20						
21						
22						
23						
24						
25		SPARE				
26		BACKPLANE NOTES	X	Y	Z	AC
27		JUMPER TO 227 FOR	32K	32K	32K	32K/16K
28		JUMPER TO 228 FOR	32K	32K	16K	16K
29		JUMPER TO 229 FOR	32K	16K	16K	16K
30		JUMPER TO 230 FOR	16K	16K	16K	16K
31		SPARE				
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45		SPARE				
46	0123	GND				
47	0123	GND				
48	0123	GND				
49		SPARE				
50		SPARE				
51		SPARE				

PIN	CROSS REF. NO.	SIGNAL
52	0123	+12VBBU
53		SPARE
54	0123	GND
55		SPARE
56		
57		
58		
59		
60		
61		
62		
63		
64		
65		
66		
67		
68		
69		
70		
71		
72		
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82		
83		
84		
85		
86		
87		
88		
89		
90		
91		
92		
93		
94		
95		
96		
97		
98		
99		SPARE
100	0123	-5V BBU
101	0123	GND
102	0123	GND

PIN	CROSS REF. NO.	SIGNAL
201	0123	+5V
202	0123	+5V
203	0123	+5V BBU
204	0123	GND
205	0123	GND
206	0102	EI6KNX-Y/
207	0102	EI6KNX-Y/
208	0101	EI6KNX-Y/
209	0101	EI6KNX-Y/
210	0101	EI6KNX-Y/
211		SPARE
212		
213		
214		
215		
216		
217		
218		
219		
220		SPARE
221	0123	SAO
222	0123	ENMOS-250
223		SPARE
224		
225		
226		SPARE
227	0106	RASI6KX-Y
228		SPARE
229		SPARE
230		SPARE
231	0106	WT-MØS
232	0106	WT-MØS
233	0106	WT-MØS
234		SPARE
235	0106	SLTBLK1
236		SPARE
237	0106	CS
238	0106	SLTBLK0
239	0106	CAS
240		SPARE
241	0106	SLTBLK2
242	0106	SLTBLK3
243		SPARE
244		
245		SPARE
246	0123	GND
247	0123	GND
248	0123	GND
249		SPARE
250		SPARE
251	0123	GND

PIN	CROSS REF. NO.	SIGNAL
252	0123	+12V BBU
253		SPARE
254	0123	GND
255	0101	MD00
256	0101	MD03
257	0105	MØSMA01
258	0105	MØSMA00
259	0105	MØSMA03
260	0105	MØSMA02
261		SPARE
262		SPARE
263	0101	MD07
264	0105	MØSMA05
265	0105	MØSMA04
266		SPARE
267		SPARE
268	0101	MD01
269	0101	MD02
270		SPARE
271	0101	MD06
272	0101	MD08
273	0101	MD11
274	0101	MD09
275		SPARE
276		SPARE
277	0101	MD05
278		SPARE
279		SPARE
280	0101	MD04
281	0101	MD10
282	0102	MPROT
283		SPARE
284	0102	MPAR
285		SPARE
286	0102	MD14
287	0102	MD15
288		SPARE
289		SPARE
290	0102	MD13
291		SPARE
292		SPARE
293	0102	MD12
294		SPARE
295		
296		
297		
298		
299		
300	0123	-9VBBU
301	0123	GND
302	0123	GND

CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION	I/O PIN REFERENCES	REV	C	CODE IDENT 09132	DWG NO. 88916000	REV A
	SHEET				0124	SHEET 15

LOGIC TYPE 5WKT/5YHT

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 15 of 16)

DWN	[illegible]	7-25-75	CONTROL DATA CORPORATION	TITLE LOGIC DIAGRAM-16K × 18 MOS MEMORY ARRAY (5WKT/5YHT)	PREFIX DR	DOCUMENT NO 88916000		REV A
CHKD	[illegible]	7-25-75	SMALL COMPUTER DEVELOPMENT DIVISION					
ENG	[illegible]	7-25 75		FIRST USED ON			SHEET 1 OF 1	
MFG			CODE IDENT 09132					
APPR	[illegible]	7-25 75						

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	18178	CL. B. PRE-RELEASED	LVP	7-25-75	[illegible]
02	14336	SEE ECO	BR	2-2-76	[illegible]
A	18312	CL. A. RELEASED	PVB	2-19-76	[illegible]

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

NOTES:

DETACHED LISTS

AA3180 REV. 8/71

PRINTED IN U.S.A.

Figure 5-15. 16K MOS Memory Array (PWA 96743702) Logic Diagram (Sheet 16 of 16)

REVISION RECORD

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APP
01	18197	CL B. PRE-RELEASED	I.P.	1-19-75	[illegible]	[illegible]
02	14336	SEE ECO	BR	2-27-76	[illegible]	[illegible]
A	18312	CL A. [illegible]	PVB	2-19-76	[illegible]	[illegible]

3. JUMPER CONFIGURATION

JUMPER	5WGT	5YJT
E9 E10	IN	IN
E11 E12	IN	OUT
E13 E14	OUT	IN
E15 E16	IN	OUT

2. CDC PART NO 15152600 OR 15152700, NO ELEMENT IDENT. AVAILABLE

1. 8T97 IS SIMILAR TO 939

NOTES: UNLESS OTHERWISE SPECIFIED

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

REFERENCE DRAWINGS

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES			
CAP.			

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON		
DR	K. WERTZ	6-16-75
CHK	[signature]	8-7-75
ENGR	[signature]	8-7-75
MFG		
APPD	[signature]	8-18-75

TITLE
LOGIC DIAGRAM
32K x 18
MOS MEMORY ARRAY CARD
5WGT/5YJT

CODE IDENT NO.	DRAWING NUMBER	
C 09132	88915900	A

SHEET 1 OF 24

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 1 of 24)

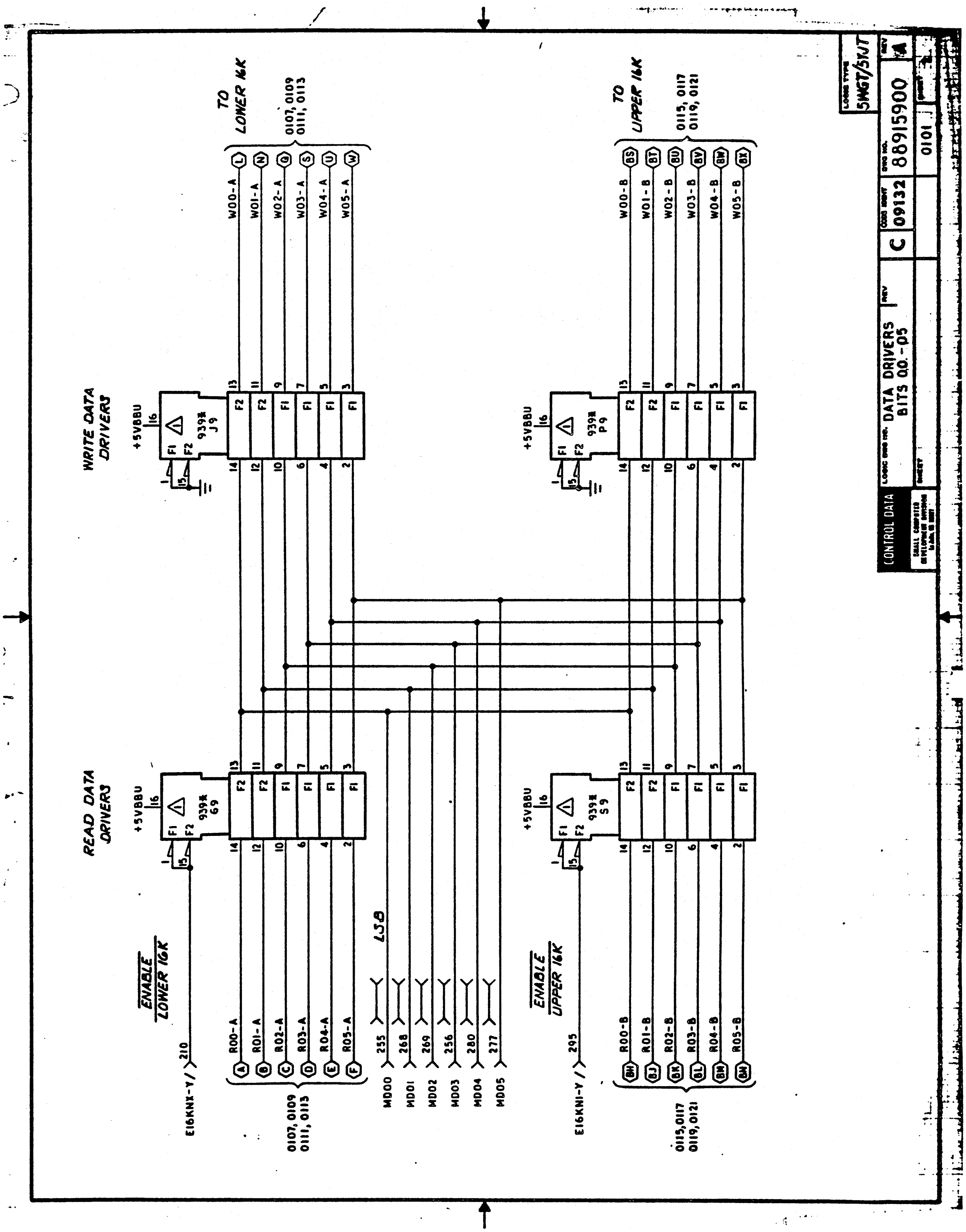

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 2 of 24)

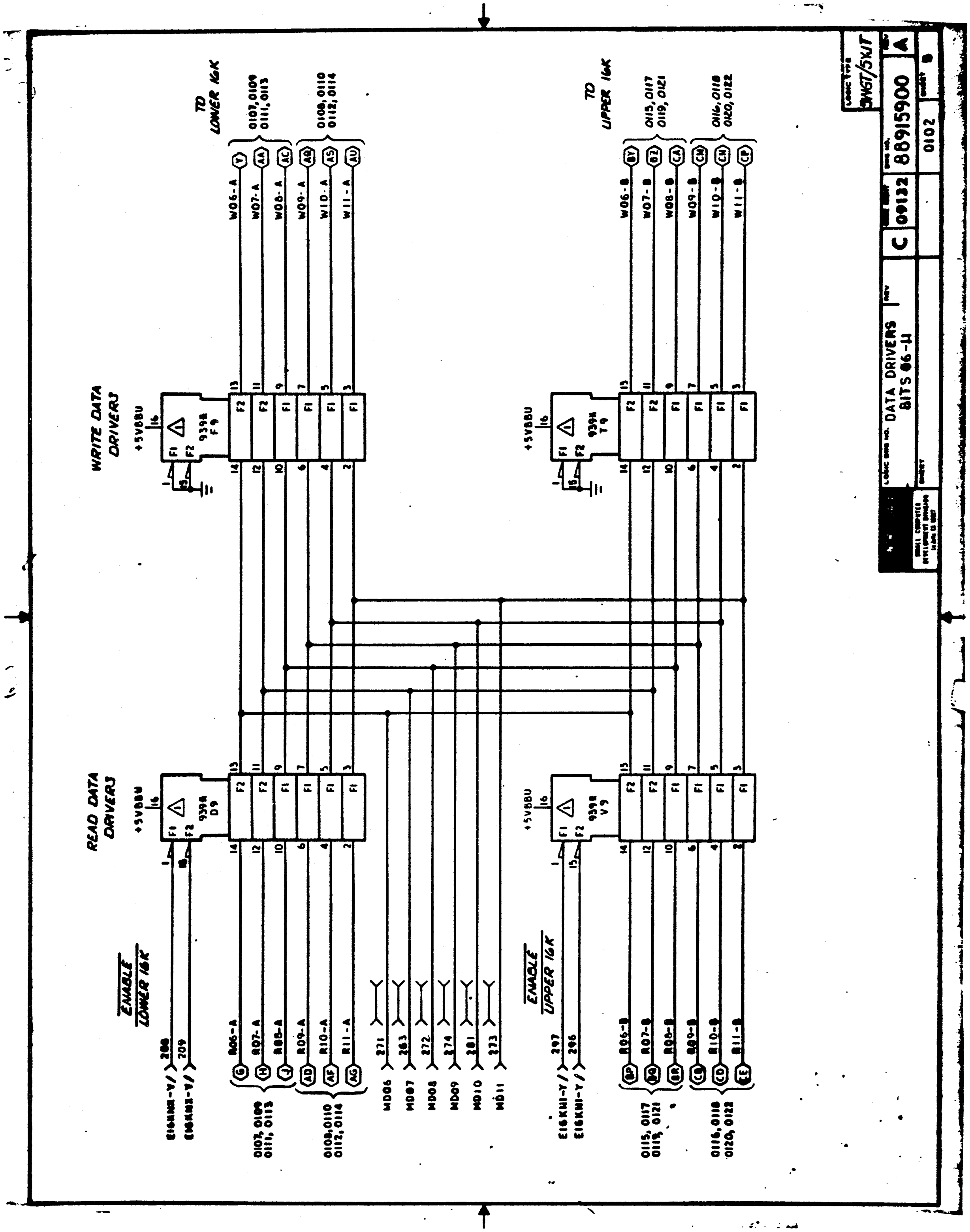

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 3 of 24)

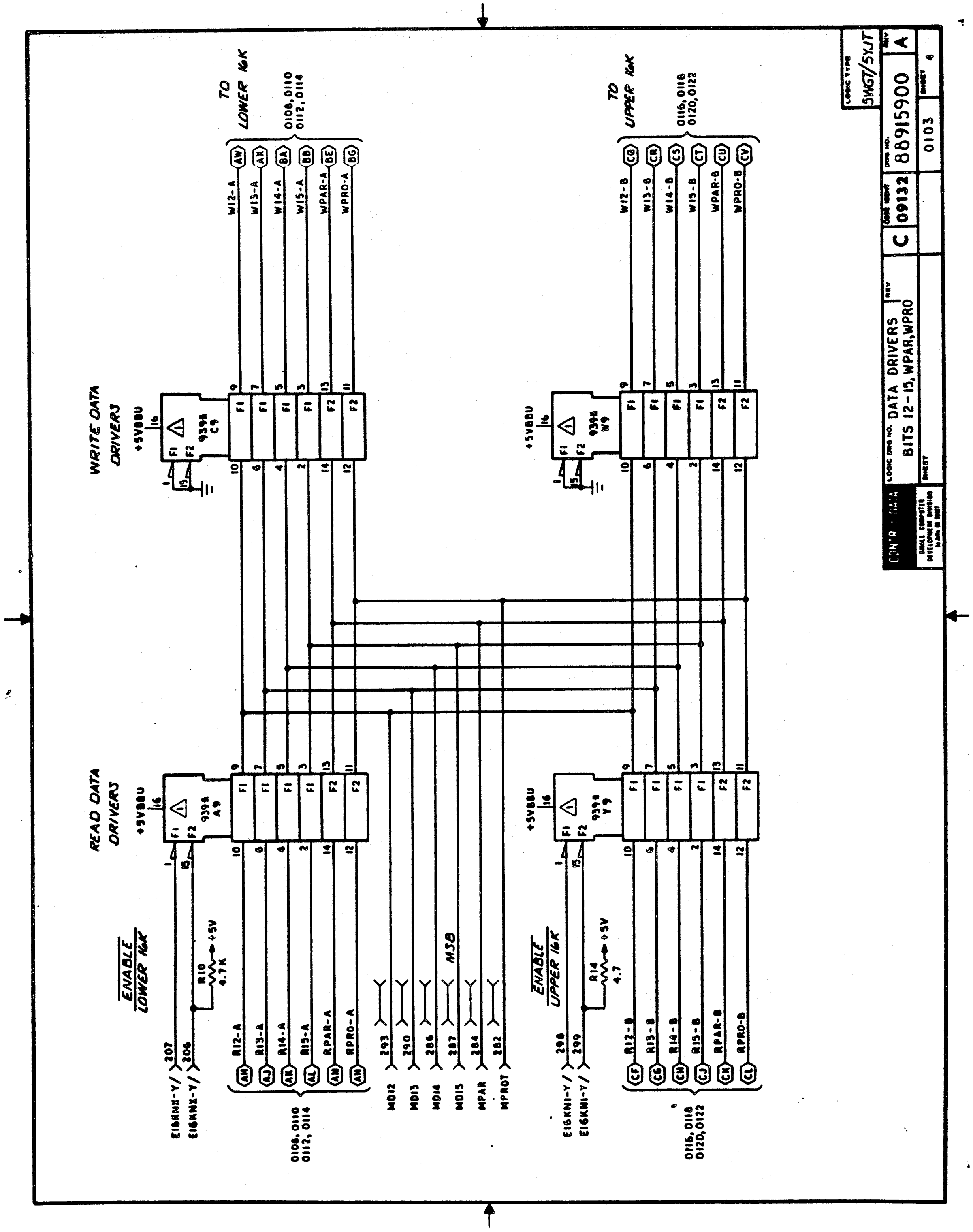

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 4 of 24)

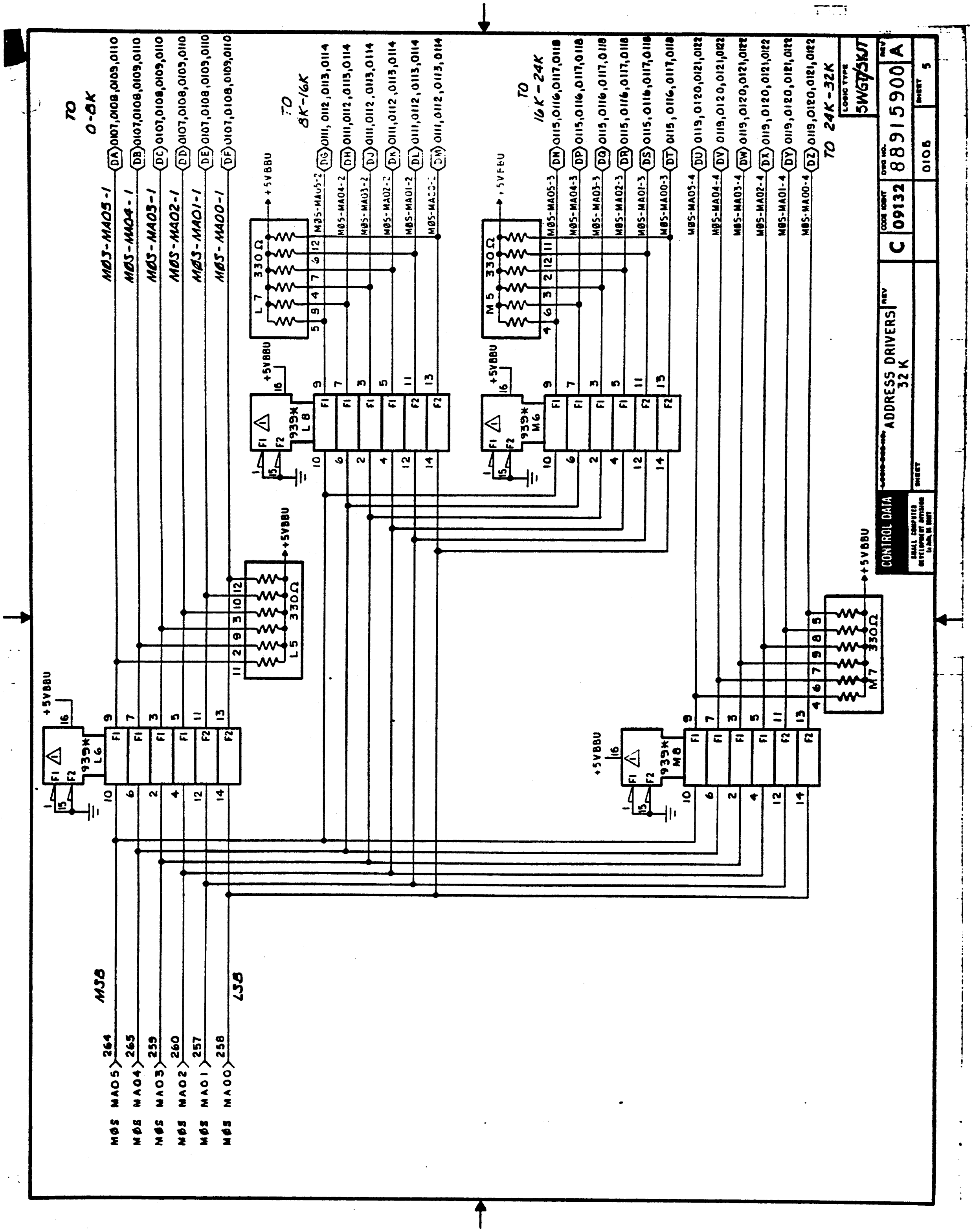

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 5 of 24)

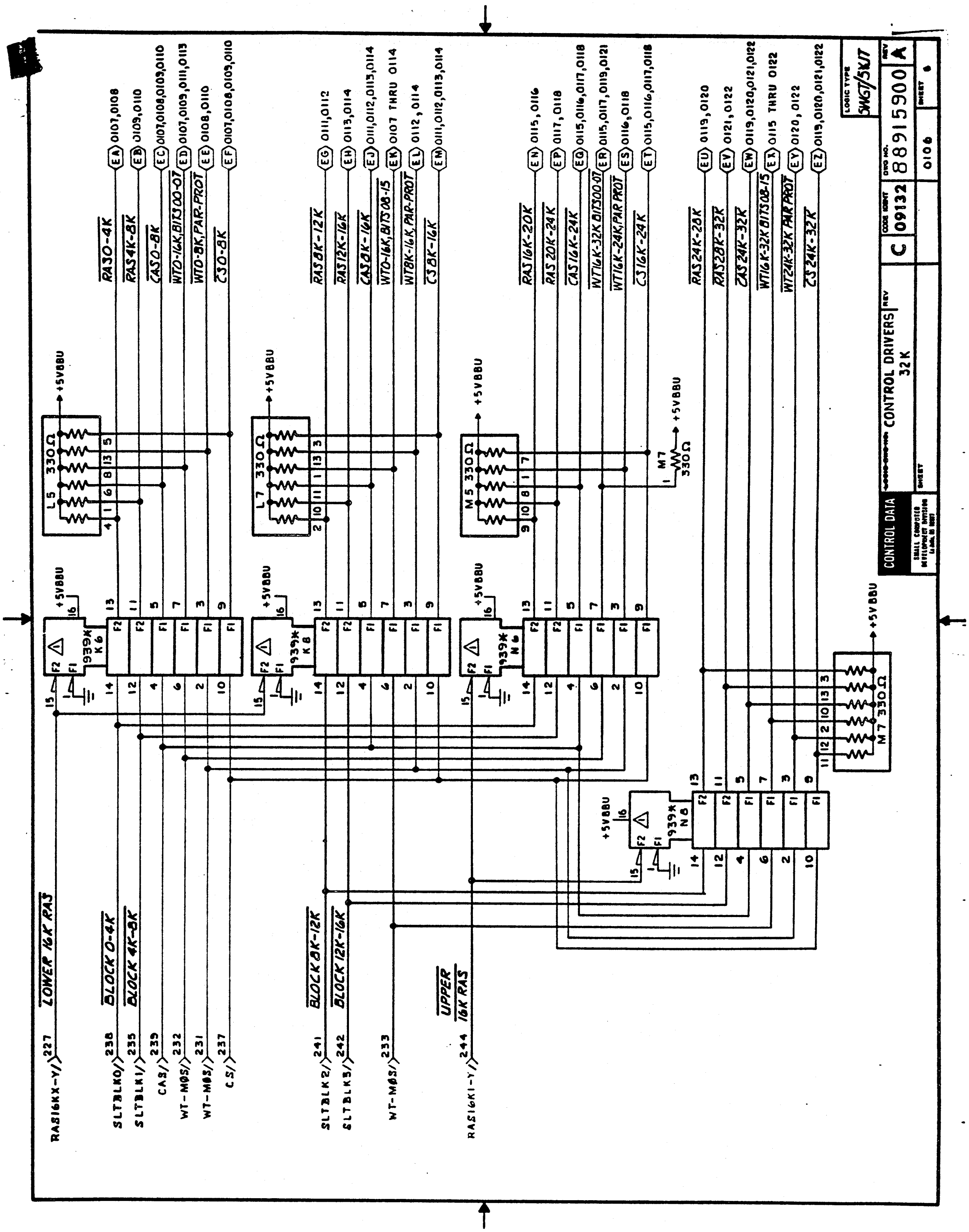

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 6 of 24)

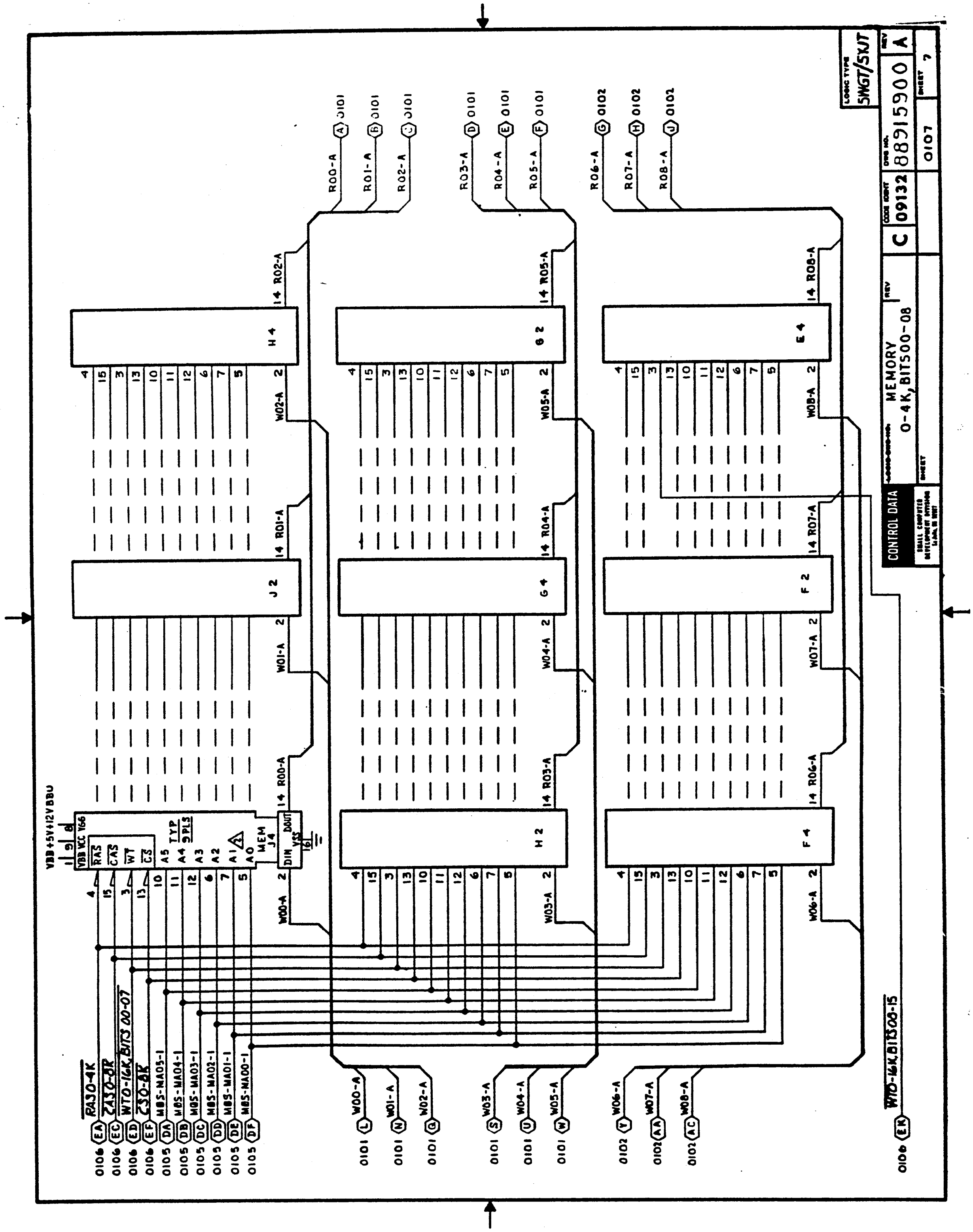

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 7 of 24)

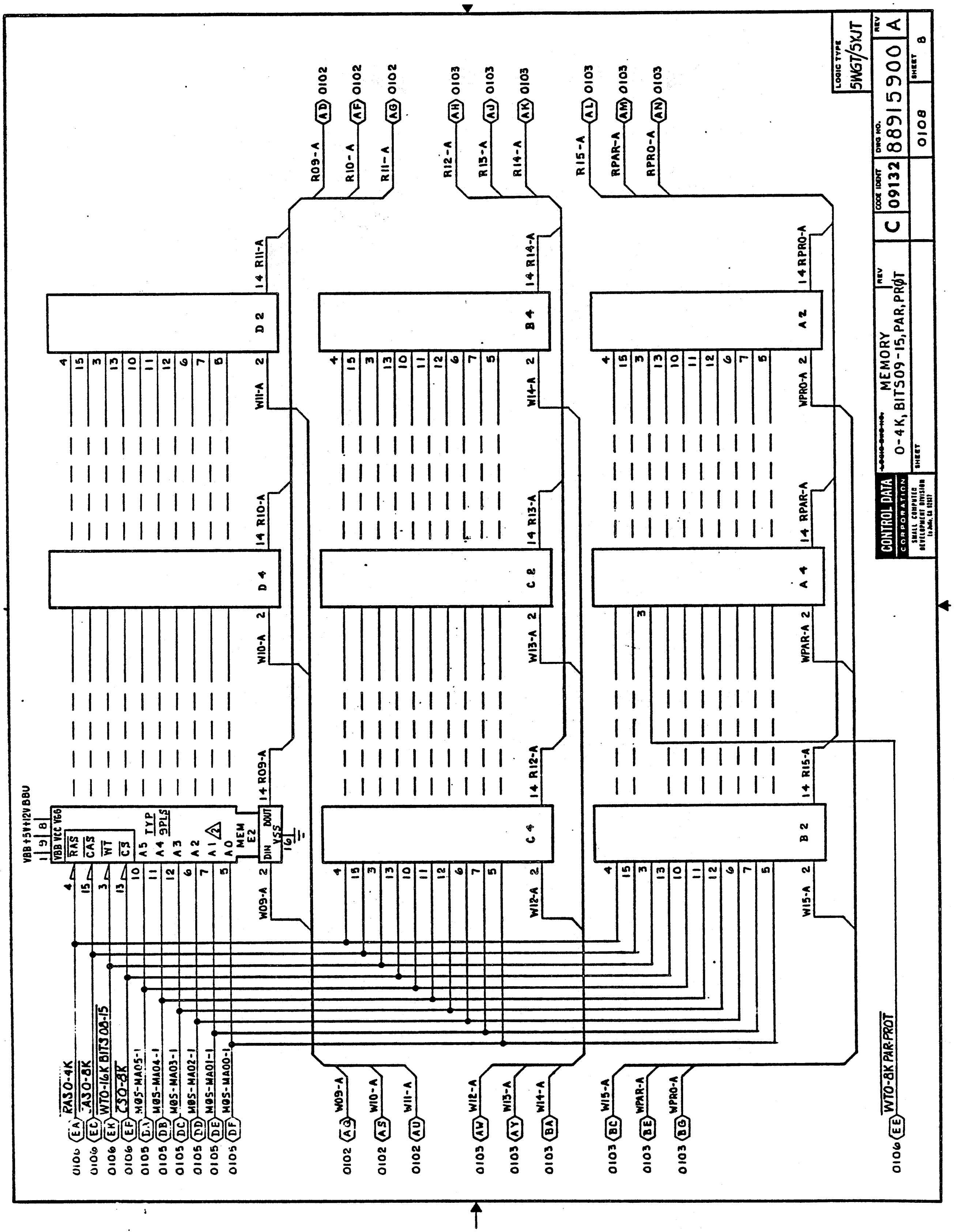

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 8 of 24)

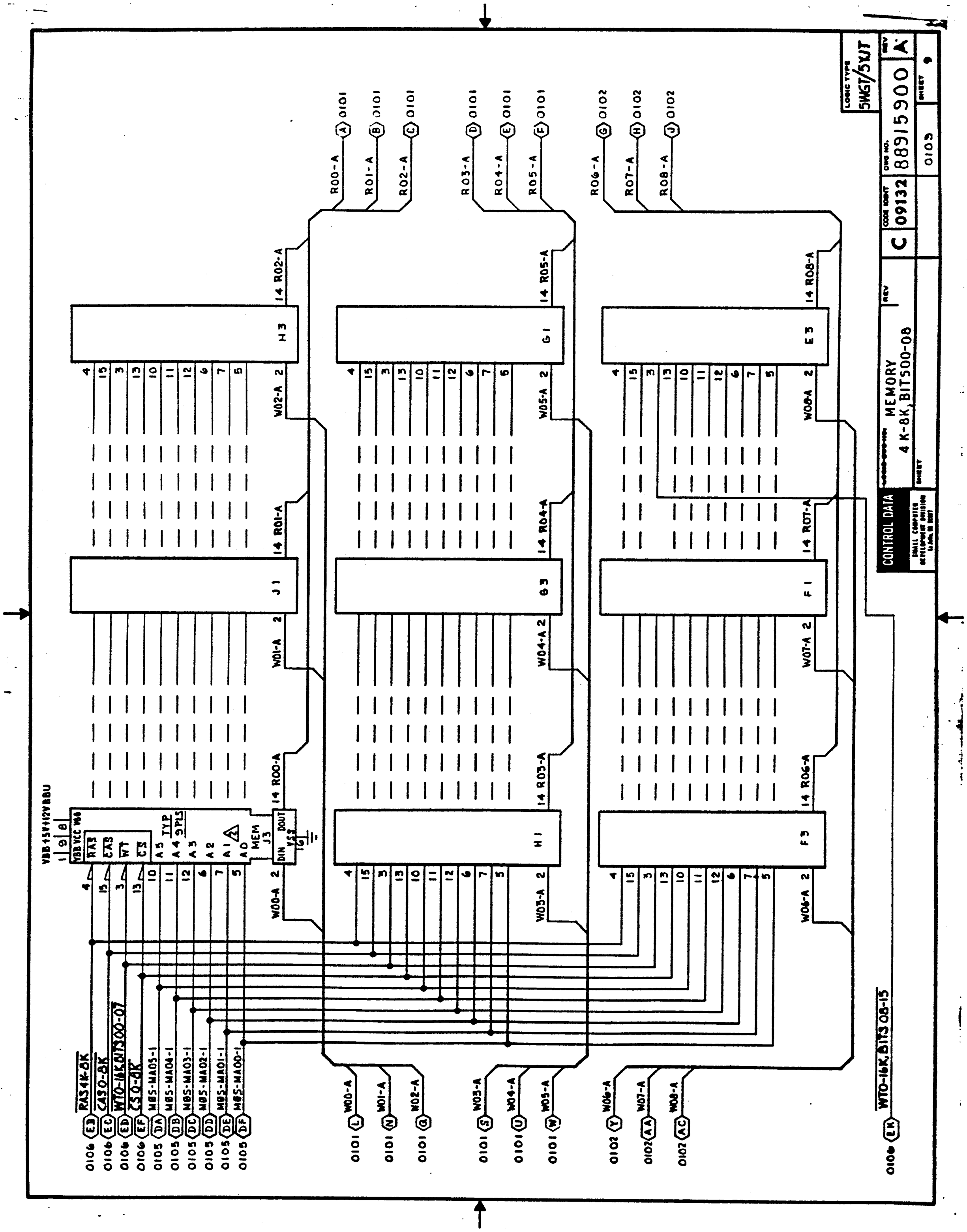

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 9 of 24)

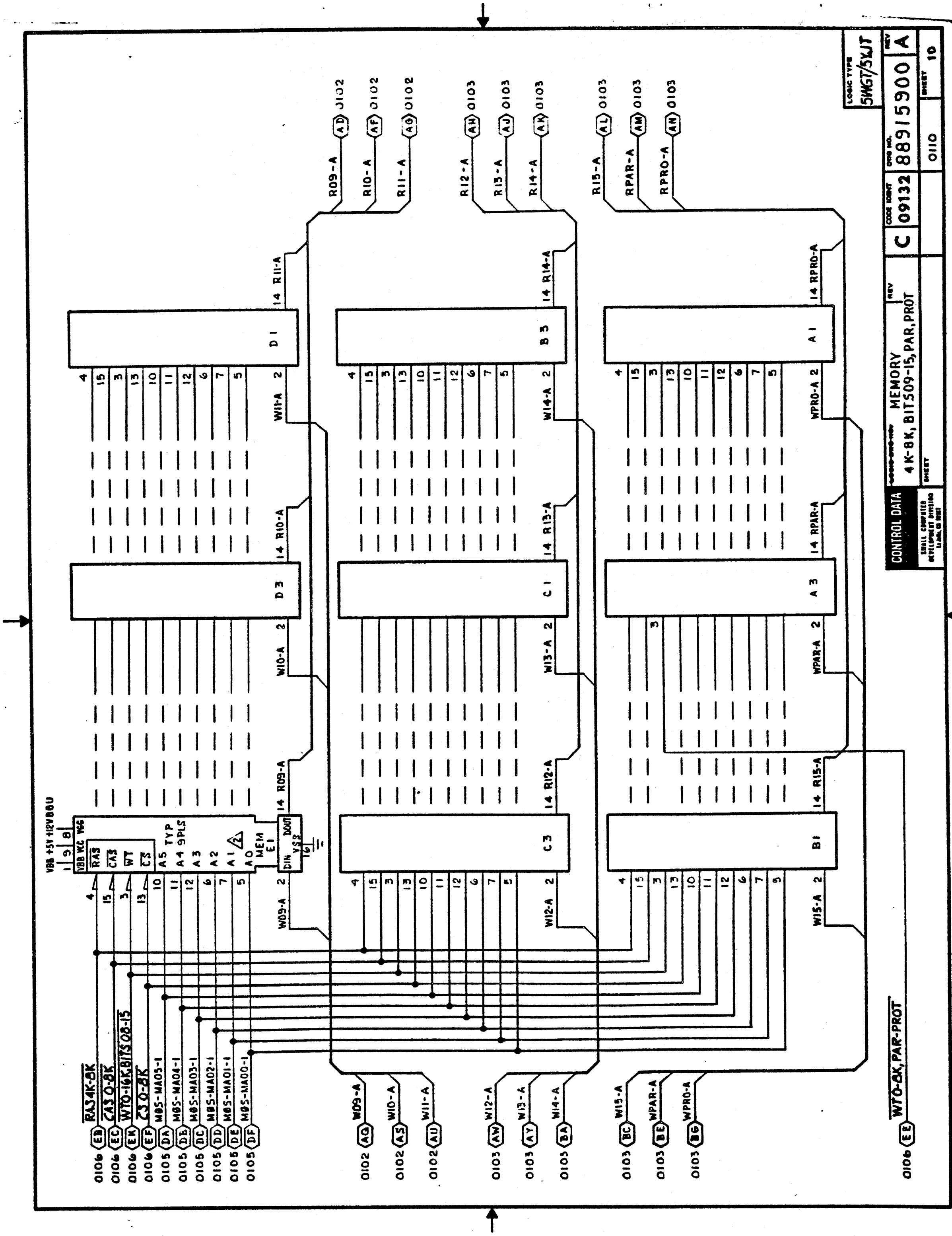

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 10 of 24)

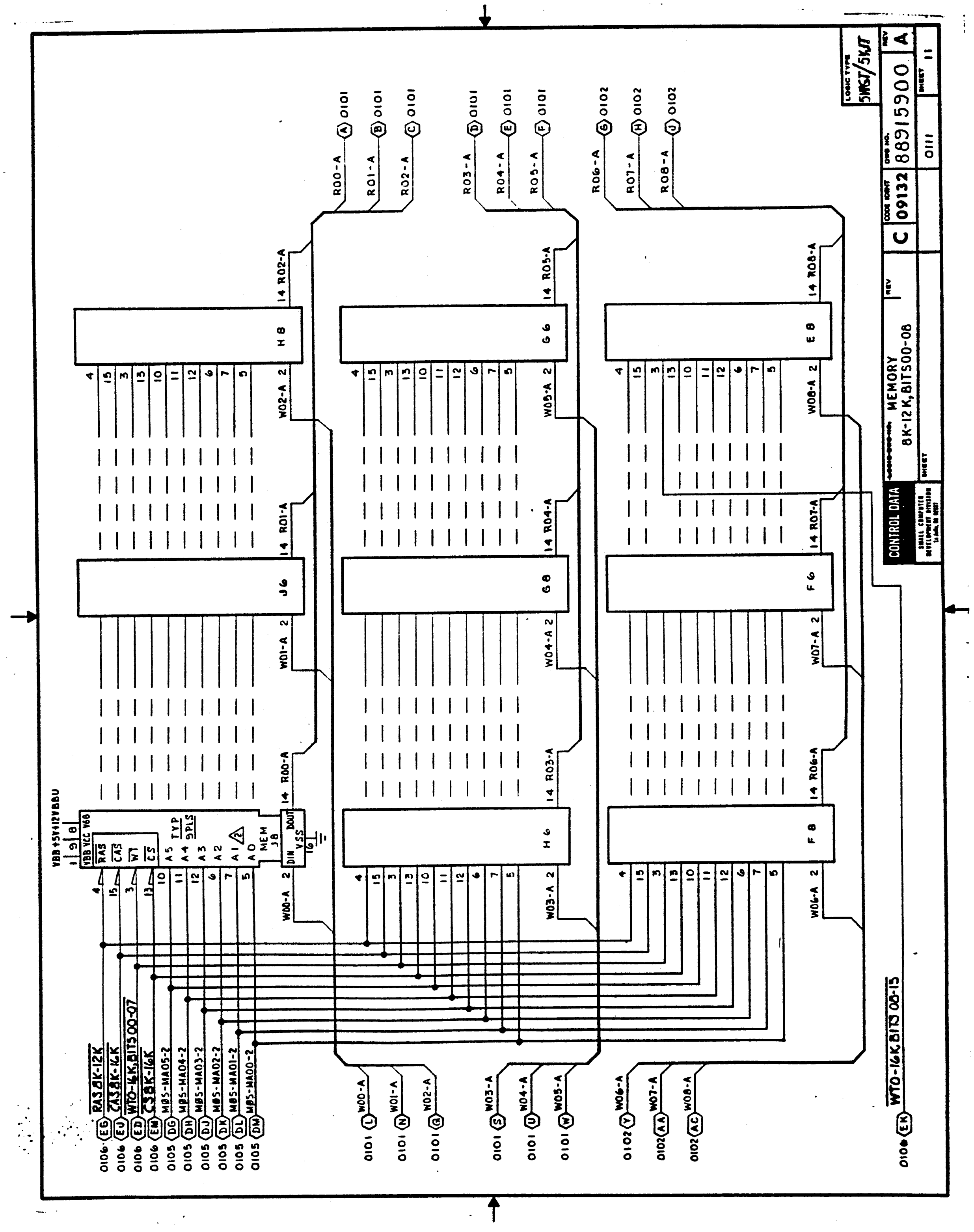

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 11 of 24)

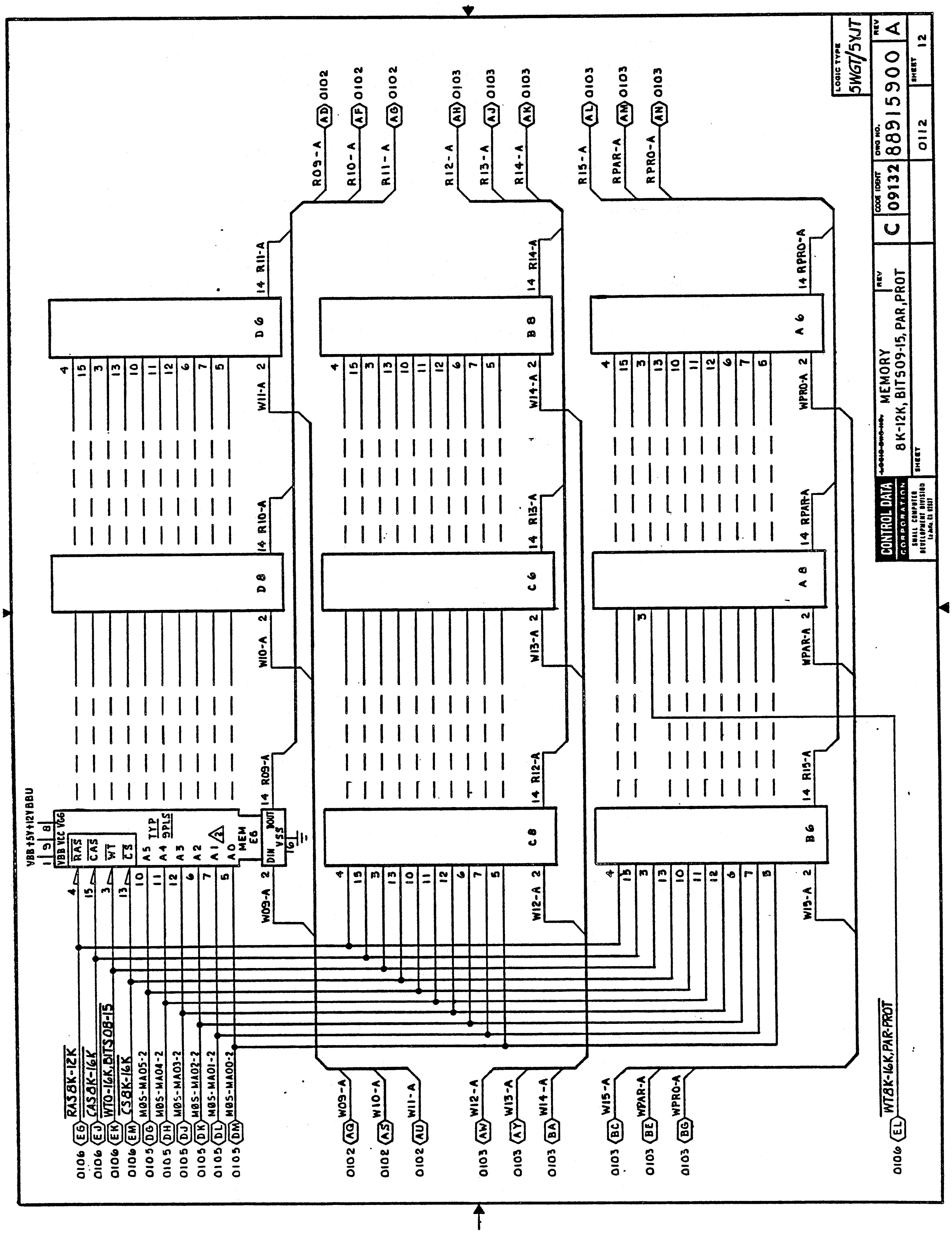

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 12 of 24)

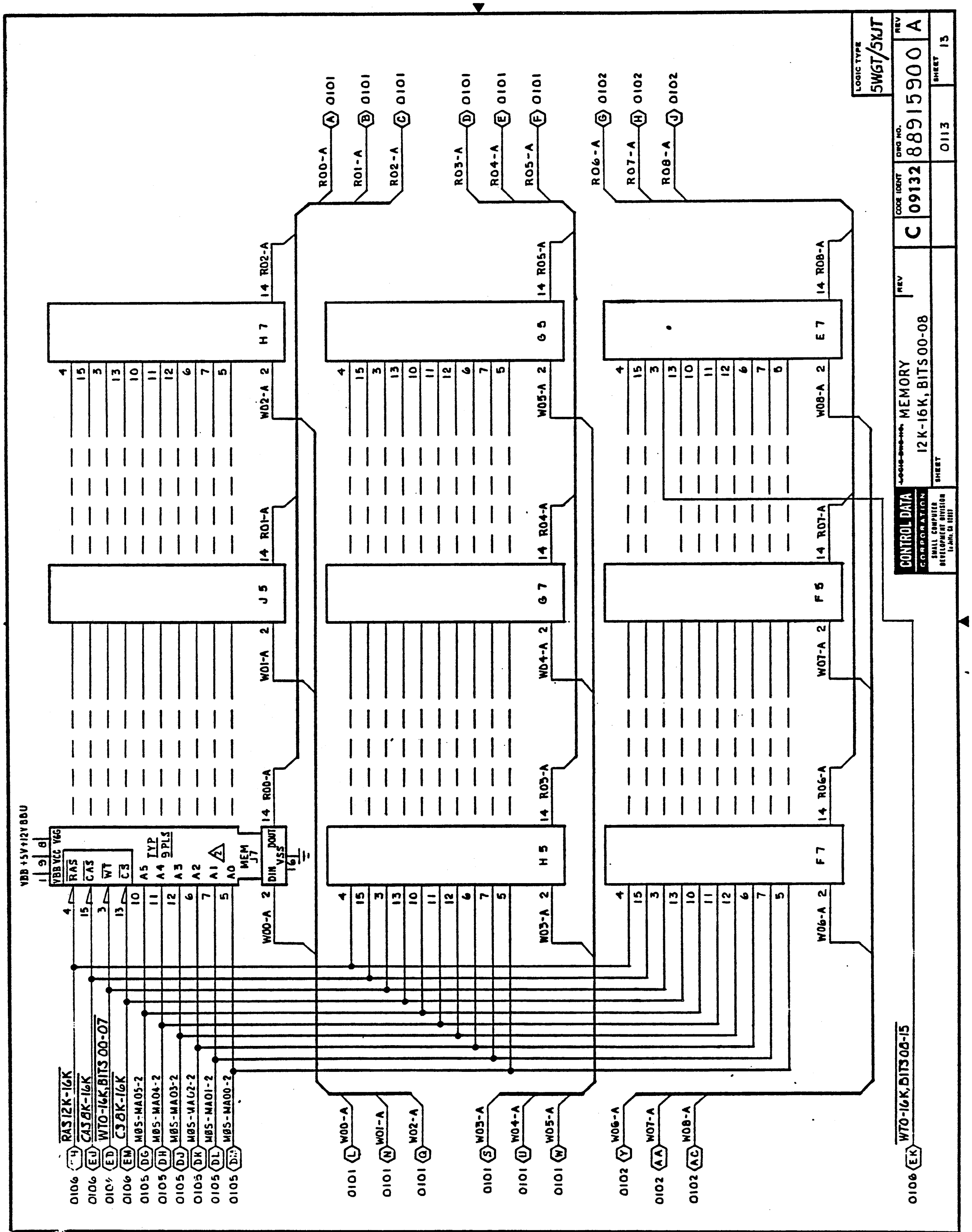

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 13 of 24)

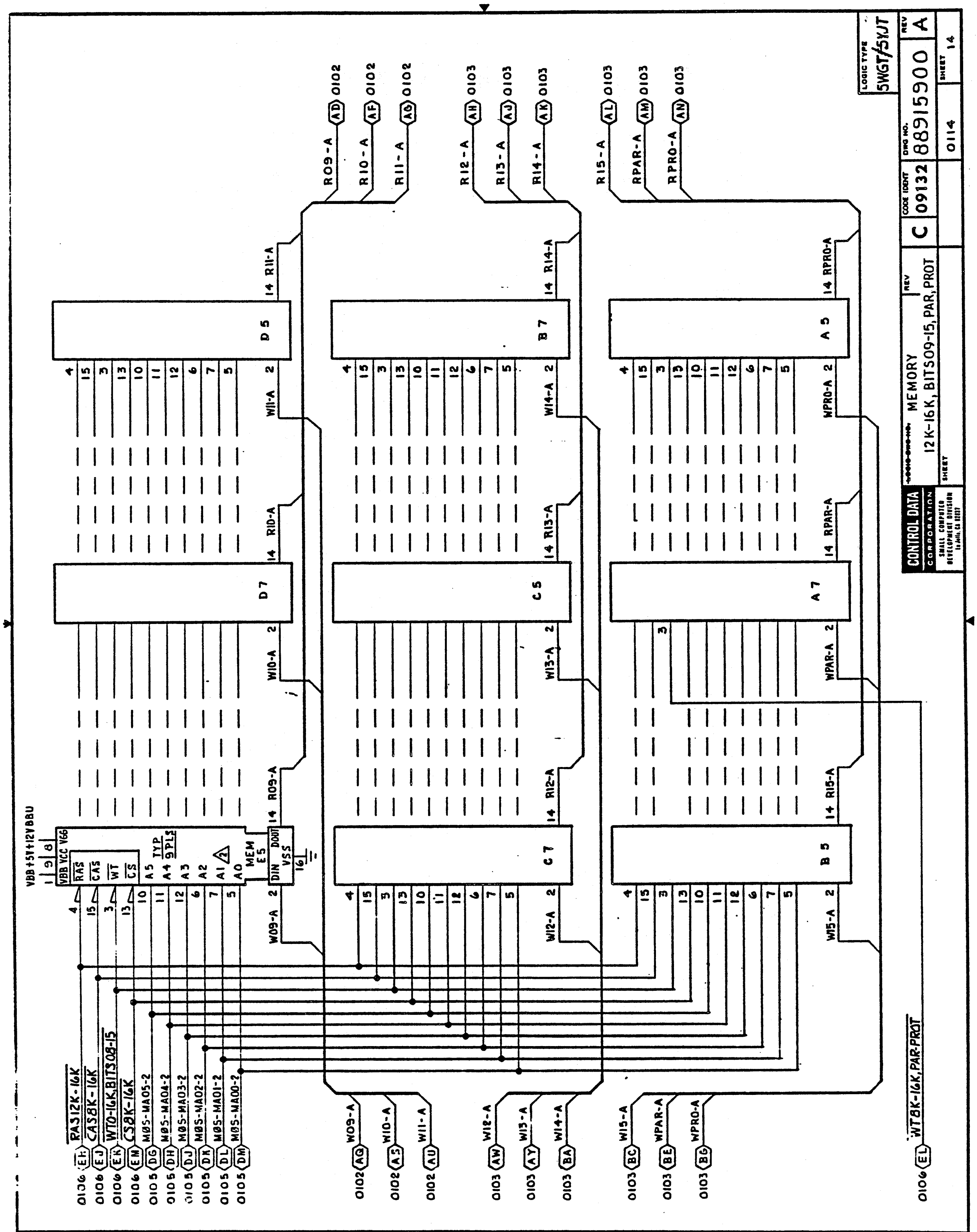

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 14 of 24)

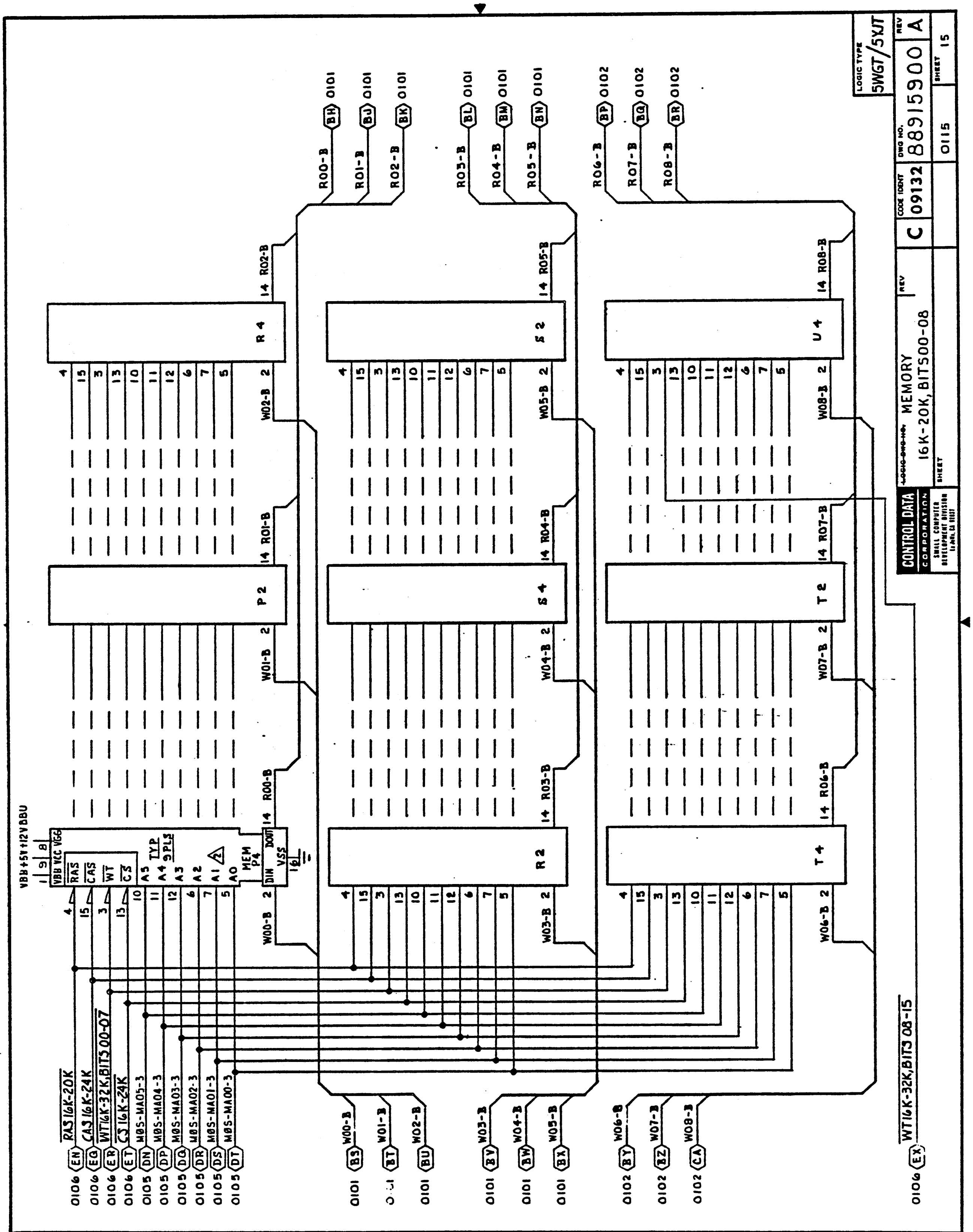

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 15 of 24)

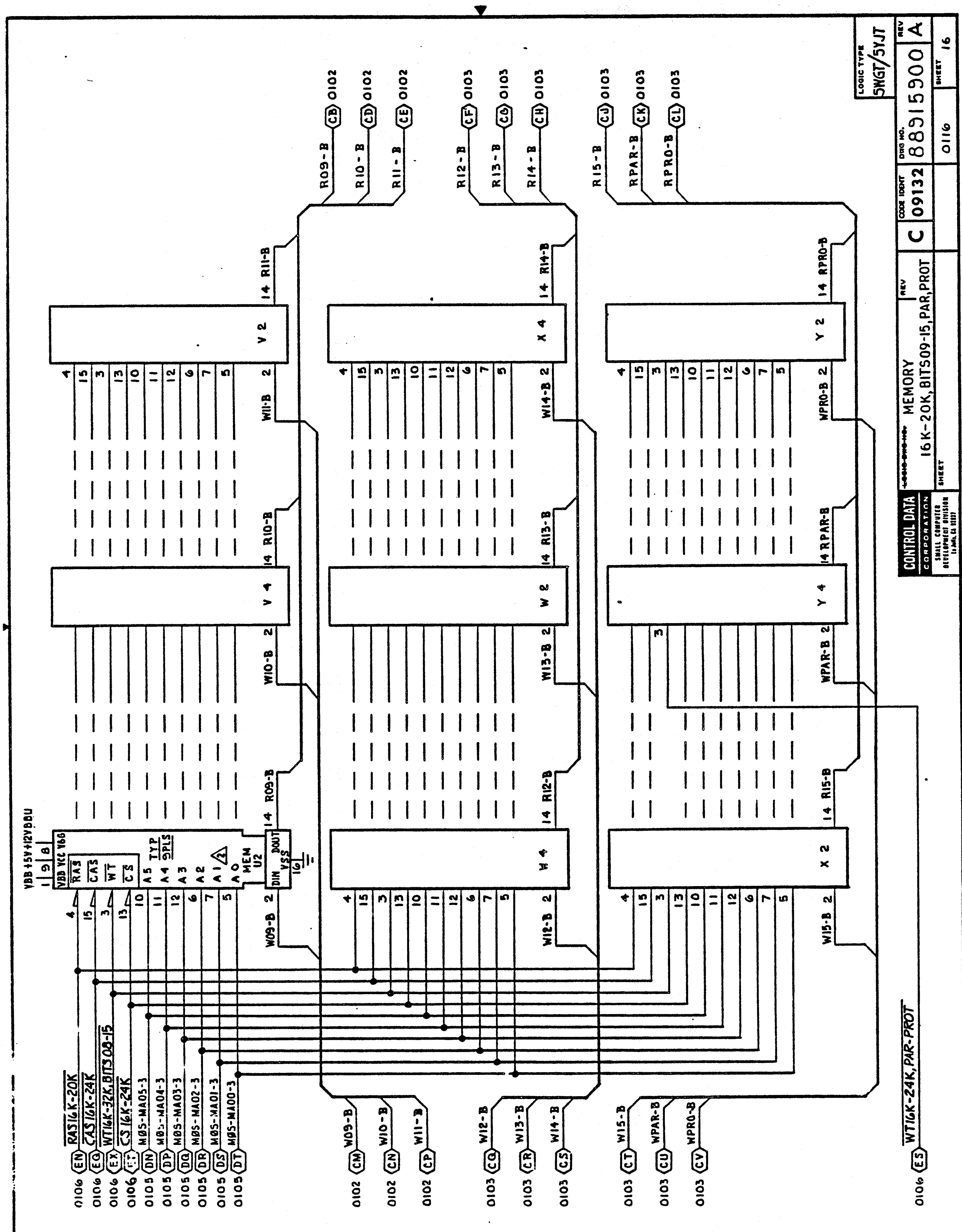

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 16 of 24)

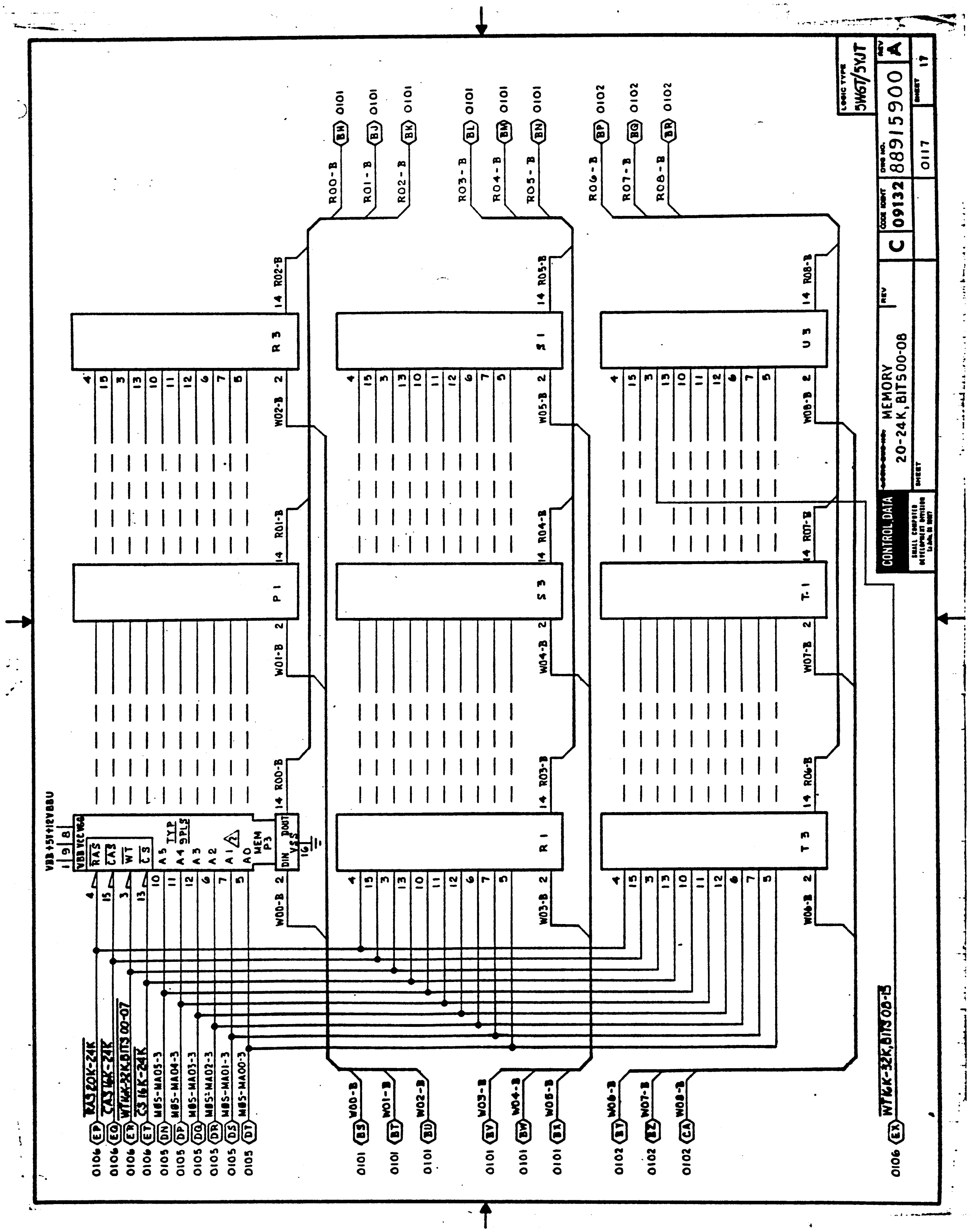

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 17 of 24)

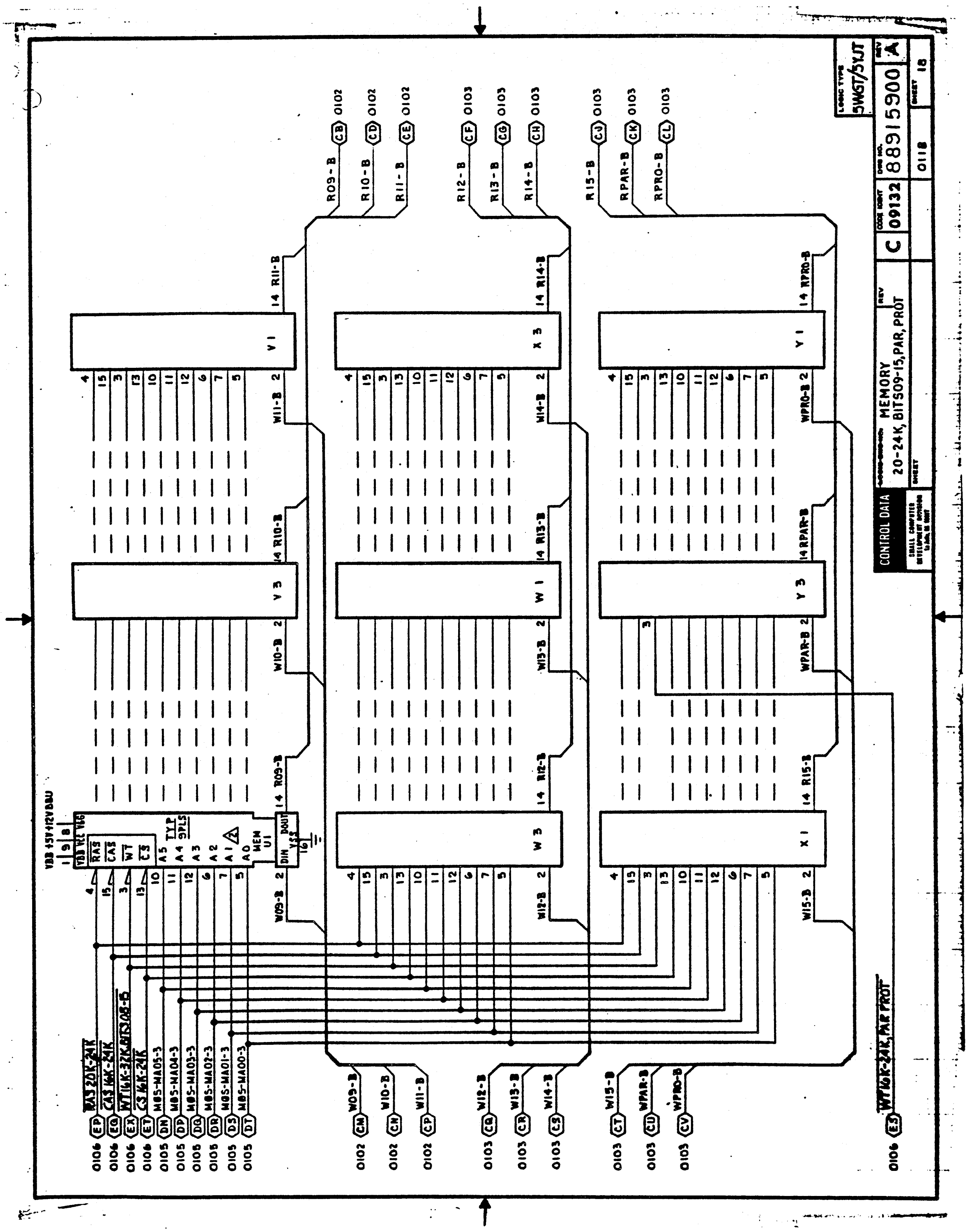

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 18 of 24)

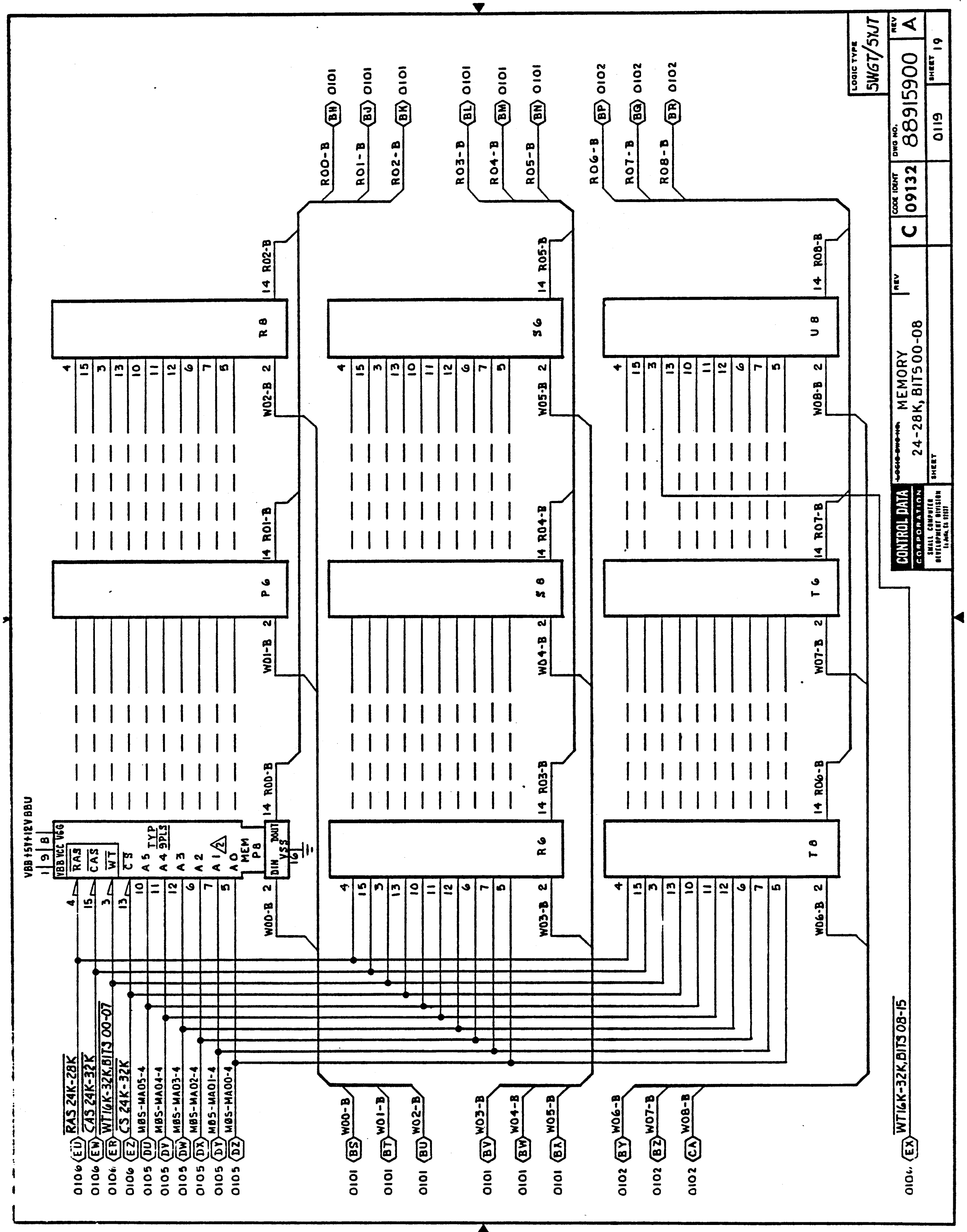

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 19 of 24)

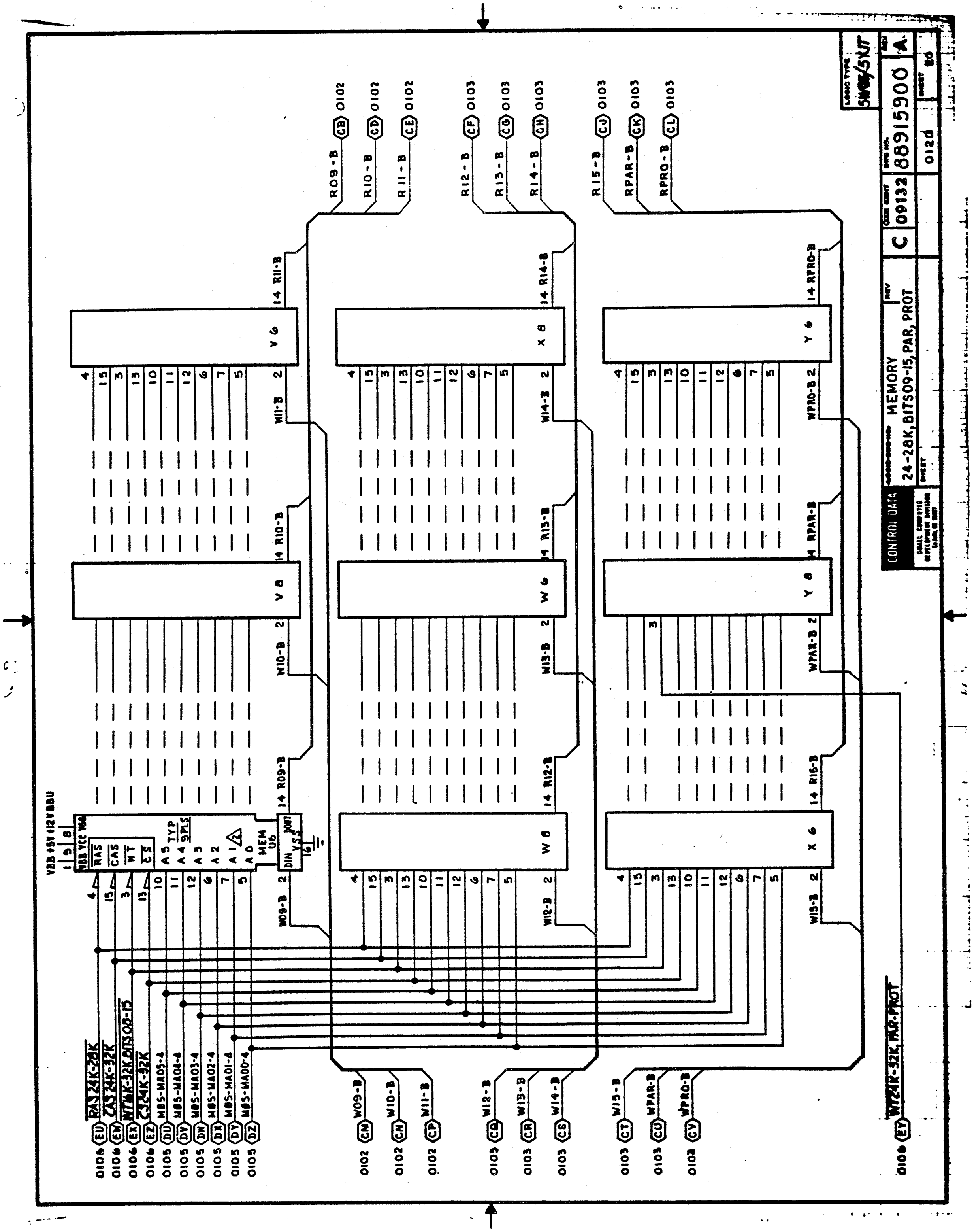

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 20 of 24)

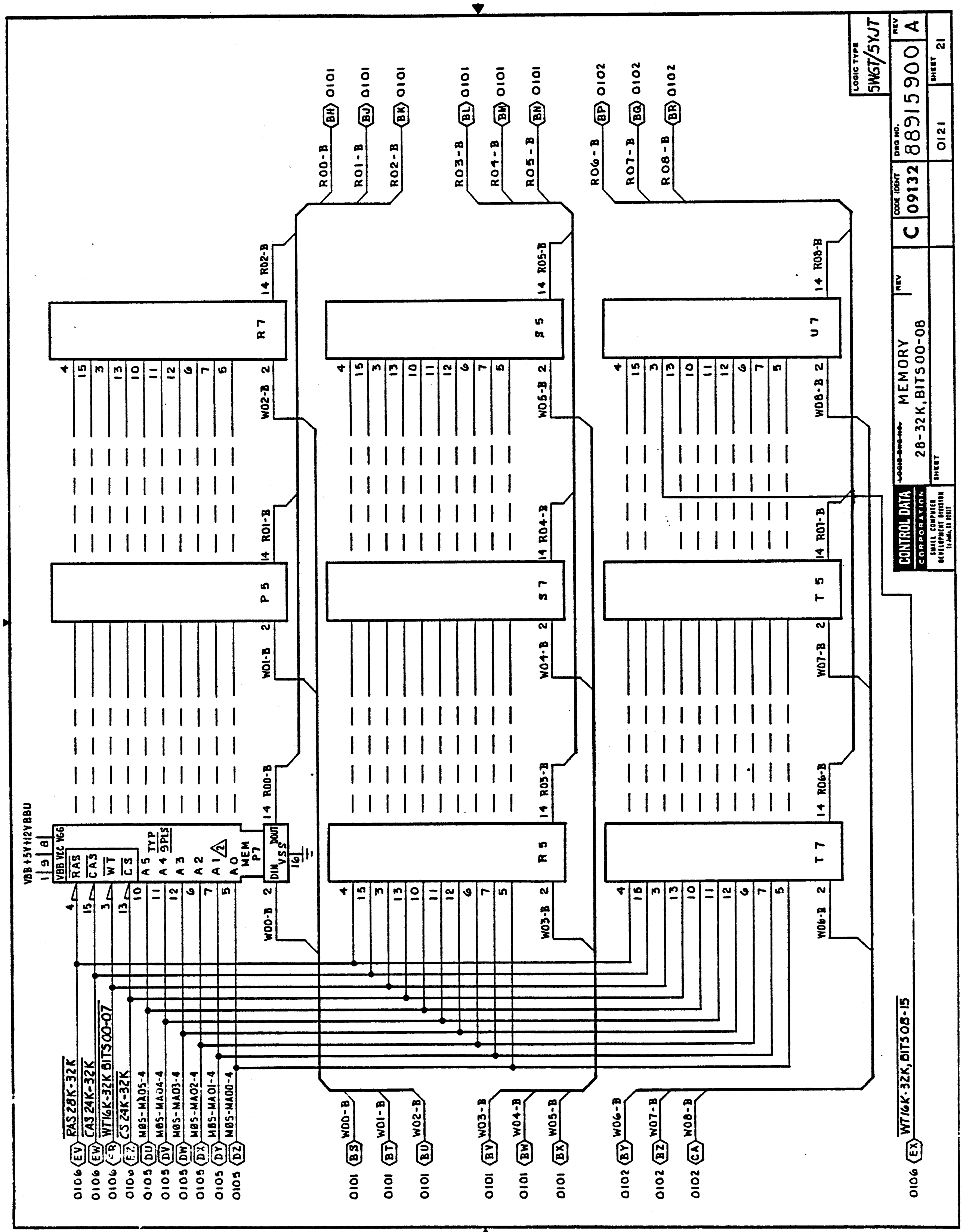

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 21 of 24)

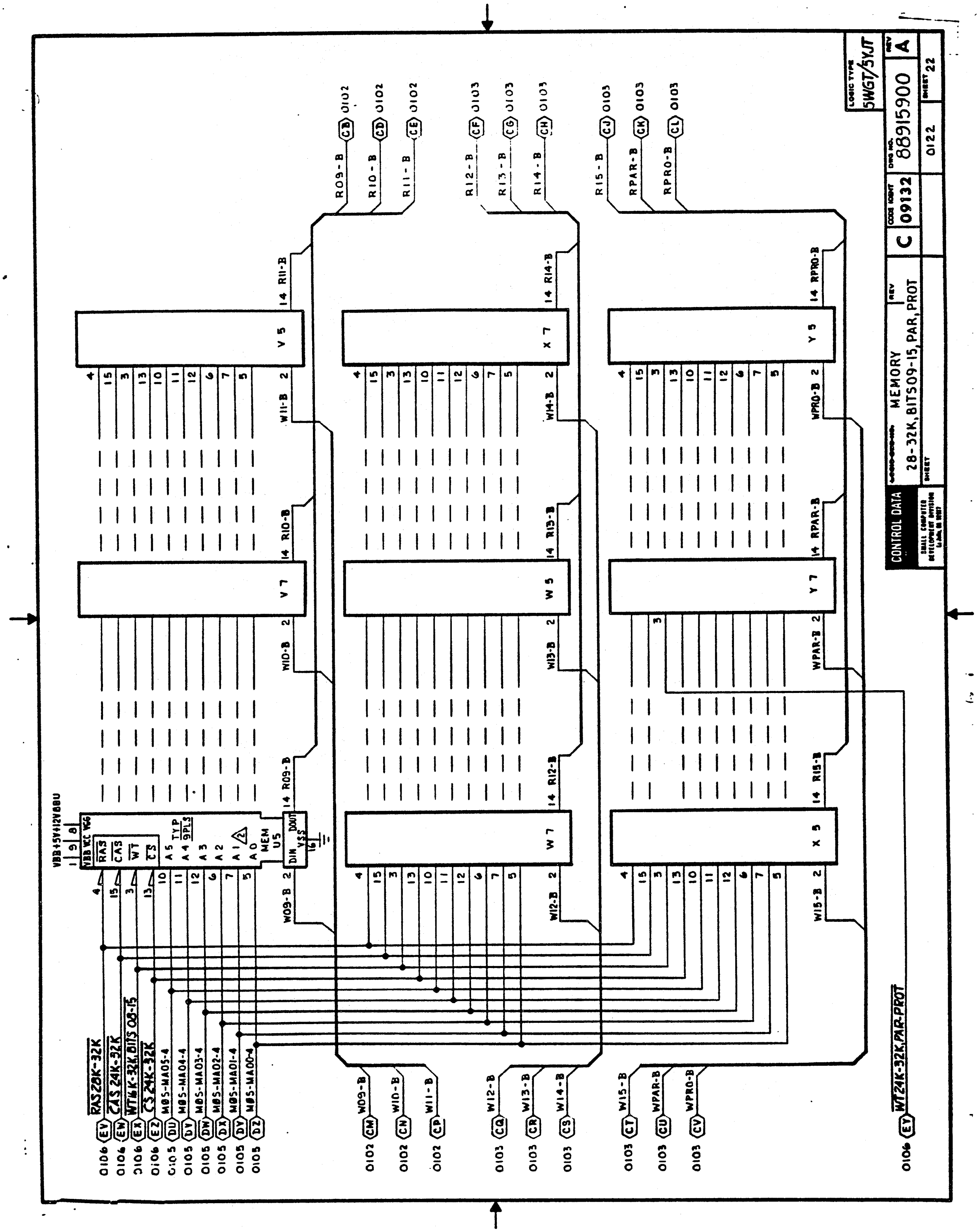

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 22 of 24)

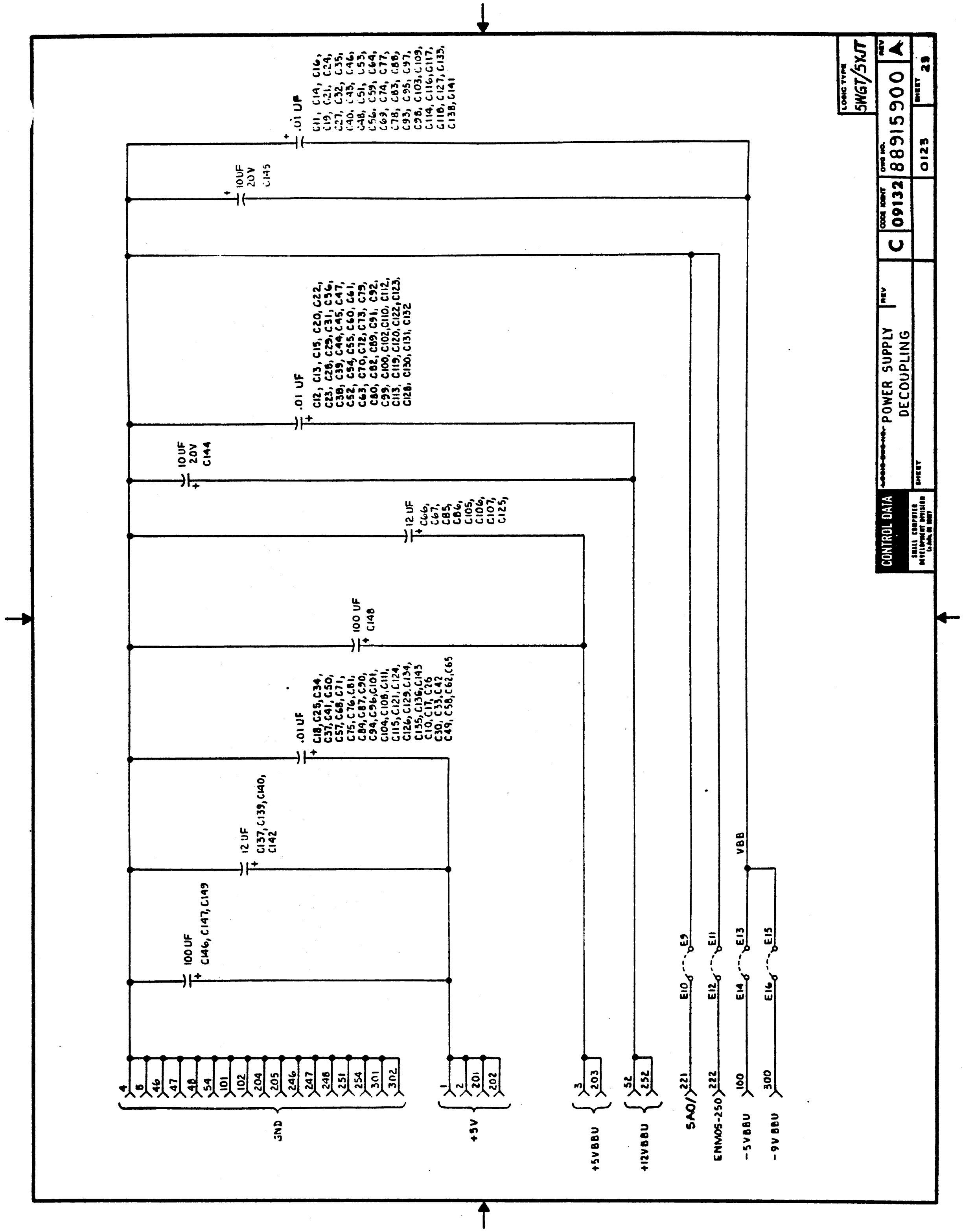

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 23 of 24)

PIN	CROSS REF. NO.	SIGNAL
1	0123	+5V
2	0123	+5V
3	0123	+5VBBU
4	0123	GND
5	0123	GND
6	BACKPLANE NOTES	X / Y / Z / AC
7	JUMPER TO 207 FOR	32K / 32K / 32K / 32K/16K
8	JUMPER TO 208 FOR	32K / 32K / 16K / 16K
9	JUMPER TO 209 FOR	32K / 16K / 16K / 16K
10	JUMPER TO 210 FOR	16K / 16K / 16K / 16K
11		SPARE
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		SPARE
26	BACKPLANE NOTES	X / Y / Z / AC
27	JUMPER TO 227 FOR	32K / 32K / 32K / 32K/16K
28	JUMPER TO 228 FOR	32K / 32K / 16K / 16K
29	JUMPER TO 229 FOR	32K / 16K / 16K / 16K
30	JUMPER TO 230 FOR	16K / 16K / 16K / 16K
31		SPARE
32		
33		
34		
35		
36		
37		
38		
39		
40		
41		
42		
43		
44		
45		SPARE
46	0123	GND
47	0123	GND
48	0123	GND
49		SPARE
50		SPARE
51		SPARE

PIN	CROSS REF. NO.	SIGNAL
52	0123	+12V BBU
53		SPARE
54	0123	GND
55		SPARE
56		
57		
58		
59		
60		
61		
62		
63		
64		
65		
66		
67		
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85		
86		
87		
88		
89		
90		
91		
92		
93		
94		
95		
96		
97		
98		
99		SPARE
100	0123	-5V BBU
101	0123	GND
102	0123	GND

PIN	CROSS REF. NO.	SIGNAL
201	0123	+5V
202	0123	+5V
203	0123	+5VBBU
204	0123	GND
205	0123	GND
206	0103	E16KNX-Y/
207	0103	E16KNX-Y/
208	0101	E16KNX-Y/ (LOWER 16K)
209	0102	E16KNX-Y/
210	0102	E16KNX-Y/
211		SPARE
212		
213		
214		
215		
216		
217		
218		
219		
220		SPARE
221	0123	SAO/
222	0123	ENMOS-250
223		SPARE
224		
225		
226		SPARE
227	0106	RASI6KX-Y/(LOWER 16K)
228		SPARE
229		SPARE
230		SPARE
231	0106	WT-MØS/
232	0106	WT-MØS/
233	0106	WT-MØS/
234		SPARE
235	0106	SLTBLK1/
236		SPARE
237	0106	CS/
238	0106	SLTBLKO/
239	0106	CAS/
240		SPARE
241	0106	SLTBLK2/
242	0106	SLTBLK3/
243		SPARE
244	0106	RASI6KI-Y (UPPER 16K)
245		SPARE
246	0123	GND
247	0123	GND
248	0123	GND
249		SPARE
250		SPARE
251	0123	GND

PIN	CROSS REF. NO.	SIGNAL
252	0123	+12VBBU
253		SPARE
254	0123	GND
255	0101	MD00
256	0101	MD03
257	0105	MØSMA01
258	0105	MØSMA00
259	0105	MØSMA03
260	0105	MØSMA02
261		SPARE
262		SPARE
263	0101	MD07
264	0105	MØSMA05
265	0105	MØSMA04
266		SPARE
267		SPARE
268	0101	MD01
269	0101	MD02
270		SPARE
271	0101	MD06
272	0101	MD08
273	0102	MD11
274	0102	MD09
275		SPARE
276		SPARE
277	0101	MD05
278		SPARE
279		SPARE
280	0101	MD04
281	0102	MD10
282	0103	MPROT
283		SPARE
284	0103	MPAR
285		SPARE
286	0103	MD14
287	0103	MD15
288		SPARE
289		SPARE
290	0103	MD13
291		SPARE
292		SPARE
293	0103	MD12
294		SPARE
295	0101	E16KN1-Y/
296	0102	E16KN1-Y/
297	0102	E16KN1-Y/ (UPPER 16K)
298	0103	E16KN1-Y/
299	0103	E16KN1-Y/
300	0123	-9VBBU
301	0123	GND
302	0123	GND

LOGIC TYPE 5WGT/5YJT

CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION	LOGIC DWG NO. I/O PIN REFERENCE	REV	C	CODE IDENT 09132	DWG NO. 88915900	REV A
	SHEET				0124	SHEET 24

Figure 5-16. 32K MOS Memory Array (PWA 96743703) Logic Diagram (Sheet 24 of 24)

SIGNAL	PIN	CROSS REF NO
CAS/	239	0102
CS/	237	0102
ECC HERE/	79	0102
ECCO0	83	0104
ECC01	85	0104
ECC02	88	0104
ECC03	91	0104
ECC04	89	0104
ENMOS-250	222	0102
ENIGKN0-1/	13	0104
ENIGKN0-2/	11	0105
ENIGKN0-3/	9	0106
ENIGKN1-1/	12	0104
ENIGKN1-2/	10	0105
ENIGKN1-3/	8	0106
GND	4	0102
GND	5	0102
GND	46	0102
GND	47	0102
GND	48	0102
GND	204	0102
GND	205	0102
GND	246	0102
GND	247	0102
GND	248	0102
GND	251	0102
GND	54	0102
GND	101	0102
GND	102	0102
GND	254	0102
GND	301	0102
GND	302	0102
MA00	258	0103
MA01	257	0103
MA02	260	0103
MA03	259	0103
MA04	265	0103
MA05	264	0103
RASIGK0-1/	24	0101
RASIGK0-2/	26	0101
RASIGK0-3/	29	0101
RASIGK1-1/	25	0101

SIGNAL	PIN	CROSS REF NO
RASIGK1-2/	30	0101
RASIGK1-3/	28	0101
SLTBLK0/	238	0101
SLTBLK1/	235	0101
SLTBLK2/	241	0101
SLTBLK3/	242	0101
WT-MOS	231	0102
+5V BB	3	0102
+5V BB	203	0102
+5V	1	0102
+5V	2	0102
+5V	201	0102
+5V	202	0102
-5V	100	0102
-9V	300	0102
+12V	52	0102
+12V	252	0102

SIGNAL	PIN	CROSS REF NO

SIGNAL	PIN	CROSS REF NO

SIGNAL	PIN	CROSS REF NO

3 ALL OUTPUT PINS AT LOC D7,K7,T7,&E7 HAVE PROVISIONS FOR CERAMIC CAP. ON PWB.

2 CDC PART NO. 15152700; NO ELEMENT IDENTIFIER AVAILABLE

1 BT97 IS SIMILAR TO 939.

NOTES UNLESS OTHERWISE SPECIFIED

DR 96738900 DETACHED LIST

	A	B	C	D	E	F
1						
2						
3						
4						
5						
6						
7						

LOGIC TITLE

LOGIC DWG NO — REV

PWA NO 96738801 — PWB NO 96738700

CONTROL DATA — SMALL COMPUTER DEVELOPMENT DIVISION

FIRST USED ON

DR	LV Tibbits	10/31/75
CHK	Gene Bricker	10-31-75
ENGR	[illegible]	10-31-75
MFG	[illegible]	
APPD	E. [illegible]	10-31-75

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.026.

AA6030

TITLE: LOGIC DIAGRAM — ECC MOS ARRAY (5XLT/5WUT)

CARD POS

LOGIC TYPE 5WUT

C — CODE IDENT NO 09132 — DRAWING NUMBER 96738900 — B

SHEET 1 OF 19

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 1 of 20)

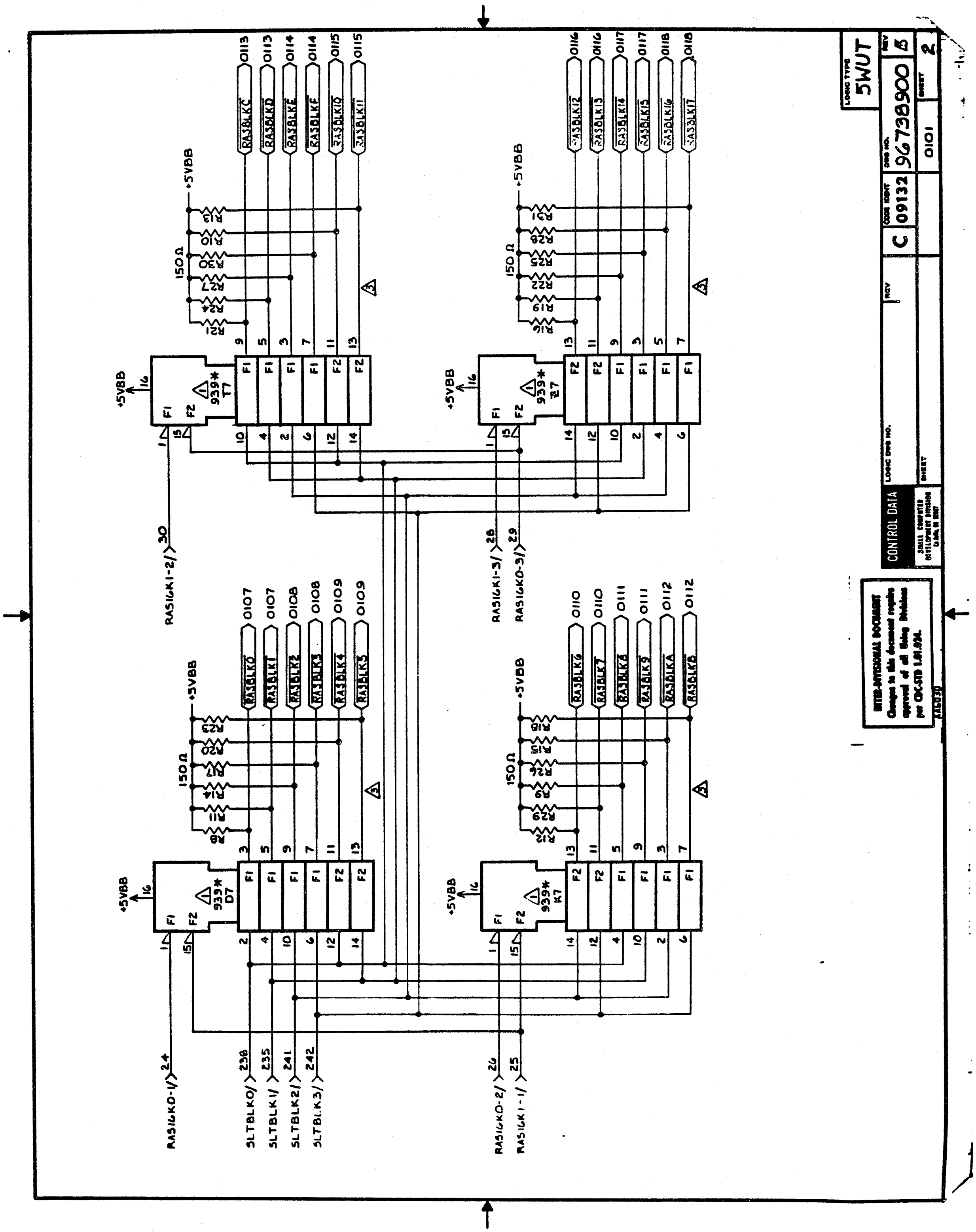

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 2 of 20)

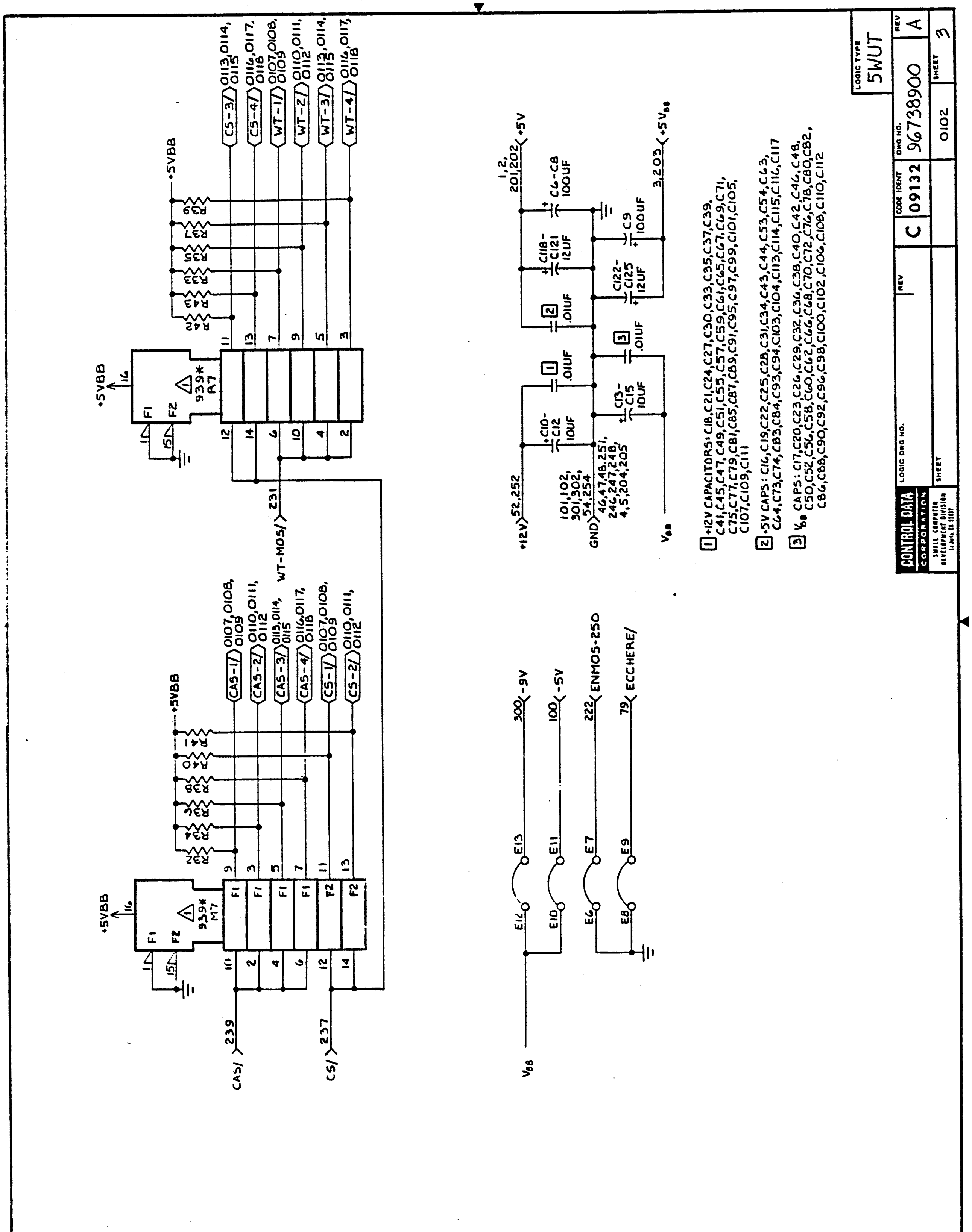

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 3 of 20)

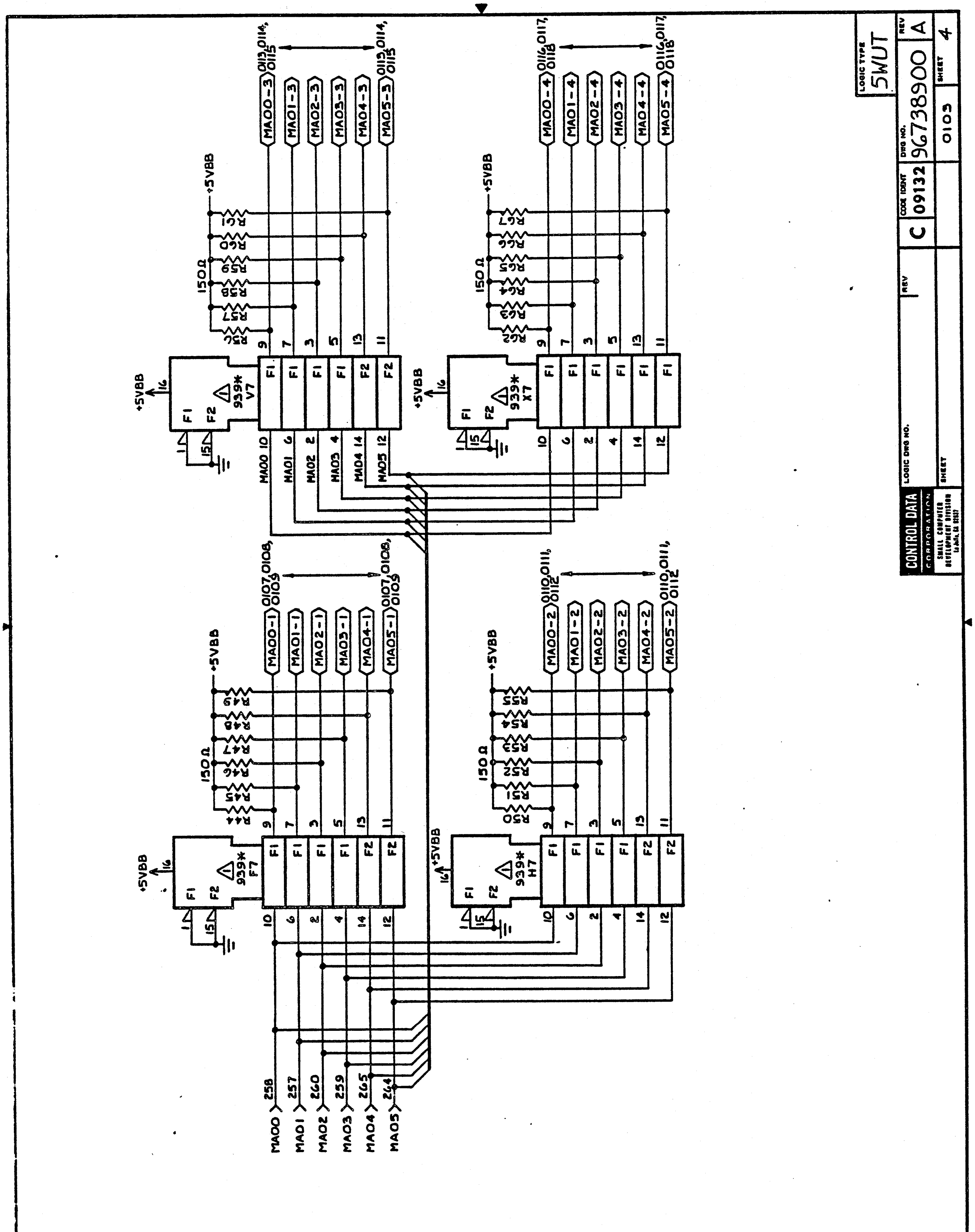

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 4 of 20)

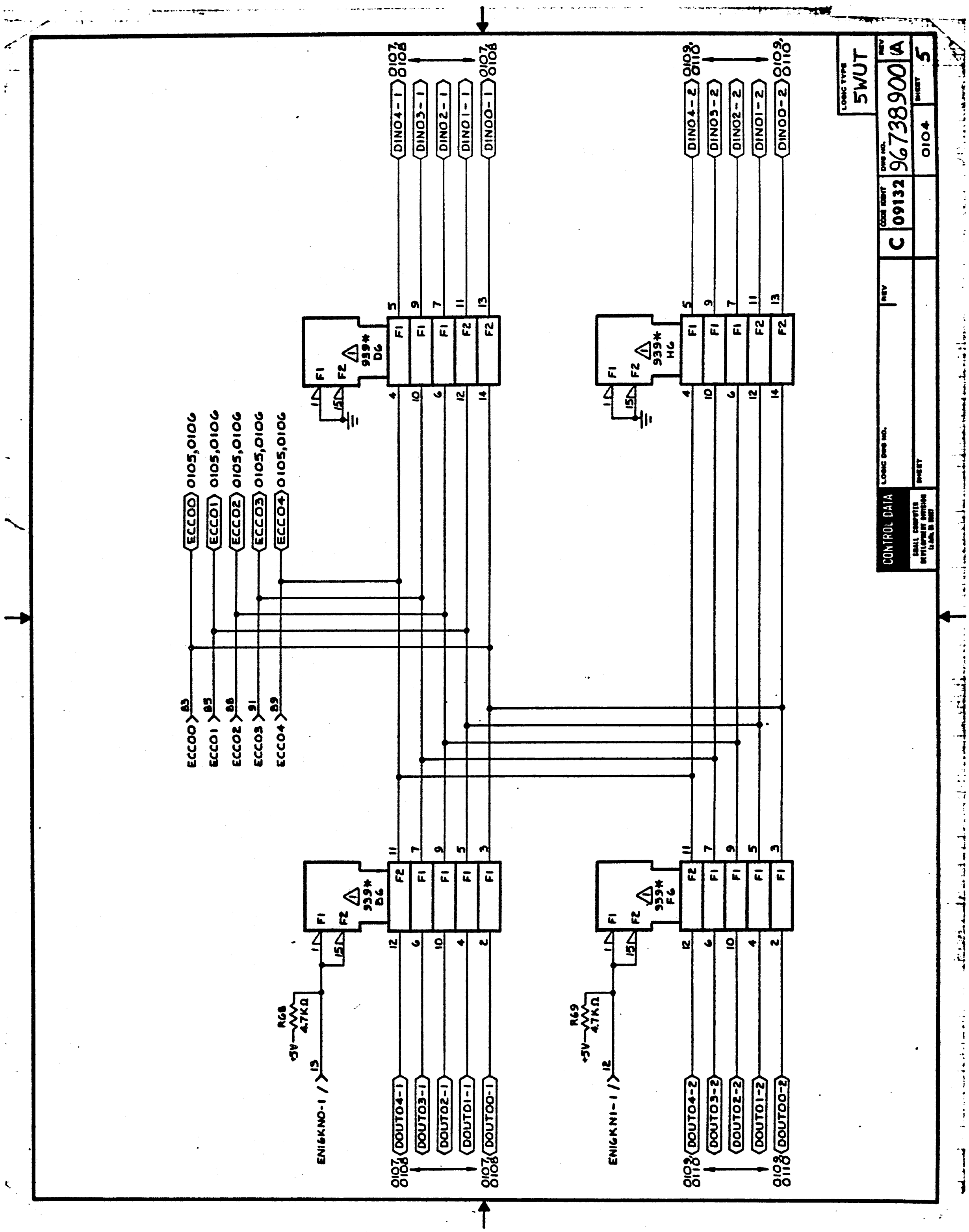

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 5 of 20)

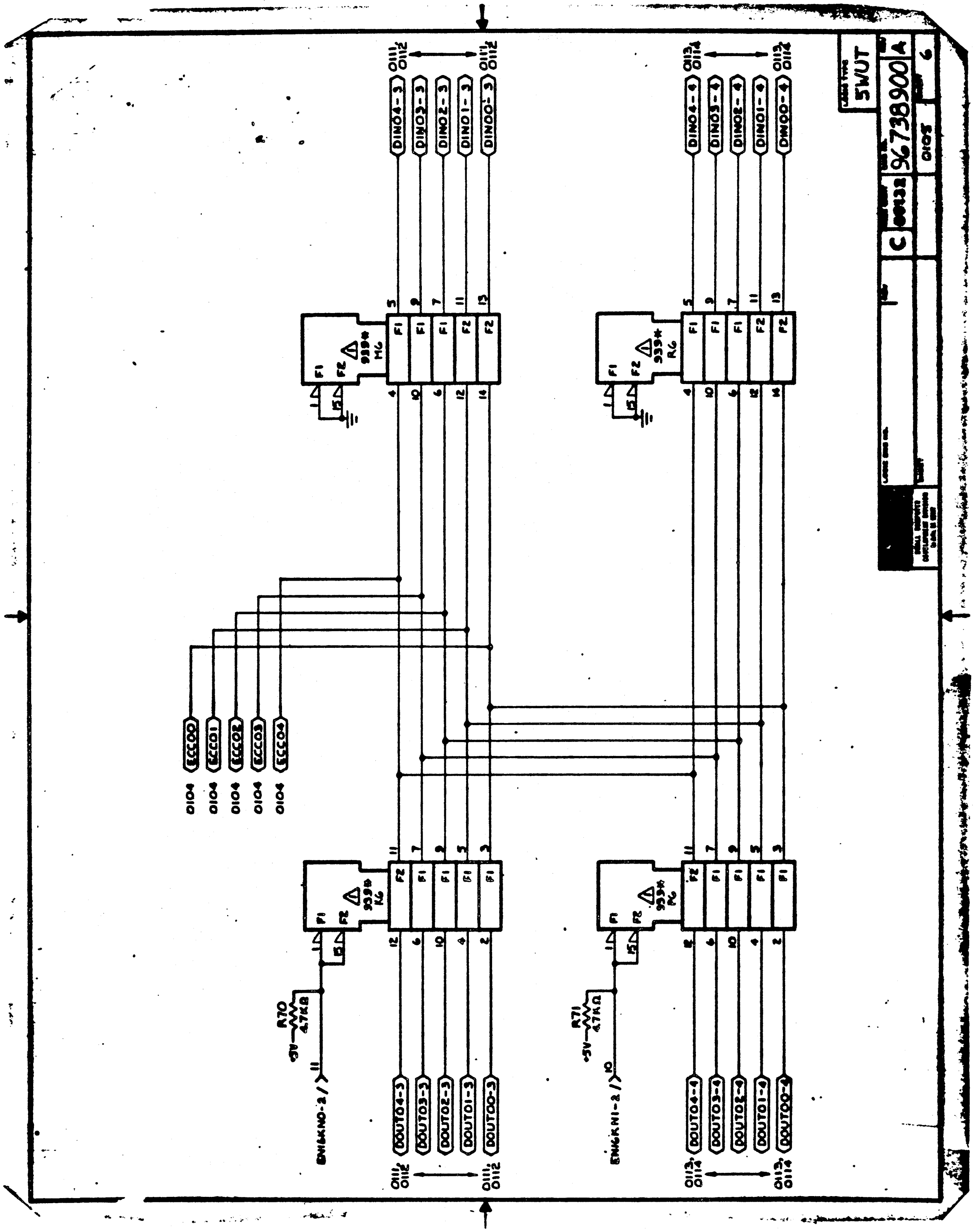

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 6 of 20)

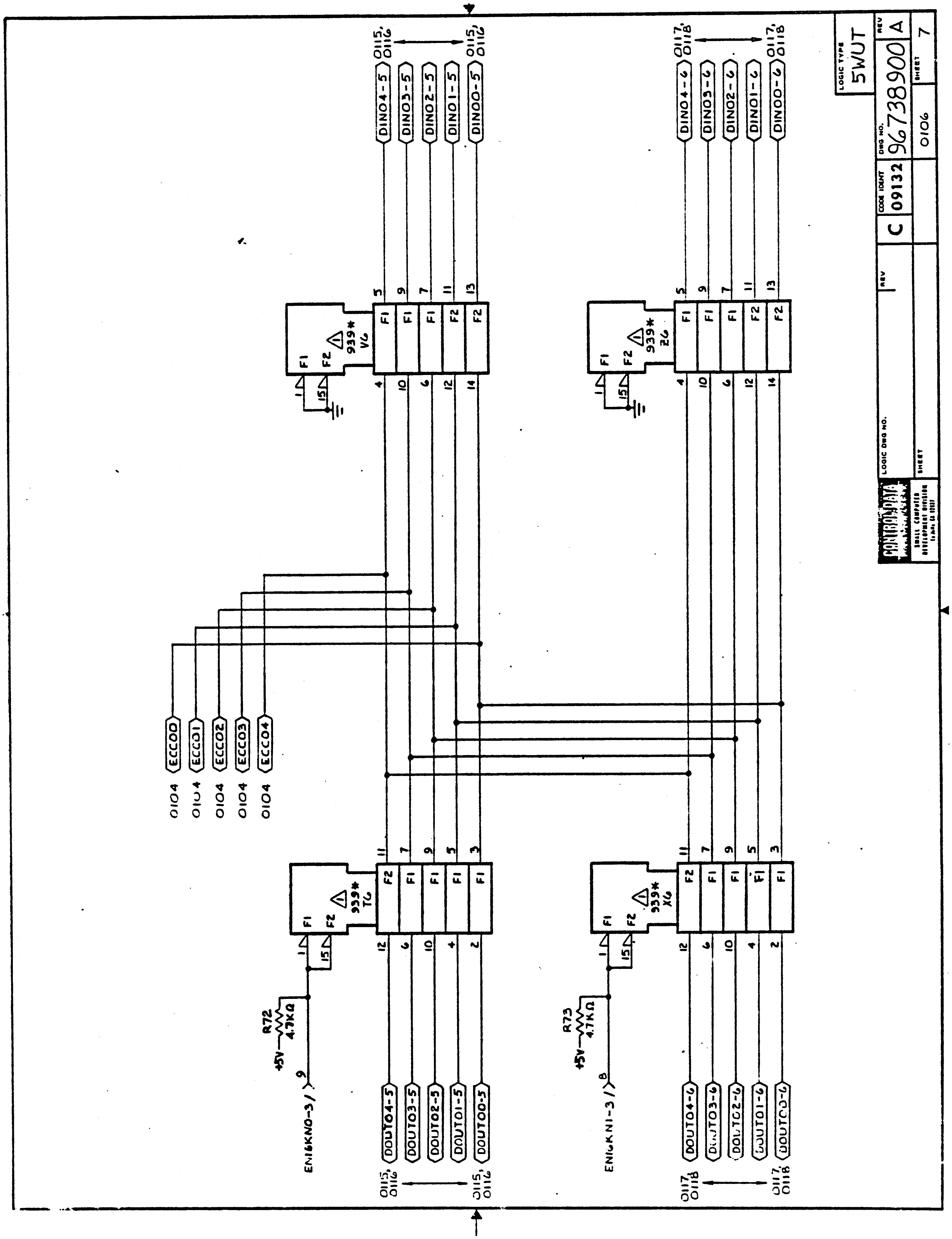

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 7 of 20)

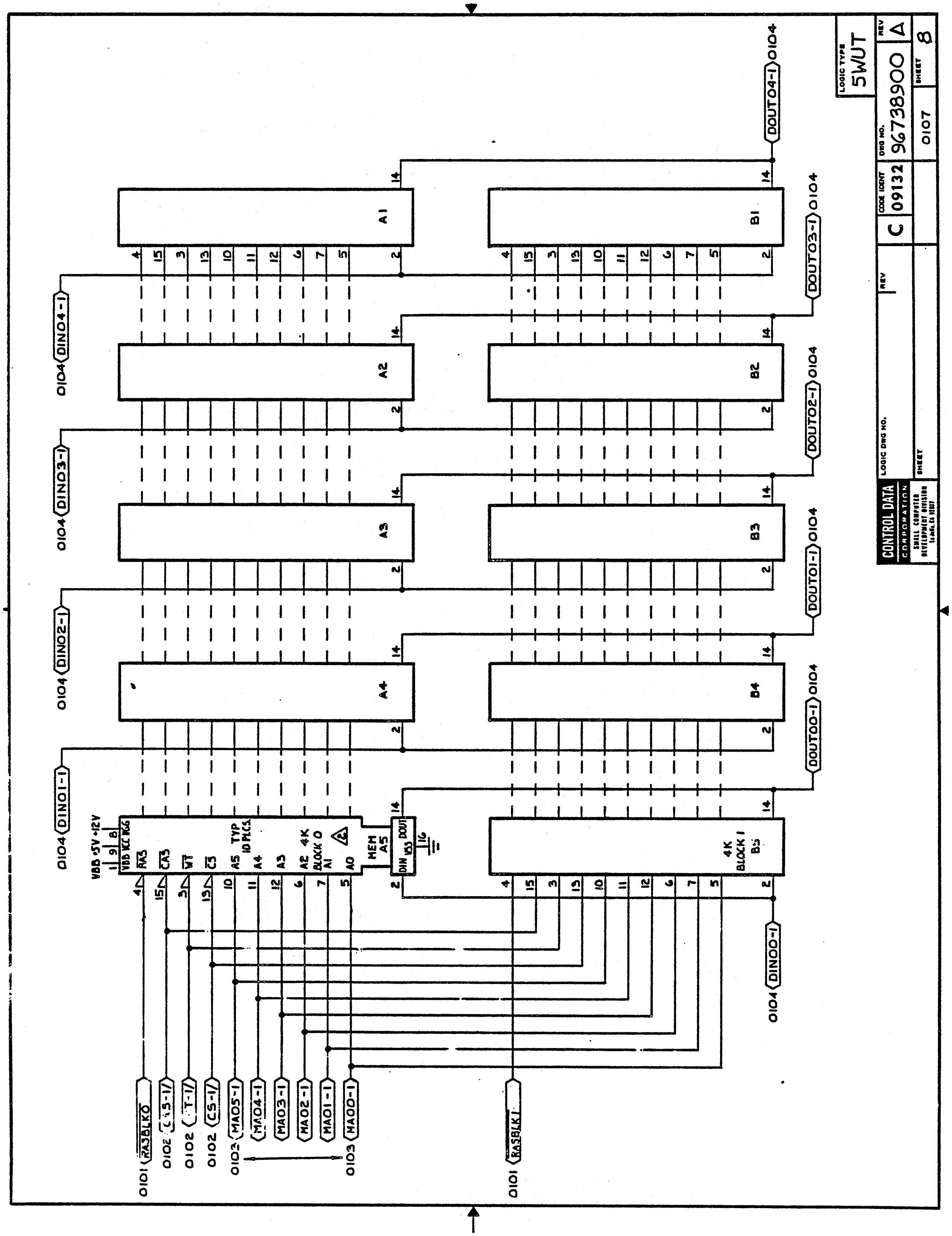

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 8 of 20)

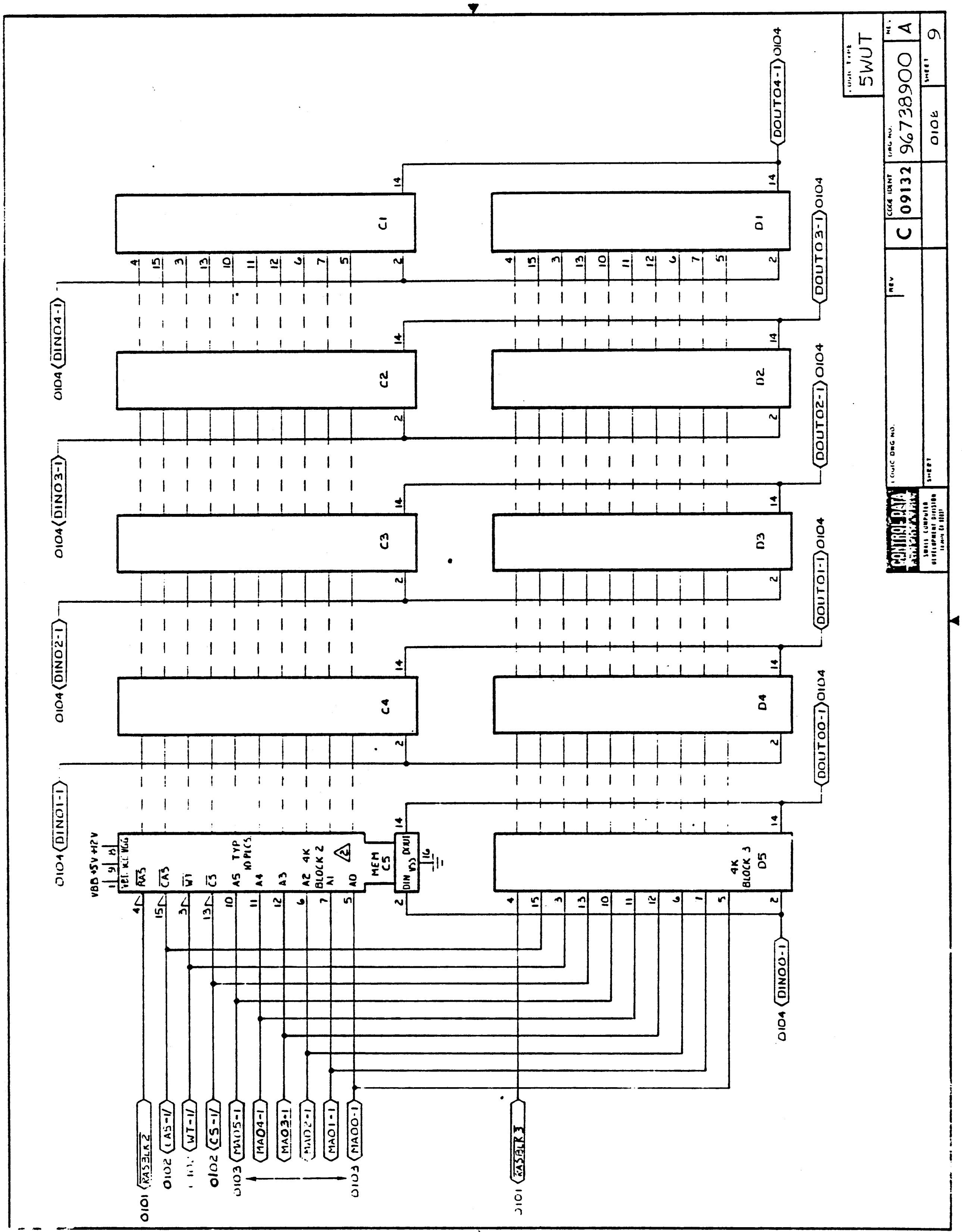

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 9 of 20)

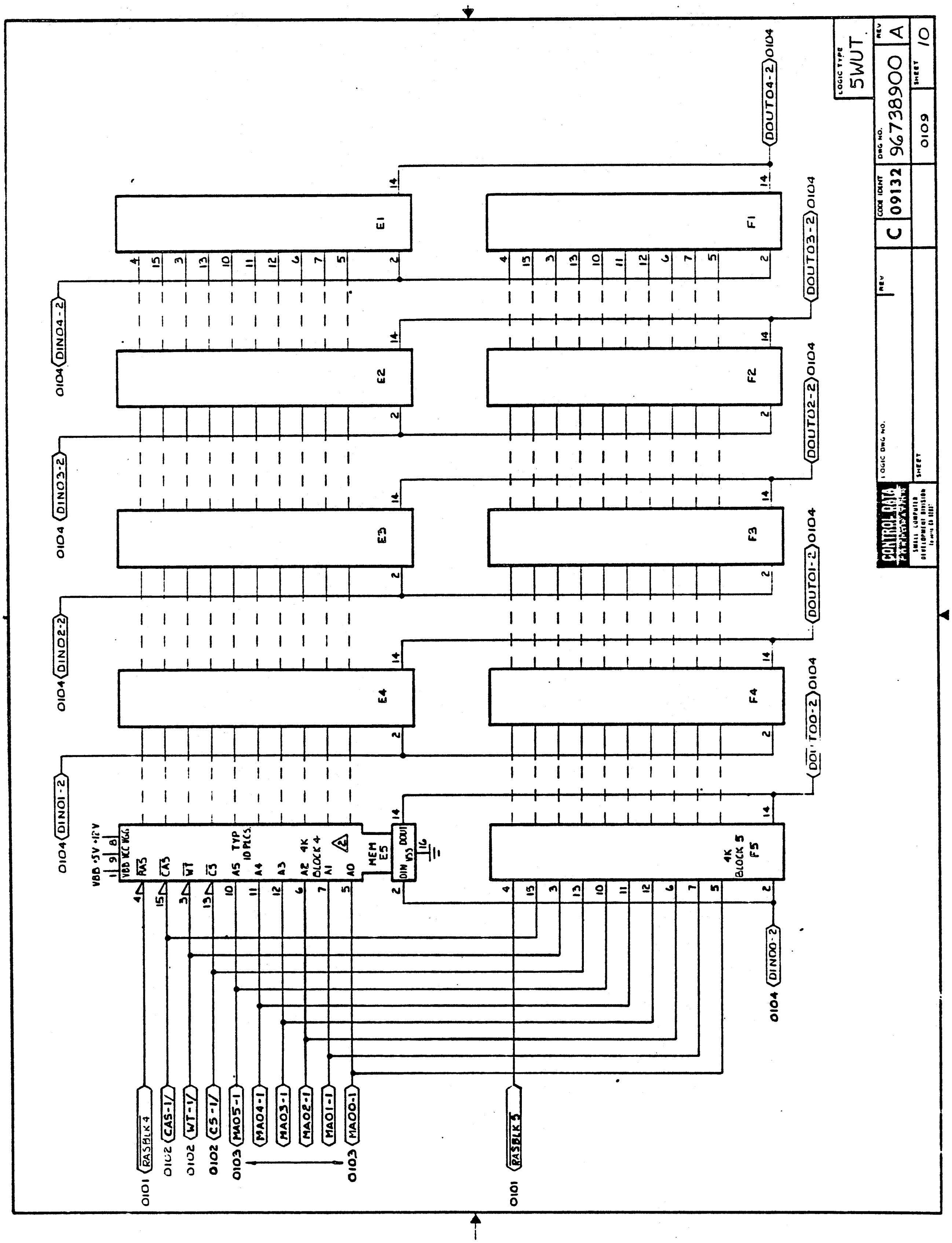

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 10 of 20)

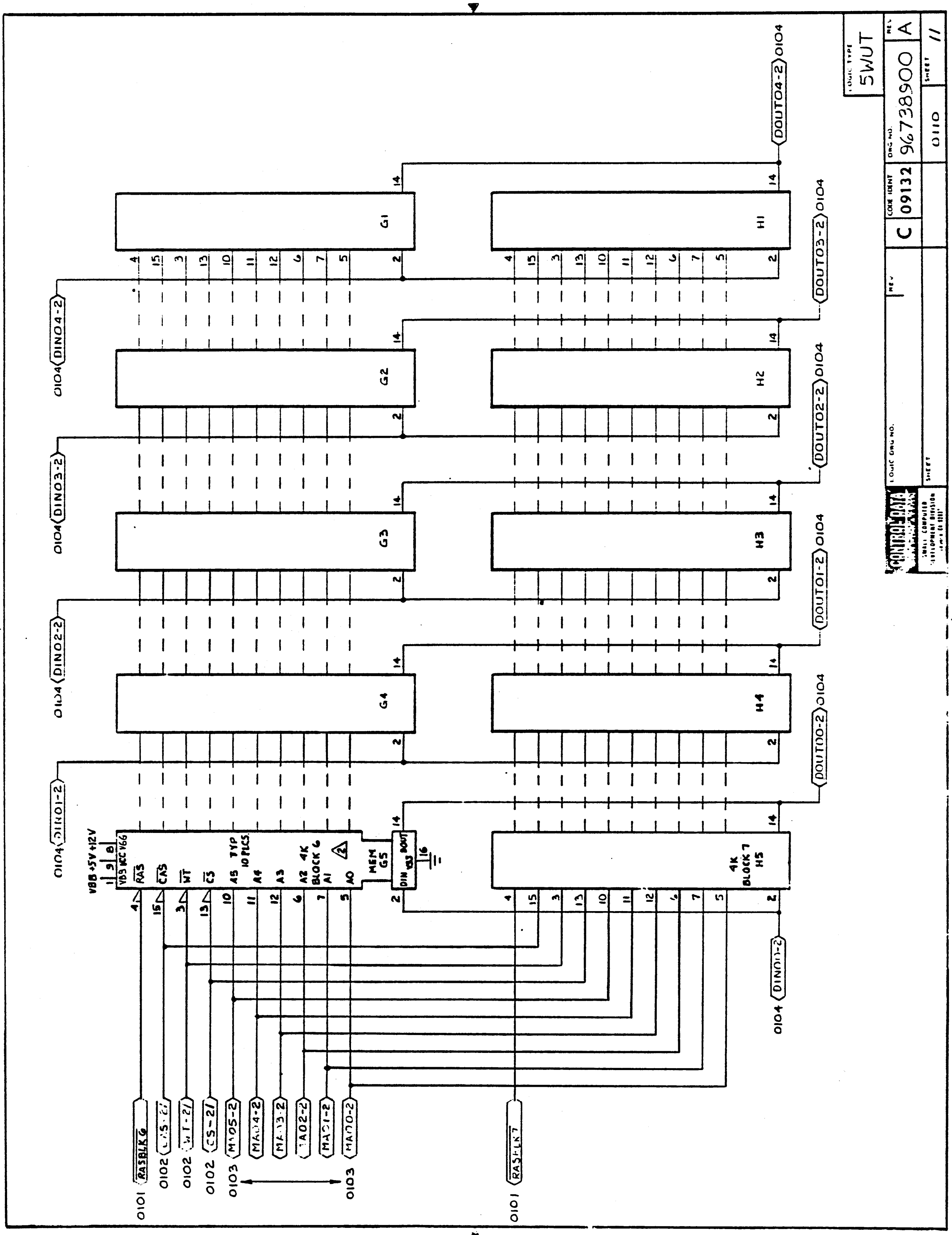

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 11 of 20)

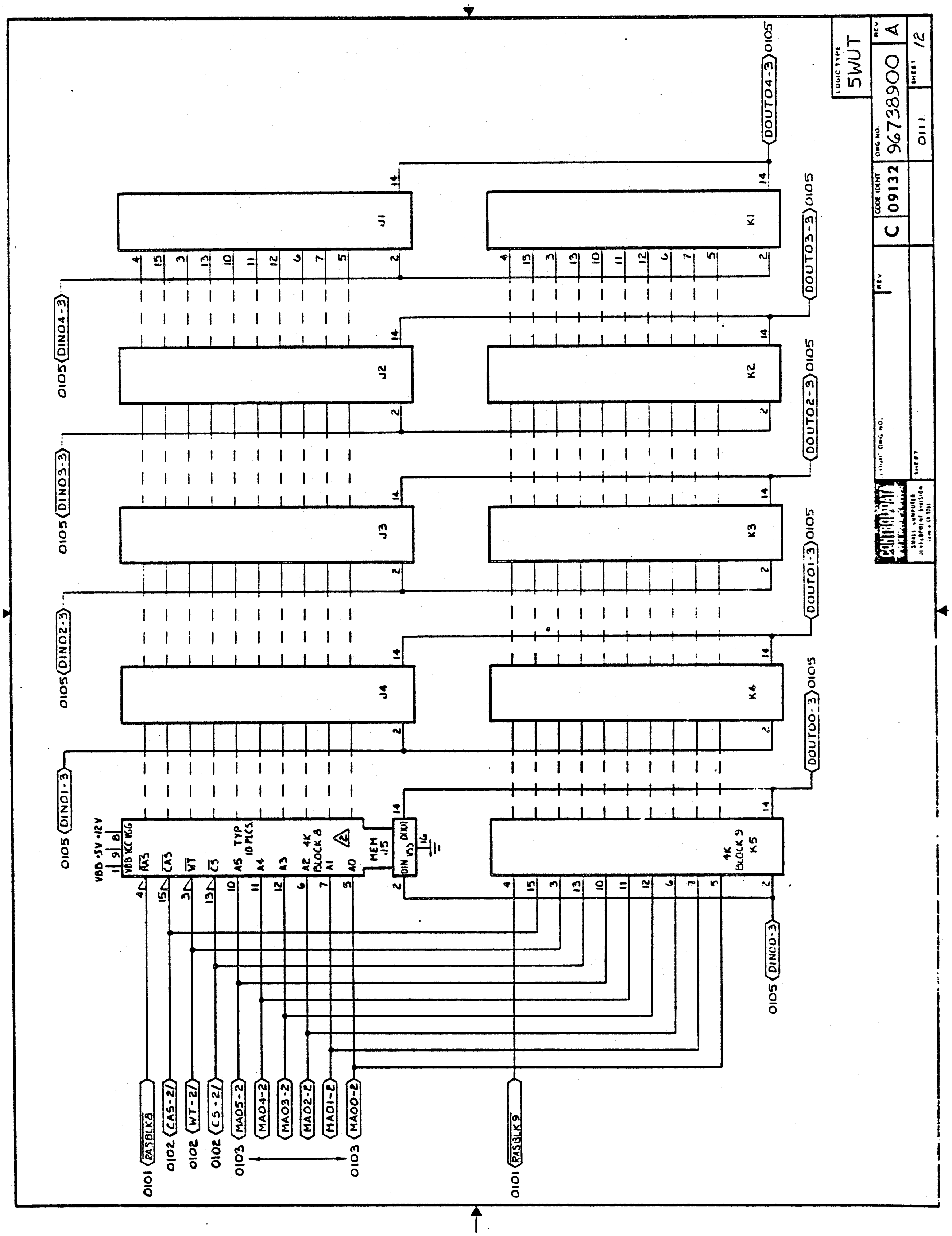

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 12 of 20)

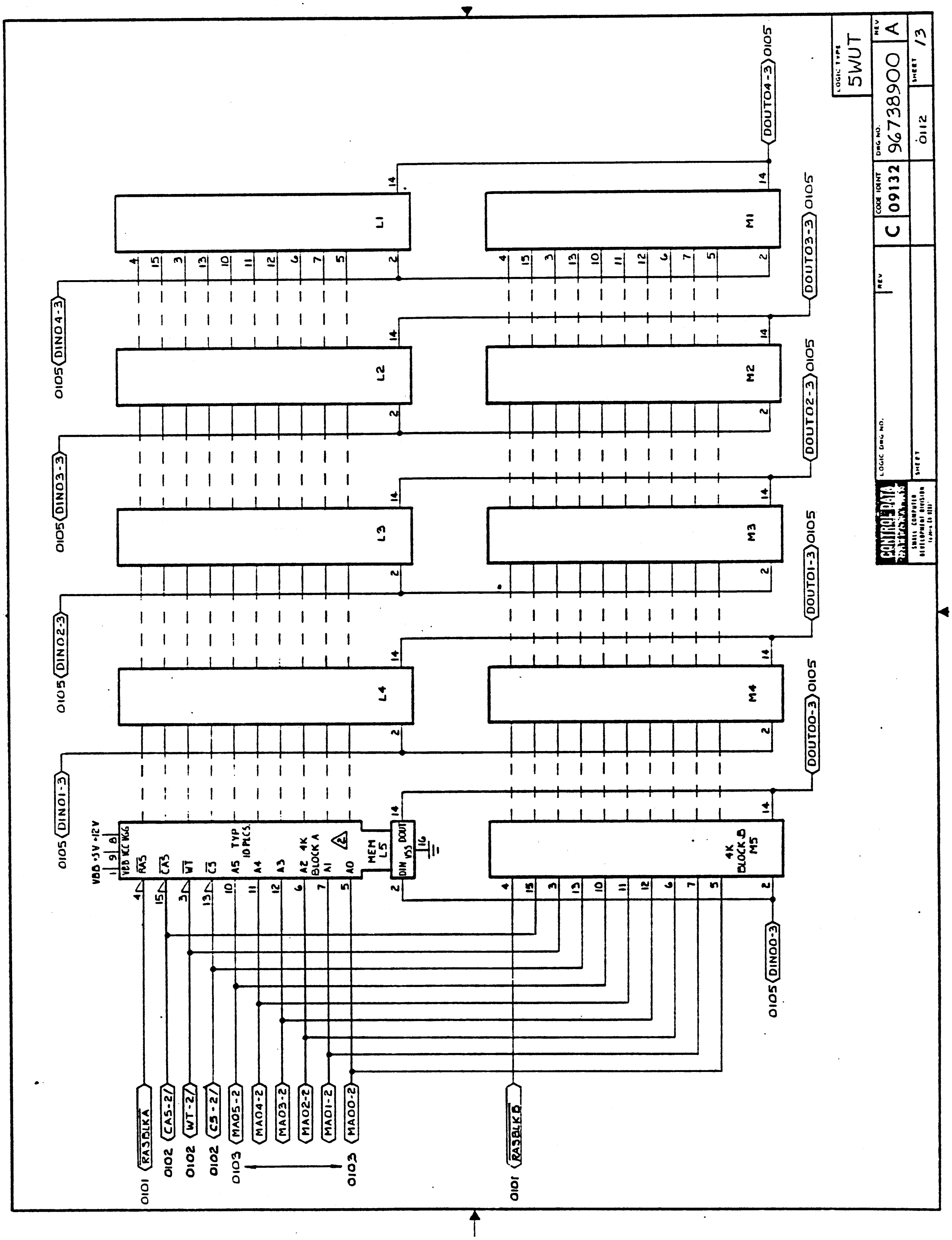

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 13 of 20)

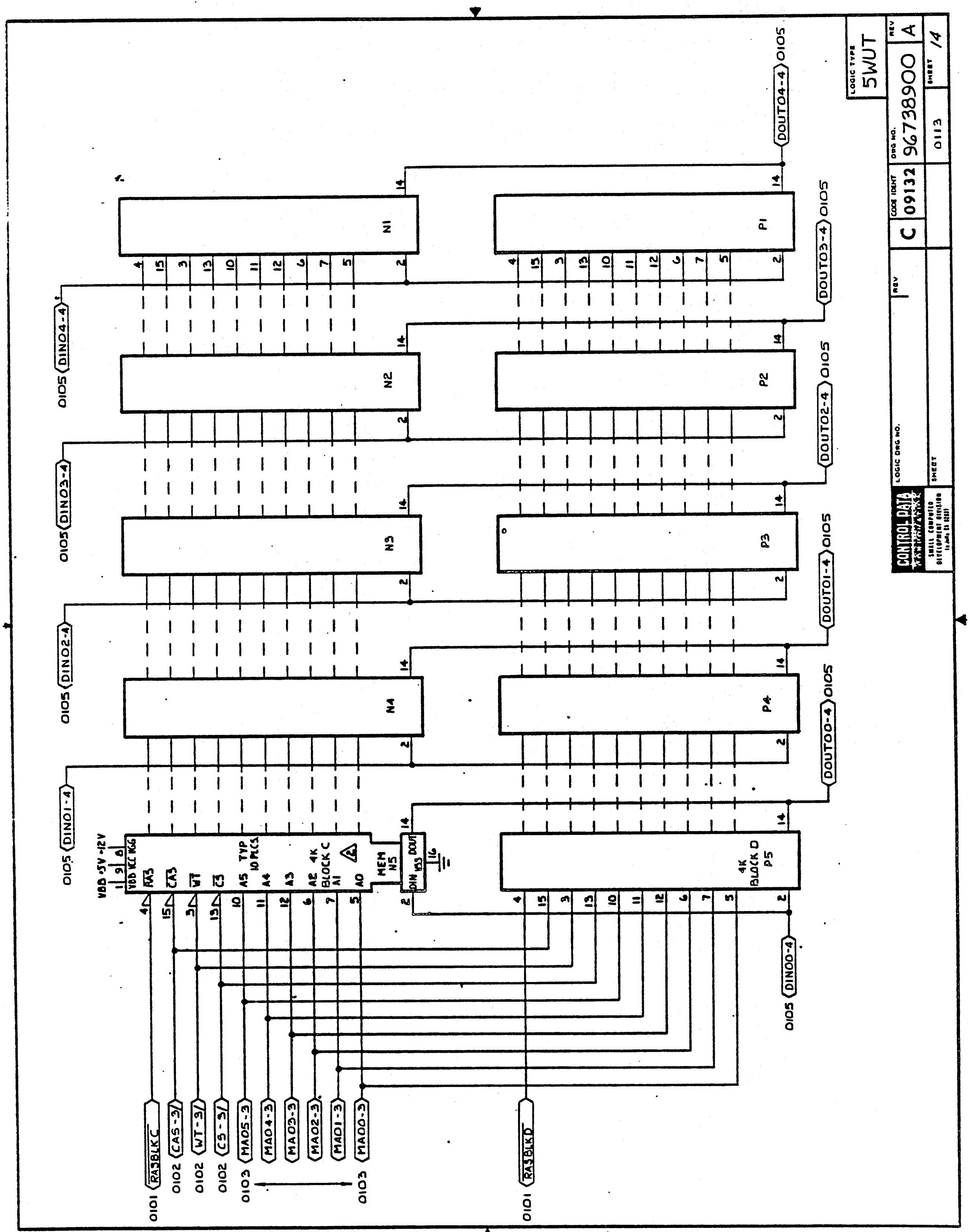

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 14 of 20)

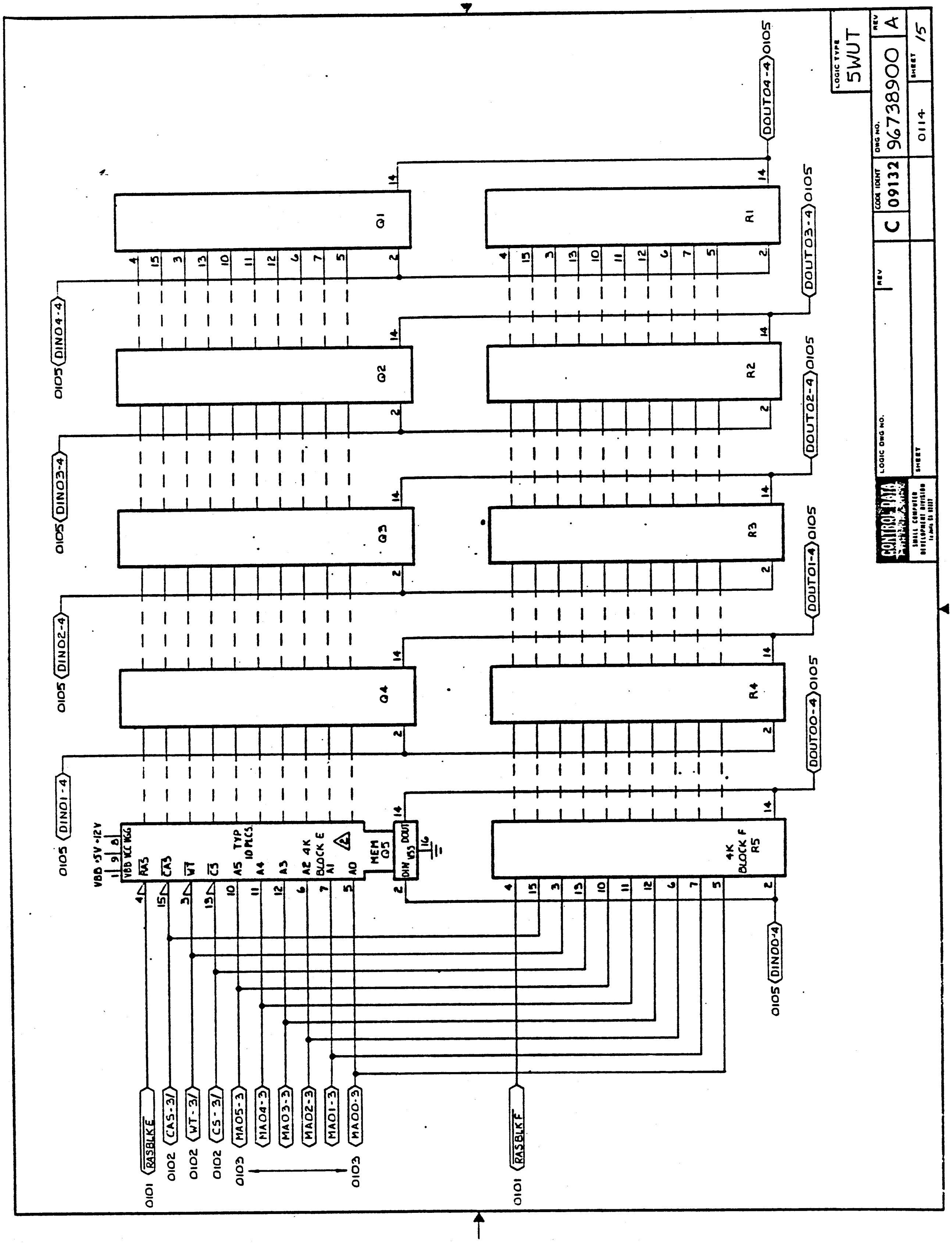

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 15 of 20)

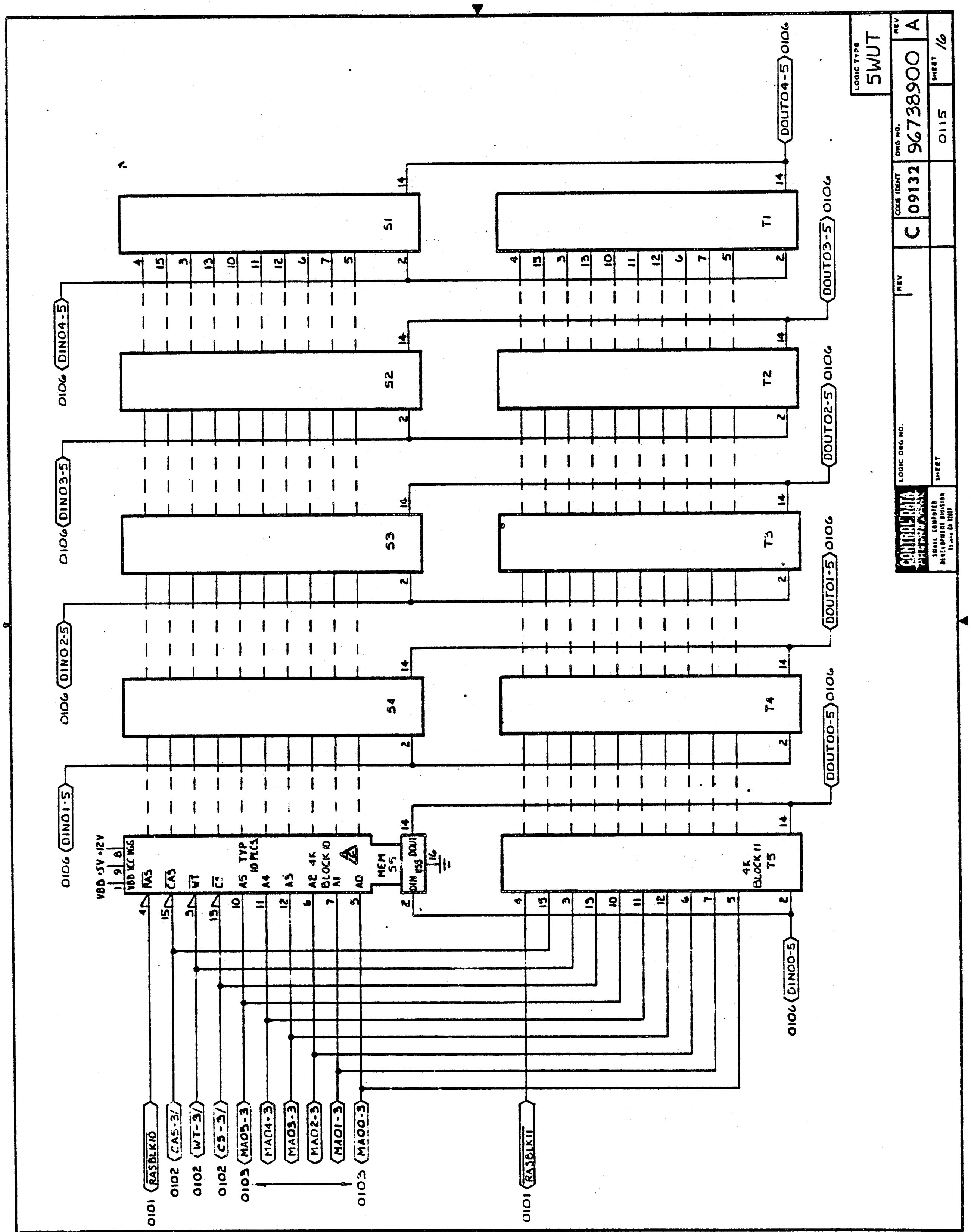

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 16 of 20)

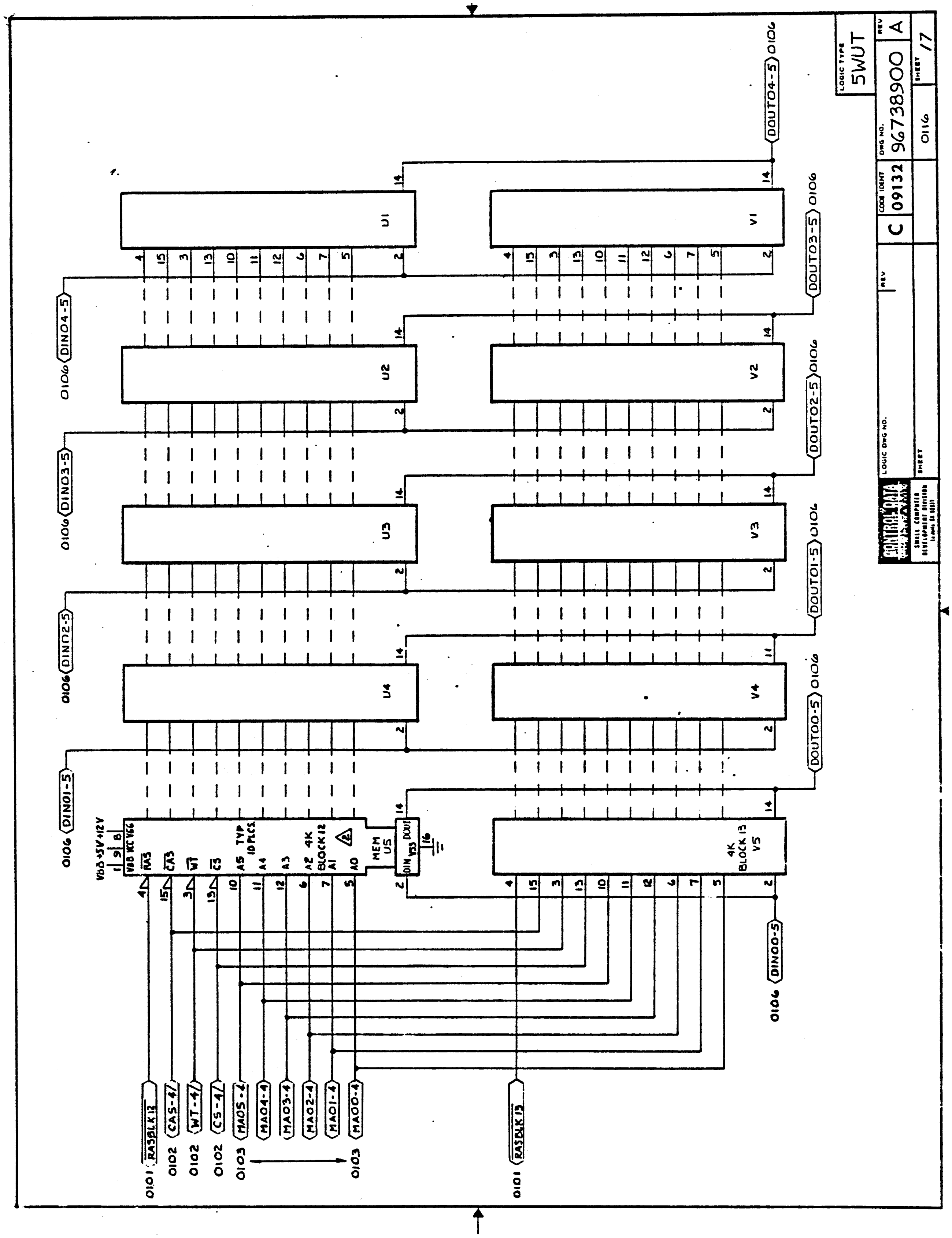

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 17 of 20)

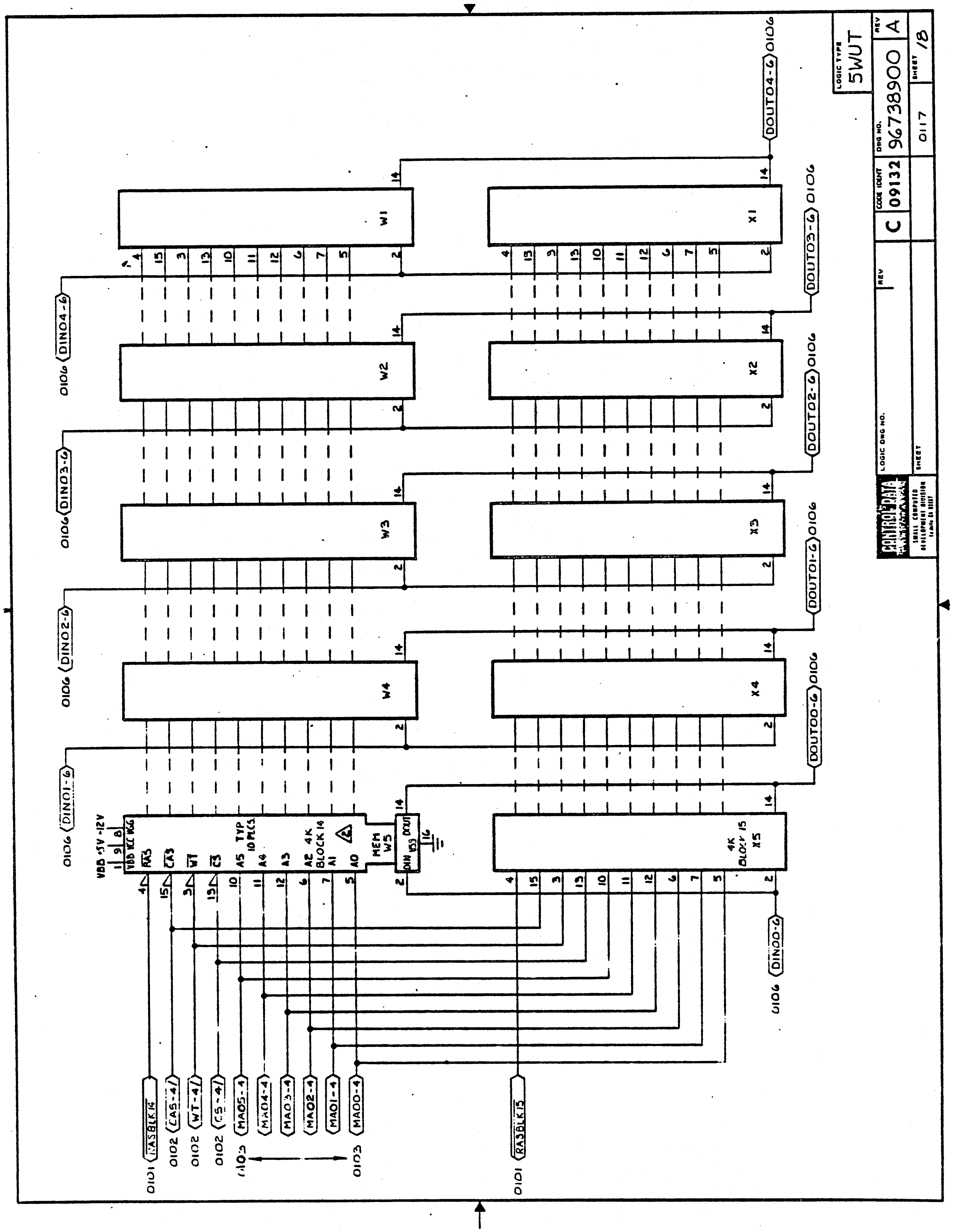

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 18 of 20)

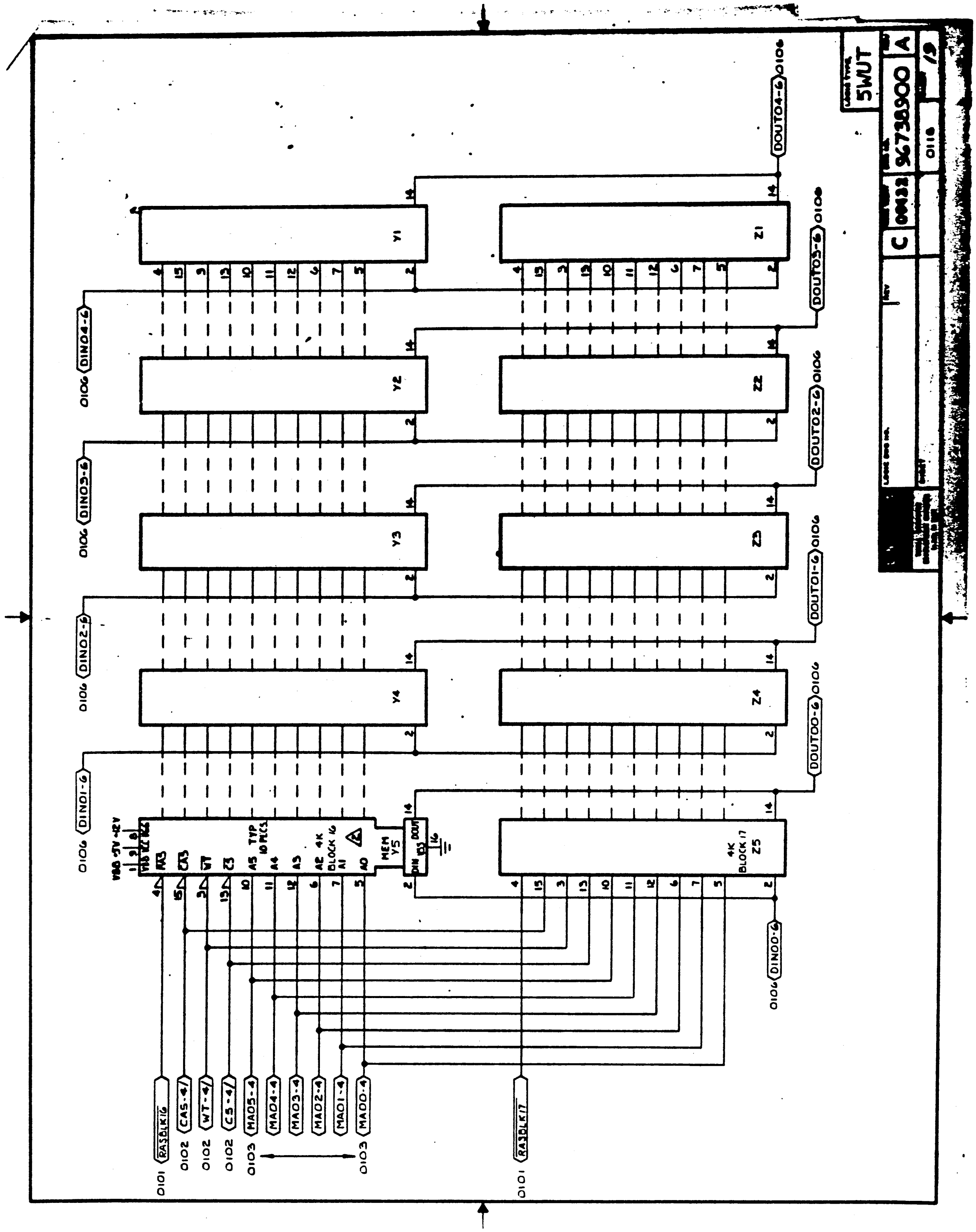

Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 19 of 20)

DWN	L.T Polelis	10/8/75	CONTROL DATA CORPORATION SMALL COMPUTER DEVELOPMENT DIVISION	TITLE LOGIC DIAGRAM-ECC MOS ARRAY (5XLT/5WUT)
CHKD	GUY BRIEN	10-31-75		PREFIX DR
ENG	[illegible]	10-31-5		DOCUMENT NO 96738900
MFG				REV B
APPR	[illegible]	2.19.76	CODE IDENT 09132	FIRST USED ON

SHEET 1 OF 1

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	14304	REDRAWN; REL. CL. B	LVP	10-31-75	[illegible]
02	14291	SEE ECO	BK	12-4-75	[illegible]
A	18312	CL. A. RELEASED	PVB	2.19.76	[illegible]
B	14575	SEE ECO	[illegible]	9.8.76	[illegible]

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NOTES:

DETACHED LISTS

AA5180 REV. 8/71

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Figure 5-17. Error Checking and Correction Array (PWA 96738801) Logic Diagram (Sheet 20 of 20)

MAINTENANCE 6

PREVENTIVE MAINTENANCE

This equipment consists of printed circuit boards that plug into the CPU chasis. Preventive maintenance for the memory consists of cleaning dirt and dust from the boards while performing preventive maintenance on the CPU. No additional preventive maintenance is required.

CALIBRATION AND ALIGNMENT

No field calibration and alignment procedures are required.

TROUBLESHOOTING

Troubleshoot to the board level using the ODS diagnostic memory tests.

PARTS DATA 7

This section contains the spare parts lists and assembly drawings applicable to the MOS memory subsystem.

DWN	L.V. Pidlas	4/3/75	CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION
CHKD	Guy Bahls	12/17/75	
ENG	W. H.	1-2-76	
MFG			
APPR	E. Klein	1-29-76	CODE IDENT 89132

TITLE SPL-MOS MAIN MEMORY I/F W/ECC CNT.

FIRST USED ON MP17/BA212-A

PREFIX SP DOCUMENT NO 96752600 REV J

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	18265	CL.B PRE-RELEASED	LVP	1-28-76	
02	14404	FN 2 WAS 96740800	BR		
A	14472	CL. A. RELEASED	BR	5-10-76	
B	14616	SEE ECO		11-15-76	
C	DS14761	CHANGED F/N 1 & 2	DL	7-13-77	AW
D	DS14982	ADDED NOTE 1. REVISED P/L		11-14-77	LP
E	DS21078	ADD. NOTE 2 & REVISED P/L		1-24-78	AW
F	DS22127	ADD'D NOTE 3 & CHG PL		11-6-81	
G	DS22172	P/L CHG	BR	4-5-82	AW
H	DS22187	SEE ECO	J.V.W.	8-25-82	AW
J	DS22294	P/L CHG ONLY		7-27-83	AW

NOTES:

DETACHED LISTS

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL		ASSEMBLY DESCRIPTION		FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96752600	J	A	A	SPL-MOS MAIN MEM I/F W/ECC CNT	DS	MP17	01/06/76	022294	07/22/83	MF

FIND NUMBER		PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	PART TYPE		
~~1~~	~~D~~	~~96740560~~	~~1.00~~	~~PC~~	~~PWA-MOS MEM ADDRESS/CONTL 5XAT~~	~~OUT~~	~~014616~~	~~100876~~	~~AYM4~~		~~N~~
2	D	96740800	1.00	PC	PWA-MOS MEM INTFC (DATA) 5XRT	OUT	014404	032276	AYM4		N
2	D	96743739	1.00	PC	PWA-MOS MEM I/F (DATA) 6ZFT	IN	014404	032276	AYM4		N
2	D	96743739	1.00	PC	PWA-MOS MEM I/F (DATA) 6ZFT	OUT	014761	070177	AYM4		N
2	D	96752104	1.00	PC	PWA-MOS MEM I/F DATA 7FWT	IN	014982	111877	AYP4		N
2	D	96752104	1.00	PC	PWA-MOS MEM I/F DATA 7FWT	OUT	022172	032382	AYP4		N
1	D	96752107	1.00	PC	PWA-MOS MEM I/F ADDR 7FXT	IN	014982	111877	AYM4		N
1	D	96752107	1.00	PC	PWA-MOS MEM I/F ADDR 7FXT	OUT	014982	112177	AYM4		N
1	D	96752170	1.00	PC	PWA-MOS MEM I/F ADDR/CONT 8GVT	IN	021078	032078	AYP4		N
1	D	96752170	1.00	PC	PWA-MOS MEM I/F ADDR/CONT 8GVT	OUT	022127	102381	AYP4		N
1	D	96752173	1.00	PC	PWA-MOS MEM I/F ADDR/CONT 8GWT	IN	021078	031778	AYM4		N
1	D	96752173	1.00	PC	PWA-MOS MEM I/F ADDR/CONT 8GWT	OUT	021078	032078	AYM4		N
1	D	96753817	1.00	PC	PWA-MOS MEM ADDRESS 6AYT	IN	014616	100876	AYM4		N
1	D	96753817	1.00	PC	PWA-MOS MEM ADDRESS 6AYT	OUT	014761	070177	AYM4		N
2	D	96753895	1.00	PC	PWA-MOS MEM I/F (DATA) 6CHT	IN	014761	070177	AYM4		N
2	D	96753895	1.00	PC	PWA-MOS MEM I/F (DATA) 6CHT	OUT	014982	111877	AYM4		N
1	D	96753897	1.00	PC	PWA-MOS MEM ADDRESS (6CJT)	IN	014761	070177	AYM4		N
1	D	96753897	1.00	PC	PWA-MOS MEM ADDRESS (6CJT)	OUT	014982	111877	AYM4		N
1	D	96754583	1.00	PC	PWA-MOS MEM I/F ADDR/CONT 7DTT	IN	014982	112177	AYM4		N
~~1~~	~~D~~	~~96754583~~	~~1.00~~	~~PC~~	~~PWA-MOS MEM I/F ADDR/CONT 7DTT~~	~~OUT~~	~~021078~~	~~031778~~	~~AYM4~~		~~N~~
2	D	96890065	1.00	PC	PW ASSY-MOS MEMORY INTF (DATA)	IN	022172	032382			N
~~1~~	~~D~~	~~96890550~~	~~1.00~~	~~PC~~	~~PWA-MEMORY I/F ADDRESS 81NXT~~	~~IN~~	~~022127~~	~~102381~~			~~N~~
~~1~~	~~D~~	~~96890550~~	~~1.00~~	~~PC~~	~~PWA-MEMORY I/F ADDRESS 81NXT~~	~~OUT~~	~~022187~~	~~102582~~			~~N~~
~~1~~	~~D~~	~~96890551~~	~~1.00~~	~~PC~~	~~PWA-MEMORY I/F ADDRESS 81PUT~~	~~IN~~	~~022187~~	~~102582~~			~~N~~
~~1~~	~~D~~	~~96890551~~	~~1.00~~	~~PC~~	~~PWA-MEMORY I/F ADDRESS 81PUT~~	~~OUT~~	~~022294~~	~~072283~~			~~N~~
1	D	96890552	1.00	PC	PWA-MEMORY I/F ADDRESS 83RNT	IN	022294	072283			N

NUMBER OF LINE ITEMS = 26
HIGHEST FIND NUMBER = 2

Figure 7-1. BA212-A MOS Memory Interface Spare Parts List

2M

DWN	B. Roberts	12-11-75	CONTROL DATA	TITLE SPL - 16K MOS MEMORY EXPANSION	PREFIX SPL	DOCUMENT NO. 96743811	REV B
CHKD		1-8-6	SMALL COMPUTER DEVELOPMENT DIVISION	FIRST USED ON AT275-B		SHEET	
ENG		1-8-6	CODE IDENT 09132				
MFG							
APPR	E.	2-6-76					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	18267	CL B PRE-RELEASED	BR	2-6-76	
A	14462	CL A. RELEASED	BR	5-11-76	
B	D521778	ADDED 96762000	CAB	12-10-79	AK

NOTES:

DETACHED LISTS

AA3100 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S : SPARE PARTS
N : NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96743811	B	CLA	A	SPL-16K MOS MEMORY EXPANSION	US	MP16C	01/05/76	12/08/79	

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	S OR N
1	D	96743702	1.00	PC	PWA 16K X 18 MOS MEMORY ARRAY	IN			AY46		N
2	A	96762000	1.00	PC	MOS ARRAY ADDRESS CONNECTOR	IN	021778	120779	AY46		N
					NUMBER OF LINE ITEMS = 2						
					HIGHEST FIND NUMBER = 2						

PROJECT ENGINEER

SCMD

AA 2700-1 REV 7-75

Figure 7-2. AT275-B 16K MOS Memory Array Spare Parts List

2 M

DWN	B. Roberts	12-15-75	CONTROL DATA	TITLE SPL 32K MOS MEMORY EXPANSION	PREFIX SPL	DOCUMENT NO. 96743812	REV B
CHKD	B. Law	1-8-6	SMALL COMPUTER DEVELOPMENT DIVISION				
ENG		1-8-6		FIRST USED ON AT241-B		SHEET	
MFG			CODE IDENT 09132				
APPR	E. Kuru	2-6-76					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	18267	CL. B. PRE-RELEASED	BR	2-6-76	E.G.
A	14462	CL. A. RELEASED	BR	5-11-76	E.G.
B	DS21778	ADDED 96762000	CAB	12-10-79	AW

NOTES:

DETACHED LISTS

AA3100 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96743812	B	CLA	A	SPL-32K MOS MEMORY EXPANSION	DS	MP16C	01/05/76	12/08/79	

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	S OR N
1	D	96743703	1.00	PC	PWA 32K X 18 MOS MEMORY ARRAY	IN			AYM4		N
2	A	96762000	1.00	PC	MOS ARRAY ADDRESS CONNECTOR	IN	021778	120779	AYM4		N
					NUMBER OF LINE ITEMS = 2						
					HIGHEST FIND NUMBER = 2						

PROJECT ENGINEER

SCMD

AA 2709-1 REV 7 75

Figure 7-3. AT241-B 32K MOS Memory Array Spare Parts List

DWN	B. Roberts	1-28-76	CONTROL DATA	TITLE SPARE PARTS LIST FOR ECC MOS MEM ARRAY(98Kx5) 280ns	PREFIX SP	DOCUMENT NO. 96787600	REV. A
CHKD		4/13/76	SMALL COMPUTER DEVELOPMENT DIVISION	FIRST USED ON DT223-B		SHEET	
ENG		4/14/76	CODE IDENT 09132				
MFG							
APPR	E. Mann	4-15-76					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	18296	CL A RELEASED	BR	4-15-76	E.G

NOTES:

DETACHED LISTS

AA8100 REV. 8/71

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S - SPARE PARTS
N - NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96787600	A	CLA	A	SPL ECC MOS MEM ARRAY 280 NS	DS	DT223B	04/09/76	04/12/76	

PR

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
	D	96738801	1.00	PC	PWA-ECC MOS ARRAY SWUT	IN			AYM4		N
					NUMBER OF LINE ITEMS = 1						
					HIGHEST FIND NUMBER =						

PROJECT ENGINEER

SCMD

AA 2700-1 REV 7-75

Figure 7-4. DT223-B Error Checking and Correction Array Spare Parts List

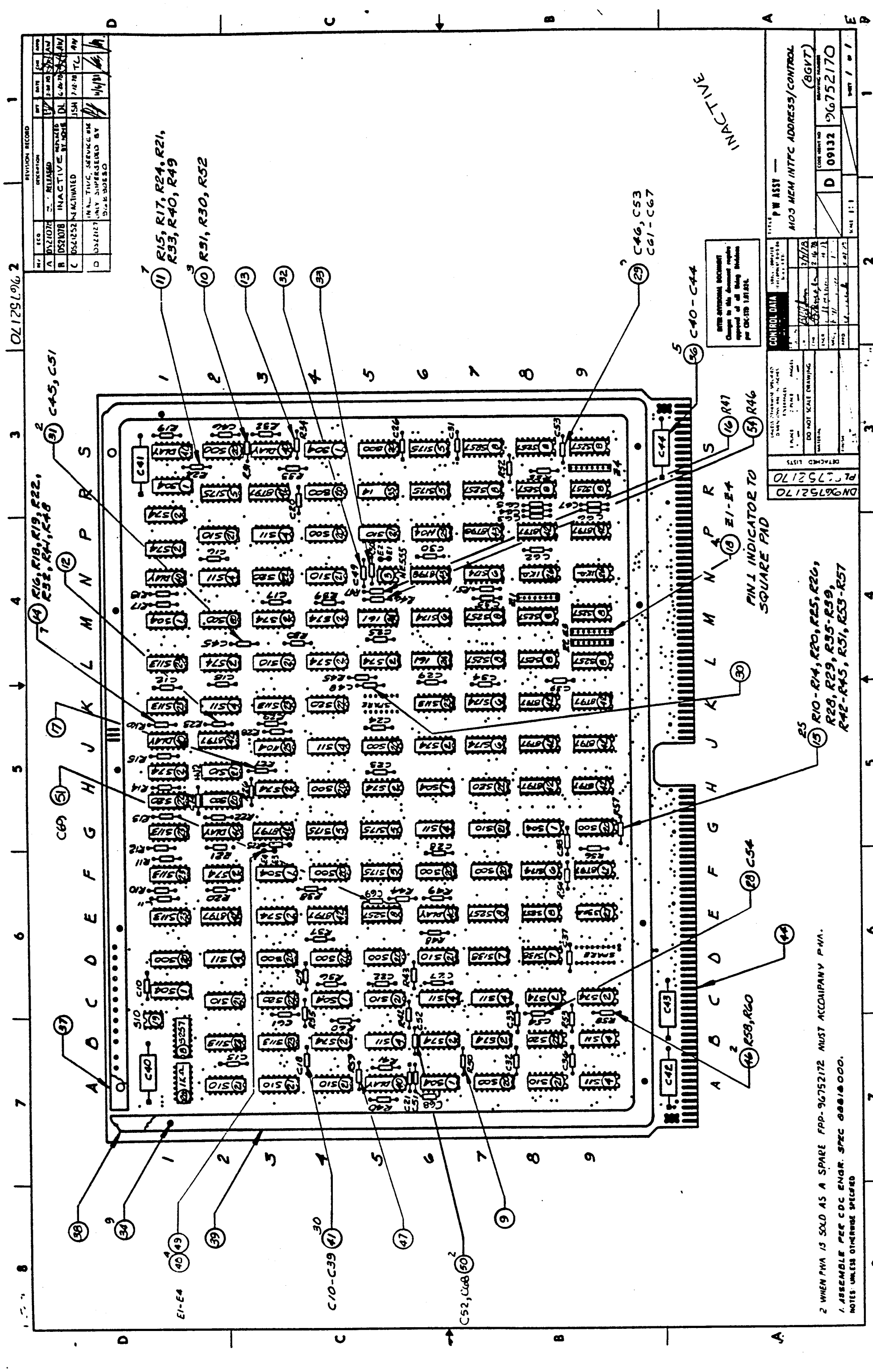

Figure 7-4.1. MOS Memory Interface Address/Control PWA (96752170) (Sheet 1 of 6)

DR				TITLE PW ASSY MOS MEM I/F ADDR/CONT	PREFIX PL	DOCUMENT NO 96752170	REV D
CHKD				FIRST USED ON 86VT		SHEET 1 OF 3	
ENG			DATA SYSTEMS				
MFG	R.W[illegible]	2-17-78					
APPR	[illegible]	3-24-78	CODE IDENT 89132				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS21078	CL. A RELEASED	BR	3-24-78	AW
B	DS21078	INACTIVATE REPLACED BY NONE	DL	6-26-78	AW
C	DS21252	REACTIVATED TL	JSH	7-12-78	AW
D	DS22127	INACTIVE, SERVICE USE ONLY SUPERSEDED BY 96890550		11-6-81	

INACTIVE

NOTES:

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DETACHED LISTS

AA3100 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96752170	D	I	D	PWA-MOS MEM I/F ADDR/CONT 86VT	DSM	CBR 16	03/22/78	022127	10/27/81	2/ 3 MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	S OR N
53	A	15006509	14.00	IN	WIRE-ELEC W/W TEFZEL 30GA WHT	IN			PPP1		N
46	C	24500027	2.00	PC	RES FXD .25W 33 OHMS	IN			PPP4		N
47	C	24500033	1.00	PC	RES FXD .25W 56 OHMS	IN			PPP4		N
10	C	24500039	3.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
9	C	24500040	1.00	PC	RES FXD .25W 110 OHMS	IN			PPP4		N
11	C	24500043	7.00	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
12	C	24500047	1.00	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
13	C	24500051	1.00	PC	RES FXD .25W 330 OHMS	IN			PPP4		N
14	C	24500052	7.00	PC	RES FXD .25W 360 OHMS	IN			PPP4		N
54	C	24500061	1.00	PC	RES FXD .25W 820 OHMS	IN			PPP6		N
15	C	24500063	25.00	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
16	C	24500066	1.00	PC	RES FXD .25W 1300 OHMS	IN			PPP4		N
17	C	24500087	1.00	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
49	C	24501806	2.00	IN	WIRE ELECT SOLID COPPER 24 GA	IN			PPP1		N
52	C	24563700	1.00	IN	INSULATION SLEEVING HIGH TEMP	IN			PPP3		N
18	A	39452200	4.00	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
19	A	39996401	1.00	PC	SWITCH,ROCKER-DUAL,SPST 4POSNS	IN			PPP4		N
26	A	75009901	3.00	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
27	A	75009915	1.00	PC	RESISTOR PAC, 330 OHMS	IN			PPP4		N
28	A	84996715	1.00	PC	CAP,CER 100V 150 PF	IN			PPP4		N
29	A	84996717	9.00	PC	CAP,CER 100V 220 PF	IN			PPP4		N
50	A	84996719	2.00	PC	CAP,CER 100V 330 PF	IN			PPP4		N
31	A	84996721	2.00	PC	CAP,CER 100V 470 PF	IN			PPP4		N
30	A	84996725	1.00	PC	CAP,CER 100V 680 PF	IN			PPP4		N
51	A	84996727	1.00	PC	CAP,CER 100V 820 PF	IN			PPP4		N
32	A	84996739	1.00	PC	CAP,CER 100V 5600 PF	IN			PPP4		N
33	A	84996743	1.00	PC	CAP,CER 100V .01 MF	IN			PPP4		N
34	A	88812400	9.00	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
36	A	88880500	5.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
8	A	88883300	16.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
1	A	88883700	9.00	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
4	A	88884100	11.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP6		N
21	A	88884200	13.00	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN			PPP4		N
20	A	88884500	17.00	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
23	A	88884600	9.00	PC	IC 74S113 SCHOTTKY TTL DUAL	IN			PPP6		N
7	A	88885100	2.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N

INACTIVE

SCMD MFG INFO INTERDIVISIONAL DOCUMENT

Figure 7-4.1. MOS Memory Interface Address/Control PWA (96752170) (Sheet 2 of 6)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER	
96752170	D	I	D	PWA-MOS MEM I/F ADDR/CONT 8GVT	DSM	CBR 18	03/22/78	022127	10/27/81	3/ 3	MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PC RC	
5	A	88885200	6.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
22	A	88885300	6.00	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN			PPP4		N
24	A	88885800	2.00	PC	IC 74161 TTL 4-BIT BINARY CNTR	IN			PPP4		N
25	A	88886600	2.00	PC	IC 74H04 TTL HEX INVERTER	IN			PPP4		N
48	A	88889200	4.00	PC	SOCKET-SPR,MINI .017-.019 PIN	IN			PPP4		N
35	A	88896100	1.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
37	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
38	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
39	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
40	A	88897300	7.00	PC	DELAY LINE-100 NSEC	IN			PPP4		N
41	A	88897800	30.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
42	A	88918800	14.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
43	A	88920900	2.00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
2	A	88923000	18.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
6	A	88923100	5.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
3	A	88923200	1.00	PC	IC NE555 INTEGRATED TIMER	IN			PPP4		N
45	C	96752171	REF	PC	LOGIC-MOS MEM I/F ADDR 8GVT	IN			RFE4		N
44	D	96754582	1.00	PC	PWB-MOS MEM I/F ADDR/CONT	IN			PPP4		N

NUMBER OF LINE ITEMS = 54
HIGHEST FIND NUMBER = 54

SCMD MFG INFO INTERDIVISIONAL DOCUMENT

DRN	[illegible]	2/10/78	DATA SYSTEMS LAJOLLA DIVISION
CHKD	[illegible]	2-16-78	
ENG	[illegible]	3-20-78	
MFG	R. Wilkinson	2.17.78	CODE IDENT 09132
APPR	[illegible]	3-24-78	

TITLE PW ASSY - MOS MEM I/F ADDR/CONT

FIRST USED ON 8GVT

PREFIX DN DOCUMENT NO. 96752170 REV. D

SHEET 1 OF 6

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS21078	CL A RELEASED	BL	3-29-78	AW
B	DS21078	INACTIVATED SUPERSEDED BY NONE	DL	6-26-78	AW
C	DS21252	REACTIVATED	JSH	7-12-78	AW
D	DS 22127	INACTIVE, SERVICE USE ONLY SUPERSEDED BY 96890550	BY	11-6-81	[illegible]

INACTIVE

NOTES

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DETACHED LIST

Figure 7-4.1. MOS Memory Interface Address/Control PWA (96752170) (Sheet 3 of 6)

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA 92037	CODE IDENT 09132	SHEET 2	DN	DOCUMENT NO 96752170	REV D

1. CUT CLAD AS FOLLOWS:

NON-COMPONENT SIDE
- A. BETWEEN D8-6 & F8-1 AND BETWEEN D8-6 & D7-6 (SEE SH 3)
- B. BETWEEN L5-10 & L5-13 AND BETWEEN L5-10 & K3-12 (SEE SH 4)

COMPONENT SIDE
- C. BETWEEN L5-10 & R45 (SEE SH 5)
- D. BETWEEEN A5-8 & FEEDTHRU "D" (SEE SH 6)

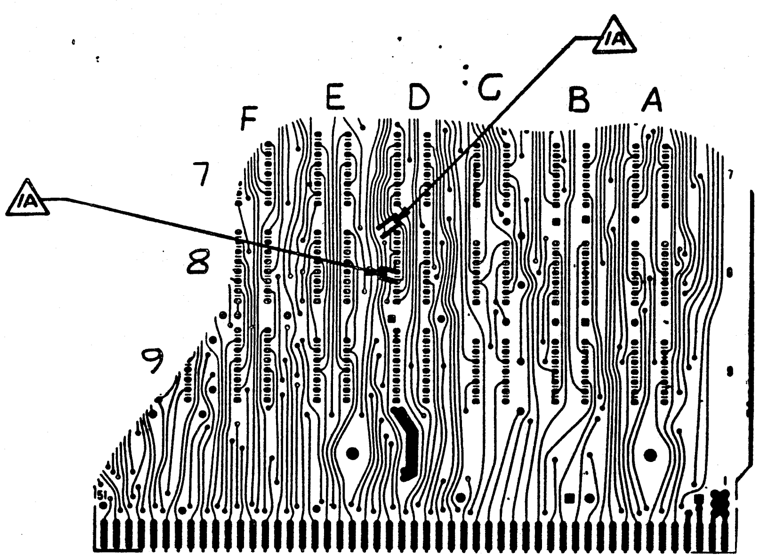
2. ADD WIRE (F/N 53) AS FOLLOWS: COMPONENT SIDE ONLY

- A. D8-6 TO E8-1 (SEE SH 6)
- B. D7-6 TO F8-1 (SEE SH 6)
- C. L5-10 TO K2-5 (SEE SH5)
- D. L5-13 TO FEEDTHRU "A" (SEE SH5)
- E. L5-1 TO R45 (SEE SH5)
- F. A5-5 TO FEEDTHRU "B" (SEE SH 6)

3. ADD FOLLOWING COMPONENTS: (SLEEVE ALL LEADS WITH F/N 52)

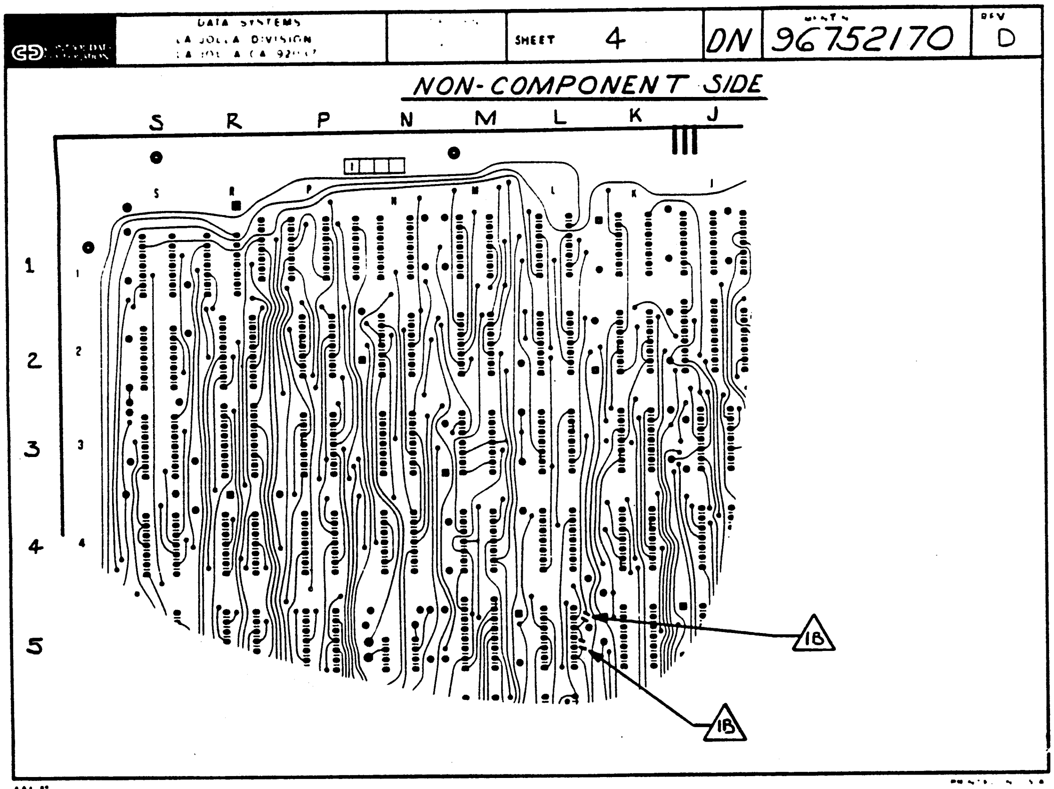
	F/N	REF DESIG	FROM	TO	
A.	50	C68	A6-11	C51 (GND)	(SEE SH 6)
B.	51	C69	E5-1	E5-8 (GND)	(SEE SH 6)

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla Ca 92037	CODE IDENT 09132	SHEET 3	DN	DOCUMENT NO 96752170	REV D



NON-COMPONENT SIDE

Figure 7-4.1. MOS Memory Interface Address/Control PWA (96752170) (Sheet 4 of 6)



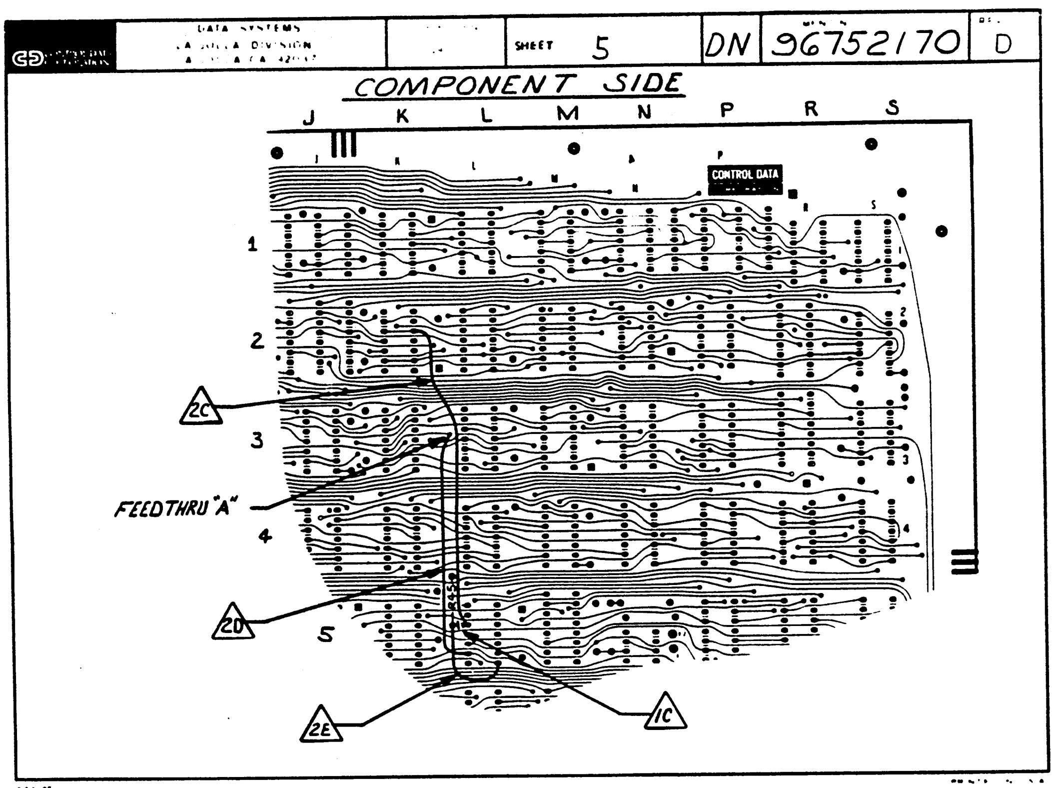


Figure 7-4.1. MOS Memory Interface Address/Control PWA (96752170) (Sheet 5 of 6)

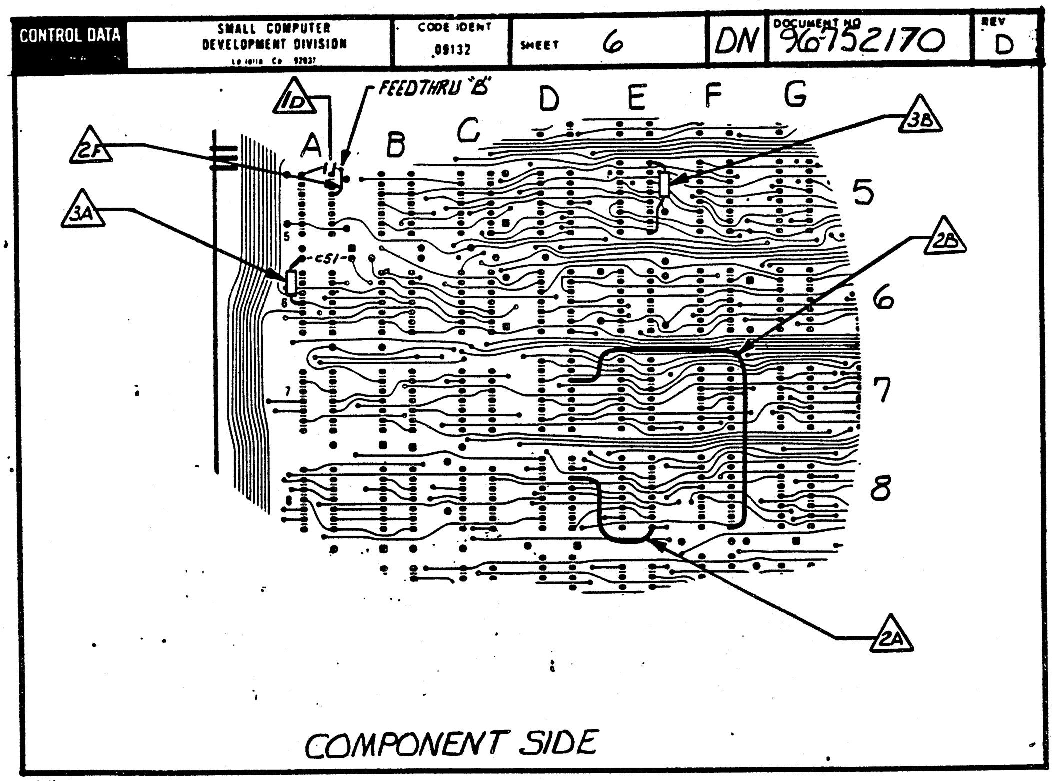


Figure 7-4.1. MOS Memory Interface Address/Control PWA (96752170) (Sheet 6 of 6)

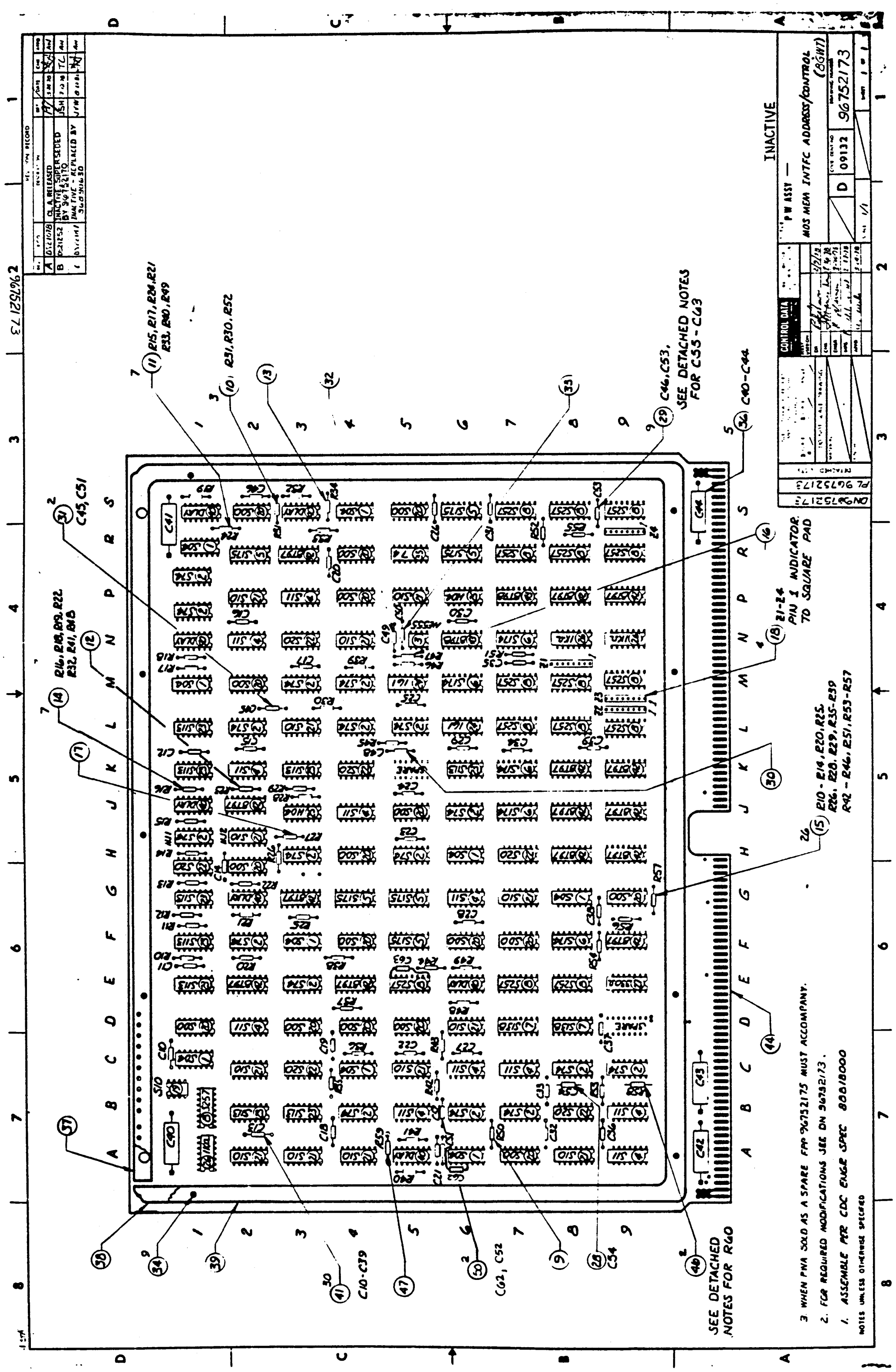


Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 1 of 7)

1-STA

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96752173	C	I	D	PWA-MOS MEM I/F ADDR/CONT 8GWT	DS	CBR 18	03/22/78	022187	08/13/82	MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NO	S OR N
48	A	15006509	24.00	IN	WIRE-ELEC W/W TEFZEL 30GA WHT	IN			PPP1		N
46	C	24500027	2.00	PC	RES FXD .25W 33 OHMS	IN			PPP4		N
47	C	24500033	1.00	PC	RES FXD .25W 56 OHMS	IN			PPP4		N
10	C	24500039	3.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
9	C	24500040	1.00	PC	RES FXD .25W 110 OHMS	IN			PPP4		N
11	C	24500043	7.00	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
12	C	24500047	1.00	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
13	C	24500051	1.00	PC	RES FXD .25W 330 OHMS	IN			PPP4		N
14	C	24500052	7.00	PC	RES FXD .25W 360 OHMS	IN			PPP4		N
15	C	24500063	26.00	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
16	C	24500066	1.00	PC	RES FXD .25W 1300 OHMS	IN			PPP4		N
17	C	24500087	1.00	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
49	C	24563700	12.00	IN	INSULATION SLEEVING HIGH TEMP	IN			PPP3		N
18	A	39452200	4.00	PC	RES NETWORK-VOLTAGE DIVIDR-SIF	IN			PPP4		N
19	A	39996401	1.00	PC	SWITCH,ROCKER-DUAL,SPST 4PUSNS	IN			PPP4		N
26	A	75009901	3.00	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
27	A	75009915	1.00	PC	RESISTOR PAC, 330 OHMS	IN			PPP4		N
28	A	84996715	1.00	PC	CAP,CER 100V 150 PF	IN			PPP4		N
29	A	84996717	9.00	PC	CAP,CER 100V 220 PF	IN			PPP4		N
50	A	84996719	2.00	PC	CAP,CER 100V 330 PF	IN			PPP4		N
31	A	84996721	2.00	PC	CAP,CER 100V 470 PF	IN			PPP4		N
30	A	84996725	1.00	PC	CAP,CER 100V 680 PF	IN			PPP4		N
51	A	84996727	1.00	PC	CAP,CER 100V 820 PF	IN			PPP4		N
32	A	84996739	1.00	PC	CAP,CER 100V 5600 PF	IN			PPP4		N
33	A	84996743	1.00	PC	CAP,CER 100V .01 MF	IN			PPP4		N
34	A	88812400	9.00	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
36	A	88880500	5.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
8	A	88883300	16.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
1	A	88883700	9.00	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
4	A	88884100	11.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP4		N
21	A	88884200	13.00	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN			PPP4		N
20	A	88884500	17.00	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
23	A	88884600	9.00	PC	IC 74S113 SCHOTTKY TTL DUAL	IN			PPP4		N
7	A	88885100	2.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
5	A	88885200	6.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
22	A	88885300	6.00	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN			PPP4		N

SCMD MFG INFO

—INACTIVE—

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96752173	C	I	D	PWA-MOS MEM I/F ADDR/CONT 8GWT	DS	CBR 18	03/22/78	022187	08/13/82	MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NO	S OR N
24	A	88885800	2.00	PC	IC 74161 TTL 4-BIT BINARY CNTR	IN			PPP4		N
25	A	88886600	2.00	PC	IC 74H04 TTL HEX INVERTER	IN			PPP4		N
35	A	88896100	1.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
37	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
38	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
39	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
40	A	88897300	7.00	PC	DELAY LINE-100 NSEC	IN			PPP4		N
41	A	88897800	30.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
42	A	88918800	14.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
43	A	88920900	2.00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
2	A	88923000	18.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
6	A	88923100	5.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
3	A	88923200	1.00	PC	IC NE555 INTEGRATED TIMER	IN			PPP4		N
45	C	96752174	REF	PC	LOGIC-MOS MEM I/F ADDR 8GWT	IN			RFE4		N
44	D	96753834	1.00	PC	PWR-MOS MEM ADDRESS	IN			PPP4		N
					NUMBER OF LINE ITEMS = 51						
					HIGHEST FIND NUMBER = 51						

SCMD MFG INFO

—INACTIVE—

Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 2 of 7)

DWN	[illegible]	2/10/78	DATA SYSTEMS LA JOLLA DIVISION	TITLE PW ASSY-MOS MEM I/F ADDR/CONT	PREFIX DN	DOCUMENT NO. 96752173	REV. C
CHKD	[illegible]	2-16-78	CODE IDENT 09132	FIRST USED ON 8GWT		SHEET	
ENG	[illegible]	[illegible]					
MFG	R. Wilkinson	2-17-78					
APPR	[illegible]	3-24-78					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS21078	~ 1. RELEASED	[illegible]	3-24-78	AW
B	DS21252	INACTIVE, SUPERSEDED BY 96752170	JSH	7-12-78	AW
C	DS22187	INACTIVE REPLACED BY 96890630	J.V.W.	8-20-82	AW

INACTIVE

NOTES

DETACHED LISTS

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA 92037	CODE IDENT 09132	SHEET	DN	DOCUMENT NO 96752173	REV A

1. CUT CLAD AS FOLLOWS:

COMPONENT SIDE

- A. BETWEEN C4-11 & I/O PIN 17 (SEE SH4)
- B. BETWEEN D6-9 & C3-13 (SEE SH5)
- C. BETWEEN H3-8 & J5-12 (SEE SH5)
- D. BETWEEN L5-10 & R45 (SEE SH10)
- E. BETWEEN N1-4 & M1-5 (SEE SH 4)
- F. BETWEEN A5-8 & FEEDTHRU "C" (SEE SH 7)

NON-COMPONENT SIDE

- F. BETWEEN C3-13 & D6-9 (SEE SH6)
- G. BETWEEN C6-10 & C6-11 (SEE SH6)
- H. BETWEEN D8-6 & D7-6 AND BETWEEN D8-6 & F8-1 (SEE SH8)
- J. BETWEEN L5-10 & L5-13 AND BETWEEN L5-10 & K3-12 (SEE SH9)

2. ADD WIRE (F/N 48) AS FOLLOWS:

COMPONENT SIDE ONLY

- A. C6-11 TO C6-1 (SEE SH 5)
- B. D7-6 TO F8-1 (SEE SH 7)
- C. D8-6 TO E8-1 (SEE SH 7)
- D. J3-11 TO J3-2 (SEE SH 5)
- E. J3-10 TO J5-12 (SEE SH 5)
- F. L5-10 TO K2-5 (SEE SH 10)
- G. L5-13 TO FEEDTHRU "B" (SEE SH 10)
- H. L5-1 TO R45 (SEE SH 10)
- J. N1-5 TO M1-5 (SEE SH4)
- K. A5-5 TO FEEDTHRU "C" (SEE SH 7)

Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 3 of 7)

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA 92037	CODE IDENT 09132	SHEET	DN	DOCUMENT NO 96752173	REV A

3 ADD FOLLOWING COMPONENTS: (SLEEVE ALL LEADS WITH F/N 49)

	F/N	REF DESIG	FROM	TO	
A.	46	R60	FEEDTHRU "A"	C4-11	SEE SH 4
B.	29	C55	C4-7	C4-11	SEE SH 4
C.	29	C56	P8-2	P8-8	SEE SH 4
D.	29	C58	P8-6	P8-8	SEE SH 4
E.	29	C57	P8-4	P8-8	SEE SH 4
F.	29	C59	P8-10	P9-8	SEE SH 4
G.	29	C60	P8-12	P9-8	SEE SH 4
H.	29	C61	P8-14	P9-8	SEE SH 4
J.	50	C62	A6-11	A6-7 (GND)	SEE SH 7
K.	51	C63	E5-1	E5-8 (GND)	SEE SH 7

CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION	CODE IDENT 09132	SHEET	DN	DOCUMENT NO 96752173	REV A

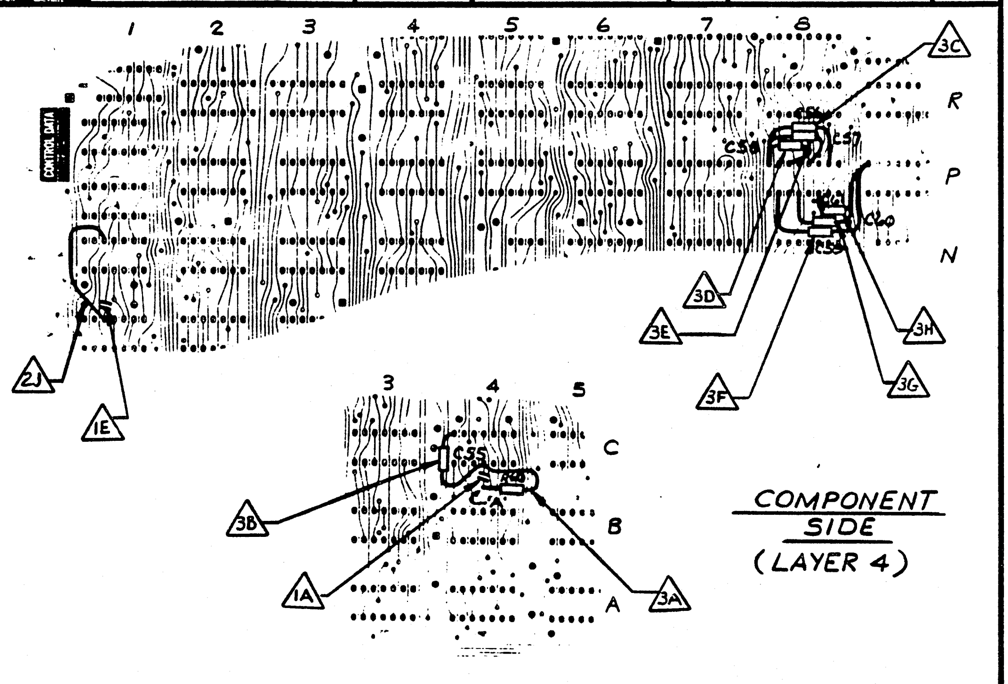
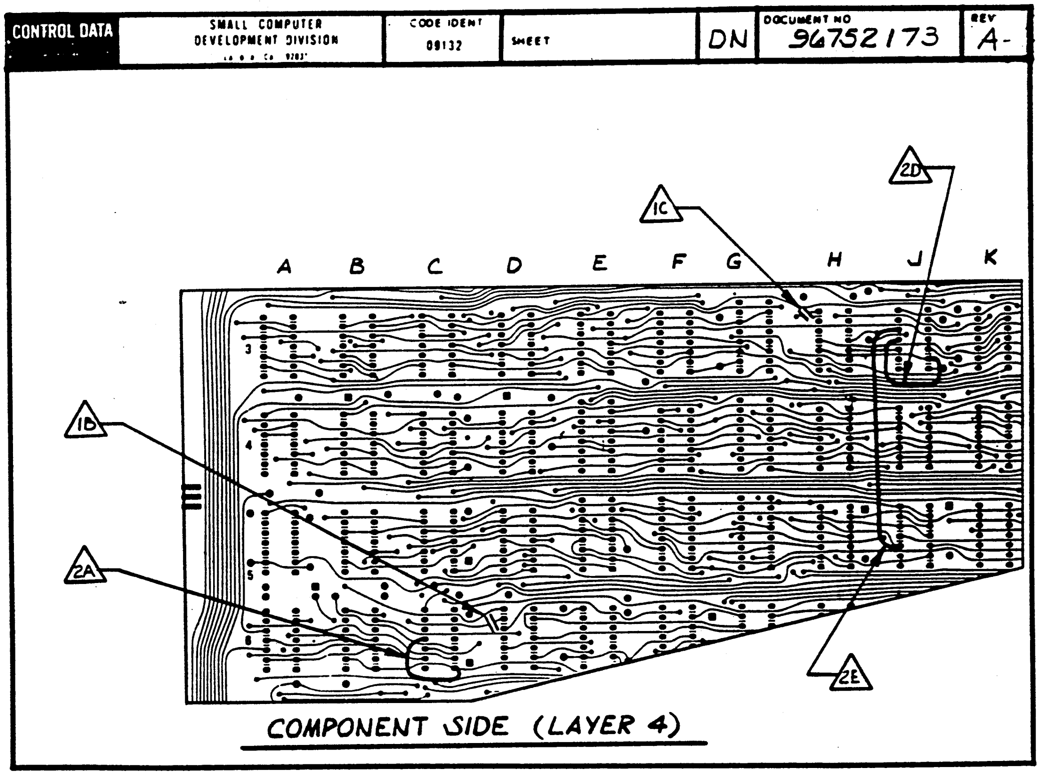


Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 4 of 7)



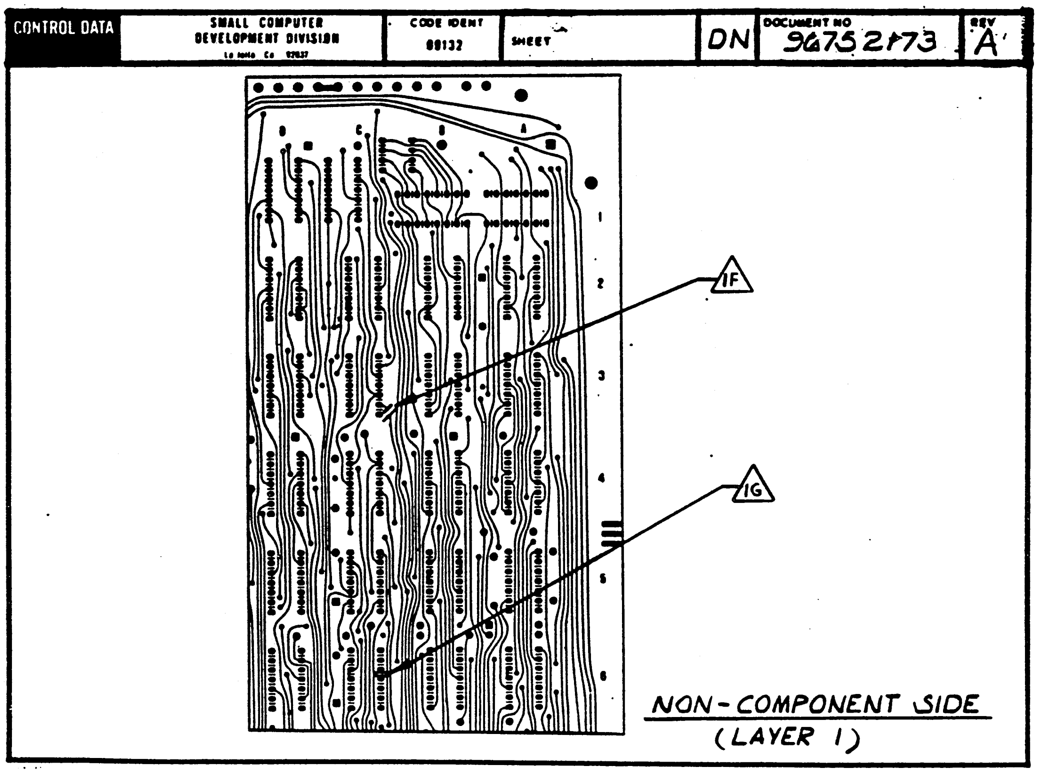
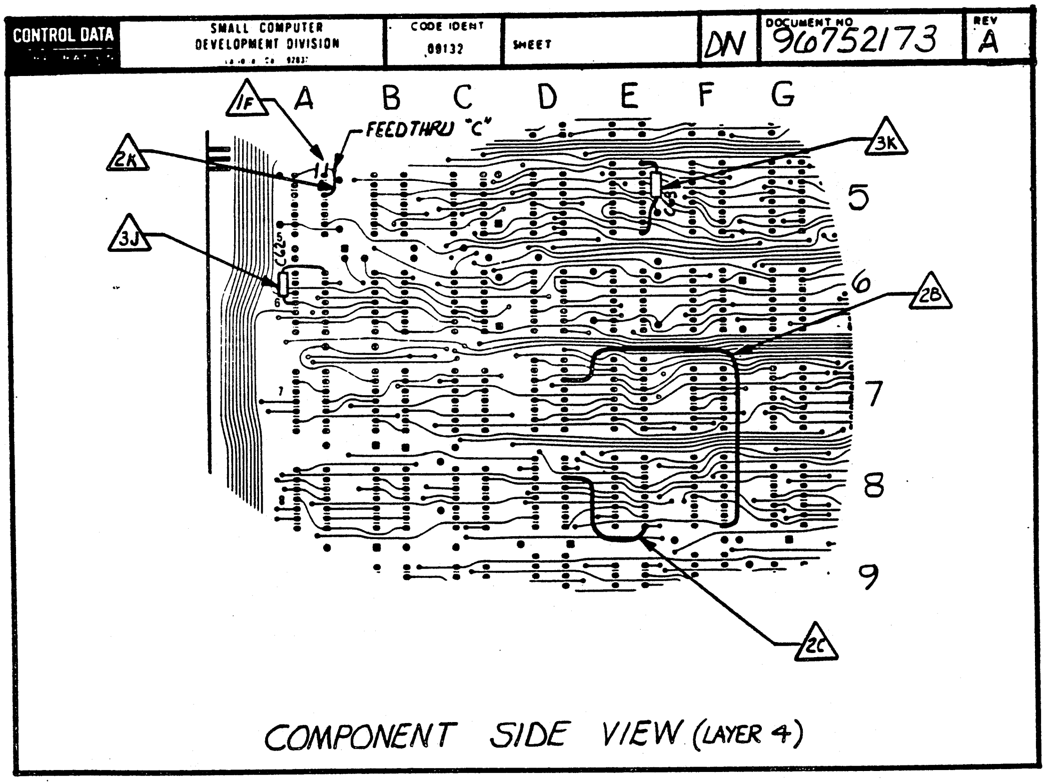


Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 5 of 7)



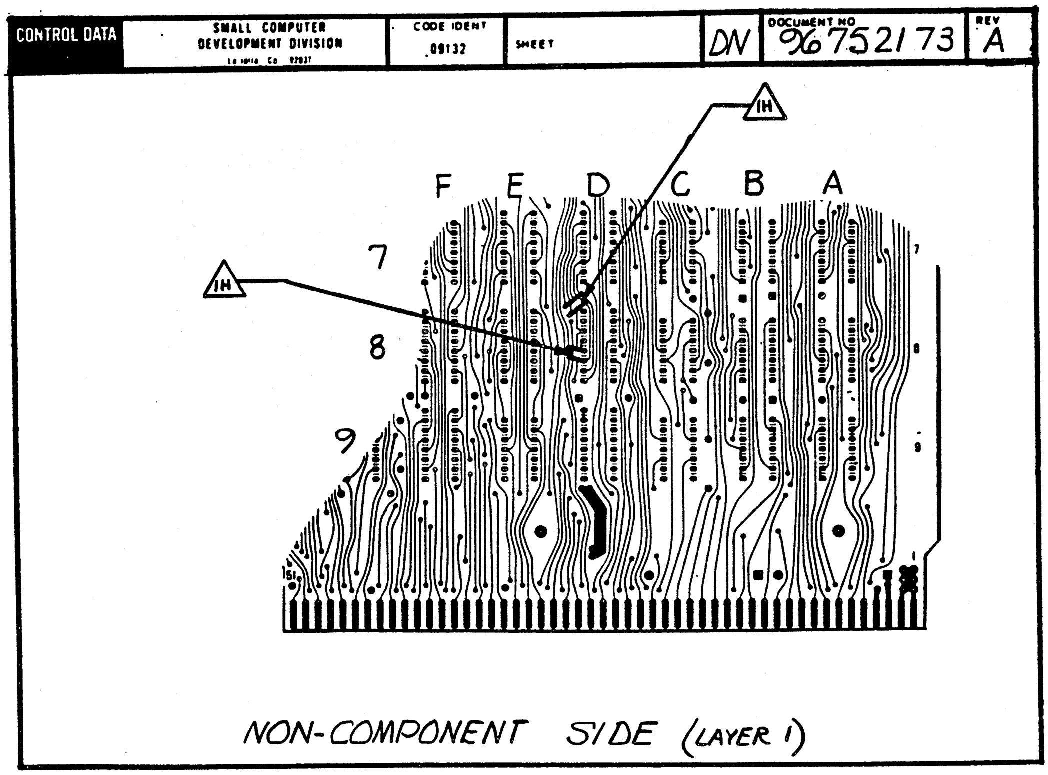
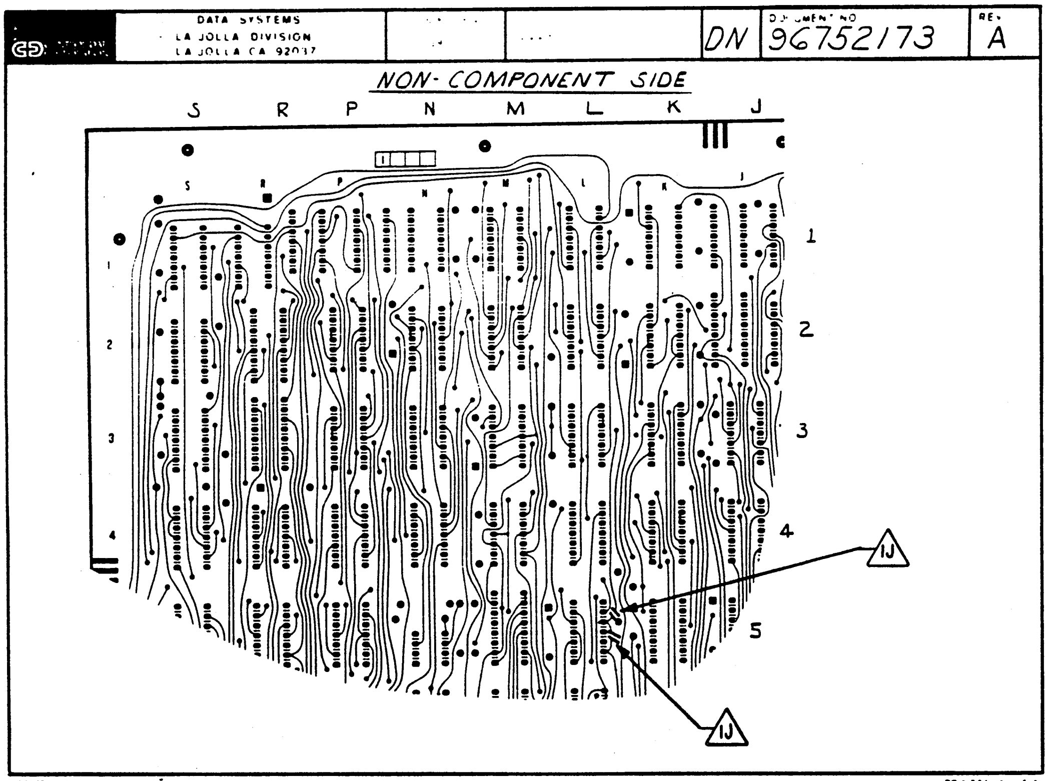


Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 6 of 7)



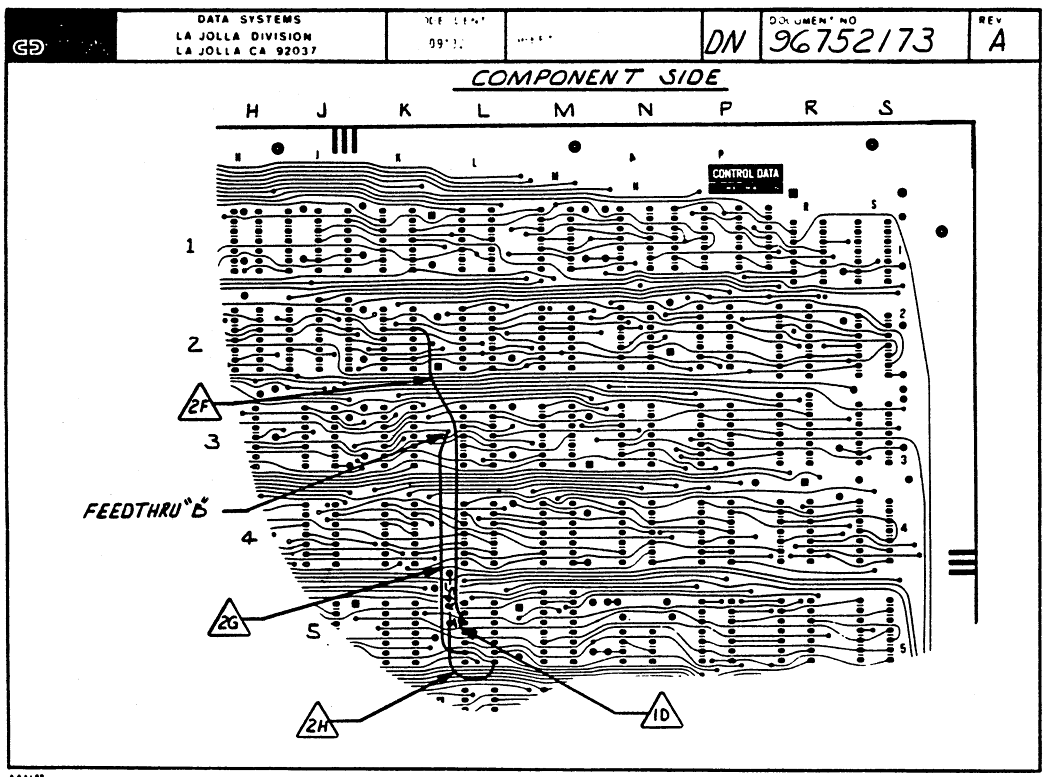


Figure 7-5. MOS Memory Interface Address/Control PWA (96752173) (Sheet 7 of 7)

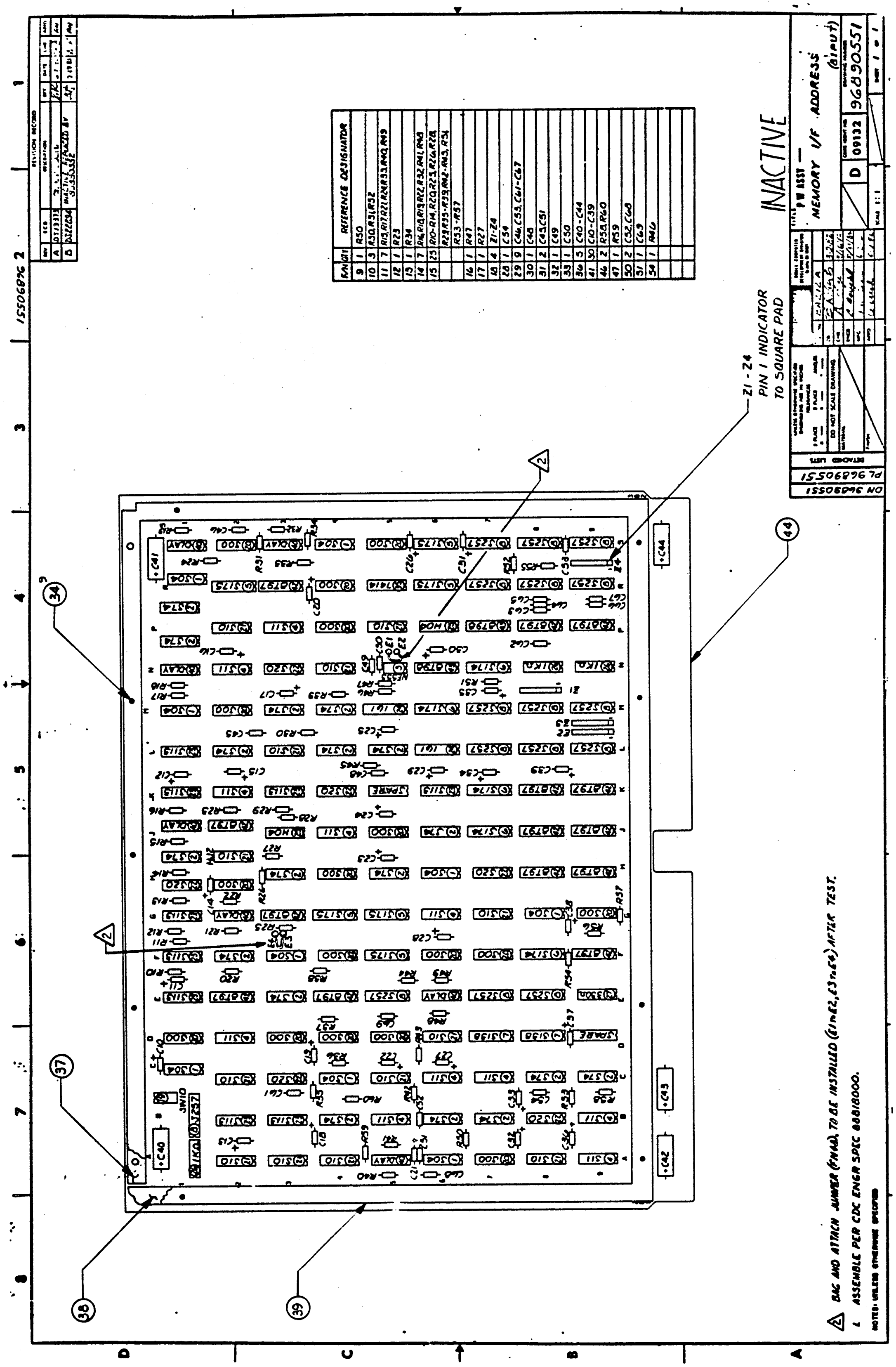


Figure 7-6. MOS Memory Interface Address/Control PWA (96890551) (Sheet 1 of 4)

CONTROL DATA CORPORATION — ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96890551	B	I	D	PWA-MEMORY I/F ADDRESS 81PUT	DSM	CBR 18	06/02/82	022294	07/20/83	

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PW NC	S OR N
46	C	24500027	2.00	PC	RES FXD .25W 33 OHMS	IN			PPP4		N
47	C	24500033	1.00	PC	RES FXD .25W 56 OHMS	IN			PPP4		N
10	C	24500039	3.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
9	C	24500040	1.00	PC	RES FXD .25W 110 OHMS	IN			PPP4		N
11	C	24500043	7.00	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
12	C	24500047	1.00	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
13	C	24500051	1.00	PC	RES FXD .25W 330 OHMS	IN			PPP4		N
14	C	24500052	7.00	PC	RES FXD .25W 360 OHMS	IN			PPP6		N
54	C	24500061	1.00	PC	RES FXD .25W 820 OHMS	IN			PPP4		N
15	C	24500063	25.00	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
16	C	24500066	1.00	PC	RES FXD .25W 1300 OHMS	IN			PPP4		N
17	C	24500087	1.00	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
18	A	39452200	4.00	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
19	A	39996401	1.00	PC	SWITCH,ROCKER-DUAL,SPST 4POSNS	IN			PPP4		N
55	C	52629949	8.00	IN	WIRE ELEC 30 GA WHITE	IN			PPP1		N
26	A	75009901	3.00	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
27	A	75009915	1.00	PC	RESISTOR PAC, 330 OHMS	IN			PPP4		N
28	A	84996715	1.00	PC	CAP,CER 100V 150 PF	IN			PPP4		N
29	A	84996717	9.00	PC	CAP,CER 100V 220 PF	IN			PPP4		N
50	A	84996719	2.00	PC	CAP,CER 100V 330 PF	IN			PPP4		N
31	A	84996721	2.00	PC	CAP,CER 100V 470 PF	IN			PPP4		N
30	A	84996725	1.00	PC	CAP,CER 100V 680 PF	IN			PPP4		N
51	A	84996727	1.00	PC	CAP,CER 100V 820 PF	IN			PPP4		N
32	A	84996739	1.00	PC	CAP,CER 100V 5600 PF	IN			PPP4		N
33	A	84996743	1.00	PC	CAP,CER 100V .01 MF	IN			PPP4		N
36	A	88880500	5.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
8	A	88883300	16.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
1	A	88883700	9.00	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
4	A	88884100	11.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP4		N
21	A	88884200	13.00	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN			PPP4		N
20	A	88884500	17.00	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
23	A	88884600	9.00	PC	IC 74S113 SCHOTTKY TTL DUAL	IN			PPP4		N
7	A	88885100	2.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
5	A	88885200	6.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
22	A	88885300	6.00	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN			PPP4		N
24	A	88885800	2.00	PC	IC 74161 TTL 4-BIT BINARY CNTR	IN			PPP4		N

INACTIVE

CONTROL DATA CORPORATION — ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96890551	B	I	D	PWA-MEMORY I/F ADDRESS 81PUT	DSM	CBR 19	06/02/82	022294	07/20/83	

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PW NC	S OR N
25	A	88886600	2.00	PC	IC 74H04 TTL HEX INVERTER	IN			PPP4		N
35	A	88896100	1.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
37	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
38	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
39	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
40	A	88897300	7.00	PC	DELAY LINE-100 NSEC	IN			PPP4		N
41	A	88897800	30.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
42	A	88918800	14.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
43	A	88920900	2.00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
2	A	88923000	18.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
6	A	88923100	5.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
3	A	88923200	1.00	PC	IC NE555 INTEGRATED TIMER	IN			PPP4		N
48	A	88945400	2.00	PC	JUMPER 24AWG TEF INSULATED .50	IN			AYE4		N
34	A	92030018	9.00	PC	EYELET	IN					N
44	D	96890250	1.00	PC	PWB-MEMORY INTERFACE ADDRESS	IN					N
45	C	96890951	REF	PC	LOGIC DIAG MEM I/F ADDR 81PUT	IN					N

NUMBER OF LINE ITEMS = 52
HIGHEST FIND NUMBER = 55

INACTIVE

Figure 7-6. MOS Memory Interface Address/Control PWA (96890551) (Sheet 2 of 4)

DWN	B. Roberts	3-9-82	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA. 92037	TITLE PW ASSY- MEMORY I/F ADDRESS	PREFIX DN	DOCUMENT NO. 96890551	REV. B
CHKD	R. Faas	3-16-82					
ENG		5-21-82		FIRST USED ON			
MFG	U McDrew	6-2-82	CODE IDENT 89132				
APPR		6-7-82					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	D319373	CL. A. RELEASED	BR	6-7-82		AW
B	D322894	INA RCPL'D BY 96890552		7-29-83		AW

INACTIVE

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

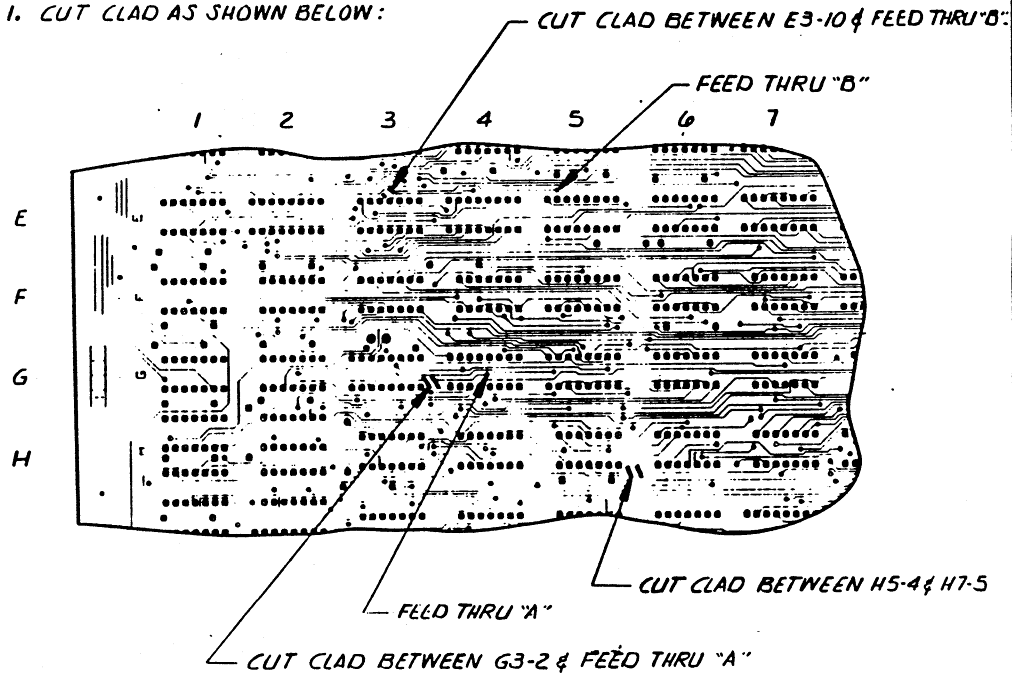
AA6030

NOTES:

DETACHED LISTS

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 89132		DN	DOCUMENT NO 96890551	REV A

1. CUT CLAD AS SHOWN BELOW:



NON-COMPONENT SIDE

Figure 7-6. MOS Memory Interface Address/Control PWA (96890551) (Sheet 3 of 4)

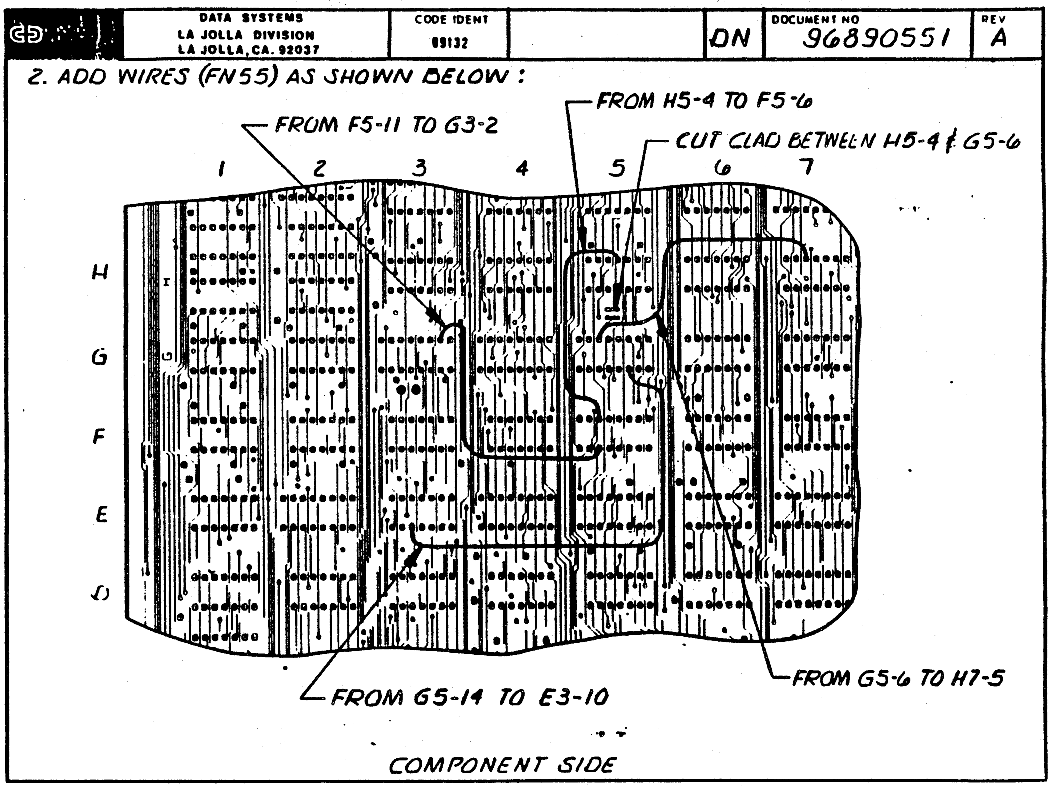


Figure 7-6. MOS Memory Interface Address/Control PWA (96890551) (Sheet 4 of 4)

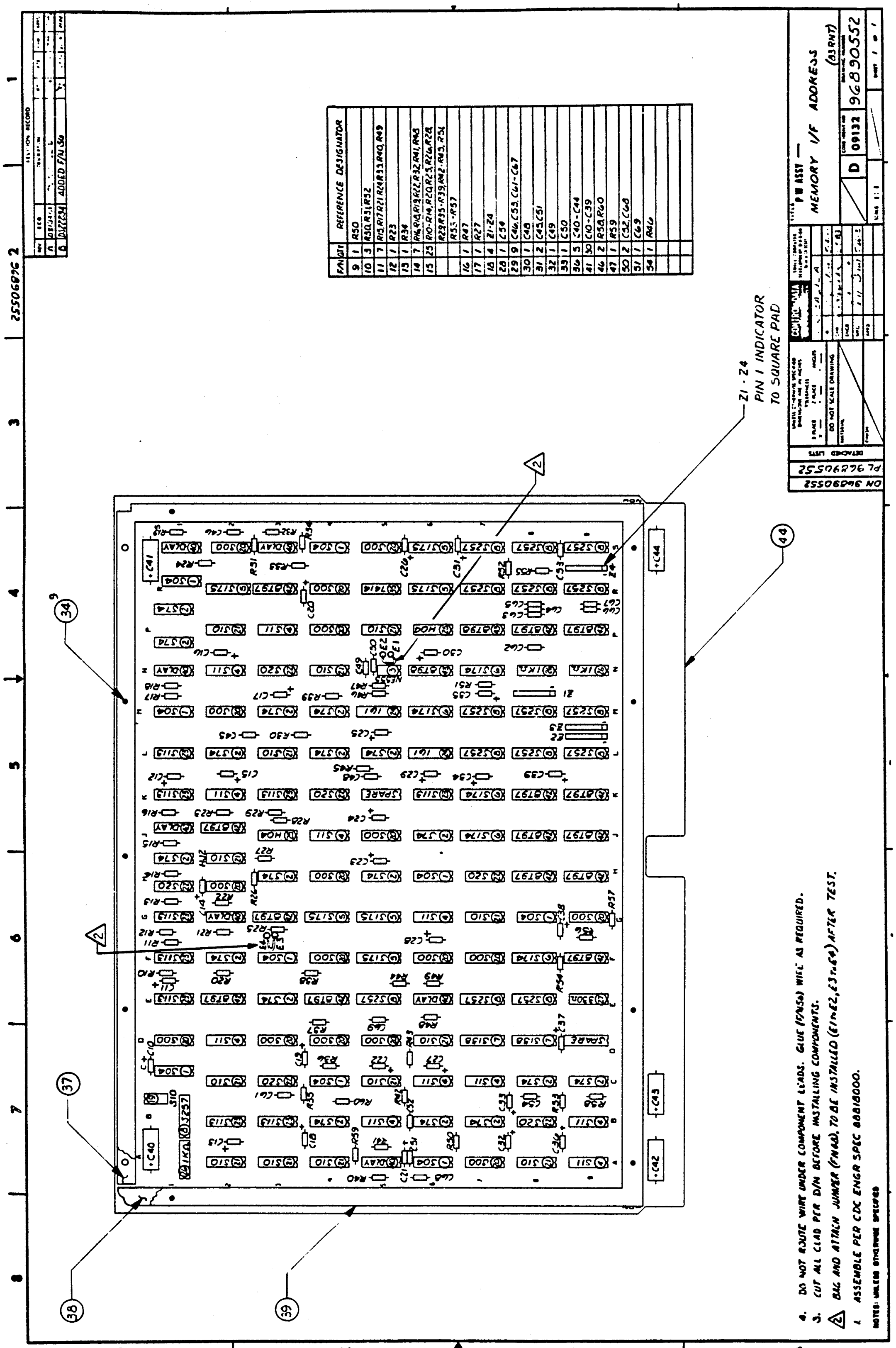


Figure 7-6.1. MOS Memory Interface Address PWA (96890552) (Sheet 1 of 5)

CONTROL DATA CORPORATION ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER	
96890552	B	A	D	PWA-MEMORY I/F ADDRESS 83RNT	DS	CYB 18	05/20/83	022294	07/22/83		MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	S OR N
46	C	24500027	2.00	PC	RES FXD .25W 33 OHMS	IN			PPP4		N
47	C	24500033	1.00	PC	RES FXD .25W 56 OHMS	IN			PPP4		N
10	C	24500039	3.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
9	C	24500040	1.00	PC	RES FXD .25W 110 OHMS	IN			PPP4		N
11	C	24500043	7.00	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
12	C	24500047	1.00	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
13	C	24500051	1.00	PC	RES FXD .25W 330 OHMS	IN			PPP4		N
14	C	24500052	7.00	PC	RES FXD .25W 360 OHMS	IN			PPP4		N
54	C	24500061	1.00	PC	RES FXD .25W 820 OHMS	IN			PPP4		N
15	C	24500063	25.00	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
16	C	24500066	1.00	PC	RES FXD .25W 1300 OHMS	IN			PPP4		N
17	C	24500087	1.00	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
18	A	39452200	4.00	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
19	A	39996401	1.00	PC	SWITCH,ROCKER-DUAL,SPST 4POSNS	IN			PPP4		N
55	C	52629949	8.00	IN	WIRE ELEC 30 GA WHITE	IN			PPP1		N
56	A	62019900	0.01	OZ	EPOXY, 2 PART 5 MIN(CLEAR)TUBE	IN	022294	072283	PFE4		N
26	A	75009901	3.00	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
27	A	75009915	1.00	PC	RESISTOR PAC, 330 OHMS	IN			PPP4		N
28	A	84996715	1.00	PC	CAP,CER 100V 150 PF	IN			PPP4		N
29	A	84996717	9.00	PC	CAP,CER 100V 220 PF	IN			PPP4		N
50	A	84996719	2.00	PC	CAP,CER 100V 330 PF	IN			PPP4		N
31	A	84996721	2.00	PC	CAP,CER 100V 470 PF	IN			PPP4		N
30	A	84996725	1.00	PC	CAP,CER 100V 680 PF	IN			PPP4		N
51	A	84996727	1.00	PC	CAP,CER 100V 820 PF	IN			PPP4		N
32	A	84996739	1.00	PC	CAP,CER 100V 5600 PF	IN			PPP4		N
33	A	84996743	1.00	PC	CAP,CER 100V .01 MF	IN			PPP4		N
36	A	88880500	5.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
8	A	88883300	16.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
1	A	88883700	9.00	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
4	A	88884100	11.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP4		N
21	A	88884200	13.00	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN			PPP4		N
20	A	88884500	17.00	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
23	A	88884600	9.00	PC	IC 74S113 SCHOTTKY TTL DUAL	IN			PPP4		N
7	A	88885100	2.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
5	A	88885200	6.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
22	A	88885300	6.00	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN			PPP4		N

CONTROL DATA CORPORATION ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER	
96890552	B	A	D	PWA-MEMORY I/F ADDRESS 83RNT	DS	CYB 18	05/20/83	022294	07/22/83		MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	S OR N
24	A	88885800	2.00	PC	IC 74161 TTL 4-BIT BINARY CNTR	IN			PPP4		N
25	A	88886600	2.00	PC	IC 74H04 TTL HEX INVERTER	IN			PPP4		N
35	A	88896100	1.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
37	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
38	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
39	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
40	A	88897300	7.00	PC	DELAY LINE-100 NSEC	IN			PPP4		N
41	A	88897800	30.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
42	A	88918800	14.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
43	A	88920900	2.00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
2	A	88923000	18.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
6	A	88923100	5.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
3	A	88923200	1.00	PC	IC NE555 INTEGRATED TIMER	IN			PPP4		N
48	A	88945400	2.00	PC	JUMPER 24AWG TEF INSULATED .50	IN			AYE4		N
34	A	92030018	9.00	PC	EYELET	IN					N
44	D	96890250	1.00	PC	PWB-MEMORY INTERFACE ADDRESS	IN					N
45	C	96890851	REF	PC	LOGIC DIAG MEM I/F ADDR 81PUT	IN					N

NUMBER OF LINE ITEMS = 53
HIGHEST FIND NUMBER = 56

Figure 7-6.1. MOS Memory Interface Address PWA (96890552) (Sheet 2 of 5)

DWN	[illegible]	5-4-83	DATA SYSTEMS LA JOLLA DIVISION
CHKD	[illegible]	5-5-83	
ENG	[illegible]	5-25-83	
MFG	[illegible]	5-26-83	CODE IDENT 09132
APPR			

TITLE PW ASSY - (83RNT) MEMORY I/F ADDRESS

PREFIX DN | DOCUMENT NO. 96890552 | REV. B

FIRST USED ON BA212-A

SHEET REVISION STATUS

REVISION RECORD

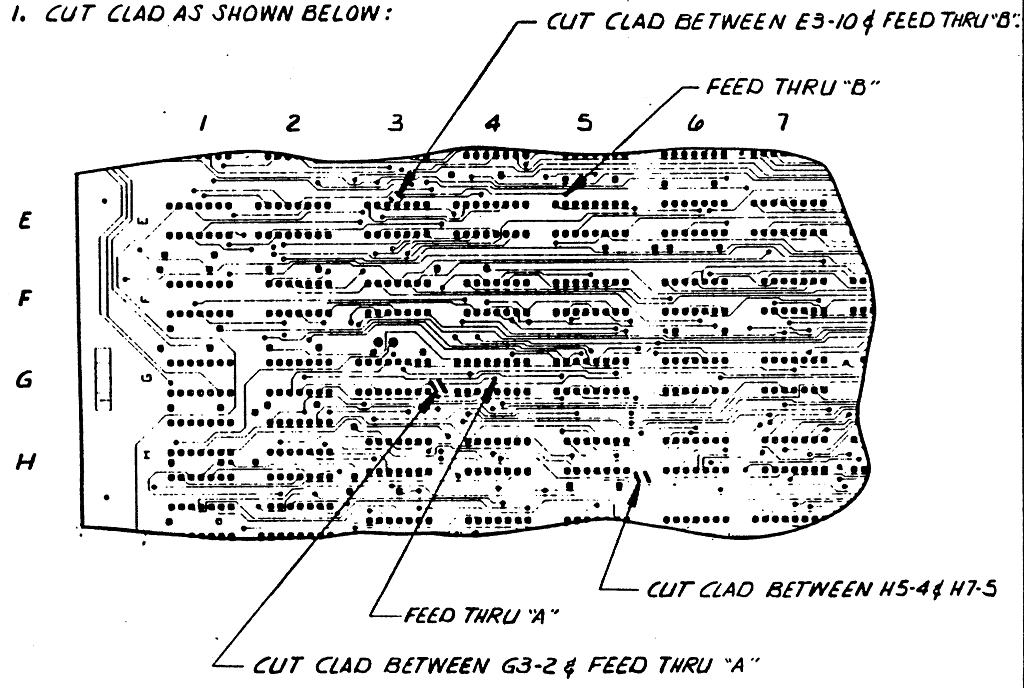
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS19401	CLASS A RELEASE	JVW	5-26-83	[illegible]	Totto

NOTES:

DETACHED LISTS

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037 | CODE IDENT 09132 | DN | DOCUMENT NO 96890552 | REV A

1. CUT CLAD AS SHOWN BELOW:

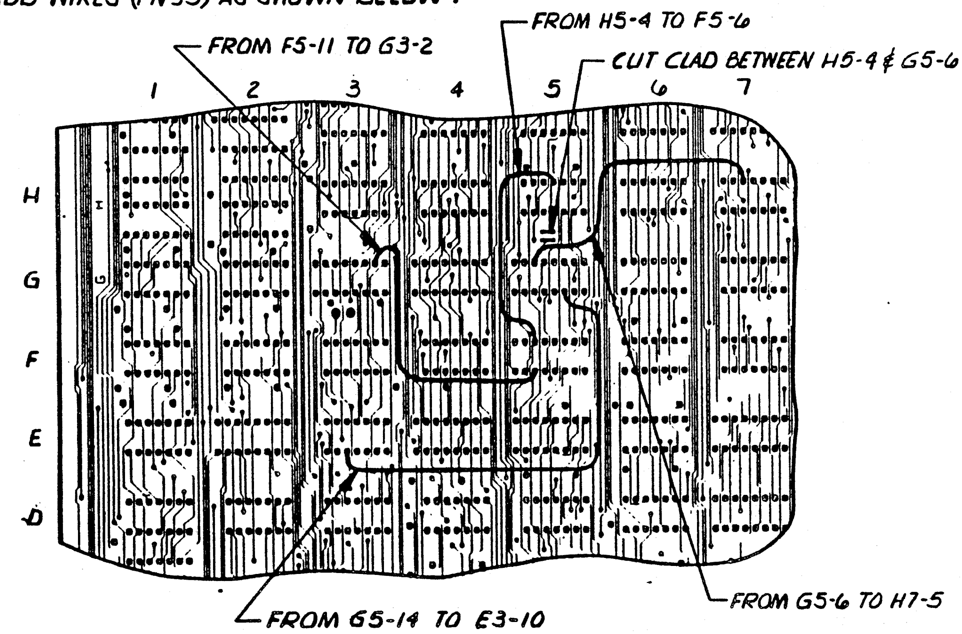


NON - COMPONENT SIDE

Figure 7-6.1. MOS Memory Interface Address PWA (96890552) (Sheet 3 of 5)

		CODE IDENT			DOCUMENT NO	REV
CD	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	89132		DN	96890552	A

2. ADD WIRES (FN55) AS SHOWN BELOW :



COMPONENT SIDE

	CODE IDENT			DOCUMENT NO	REV
CD CONTROL DATA CORPORATION	89132		DN	96890552	A

COMPONENT SIDE

3. ADD WIRE (F/N55) AS SHOWN BELOW.

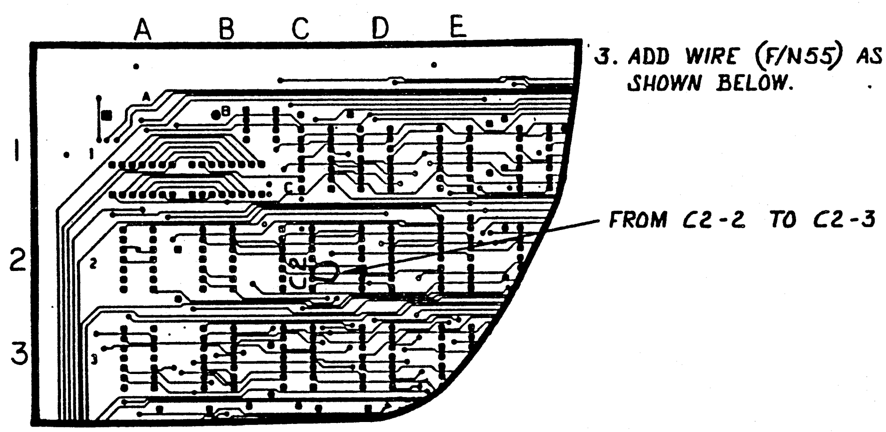


Figure 7-6.1. MOS Memory Interface Address PWA (96890552) (Sheet 4 of 5)

CONTROL DATA CORPORATION	CODE IDENT 89132		DN	DOCUMENT NO 96890552	REV A

COMPONENT SIDE

5. ADD WIRE (F/N55) AS SHOWN BELOW.

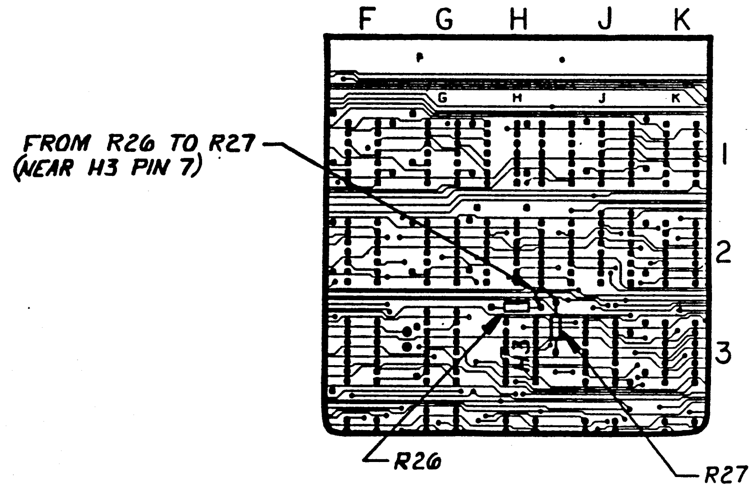


Figure 7-6.1. MOS Memory Interface Address PWA (96890552) (Sheet 5 of 5)

		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS19376	CL. A. RELEASED	BC	6-18-82		AW
B	DS22187	INACTIVE - REPLACED BY NONE	JVW.	8-20-82		AW
C	DS22894	INA REPL'D BY 96890551		7-29-83		AW

NOTES:

1. REWORK PWA 96752173 PER SHEETS 2-4 OF THIS DRAWING.
2. RE-IDENTIFY WITH PART NO. 96890630 & CODE 82RHT PER 88818000.

—INACTIVE—

INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DWN		5/26/82
CHKD		6-2-82
ENG		6-2-82
MFG		6-2-82
APP		6-18-82

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA. 92037

TITLE PWA-MEMORY I/F ADDRESS EARLY VERSION

CODE IDENT 09132 | A | DWG No 96890630

SCALE

	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132			DOCUMENT NO 96890630	REV A

1 CONT'D
REWORK PWA 96752173 AS FOLLOWS:

A. REMOVE EXISTING IC 74S11 AT LOCATION "B5"

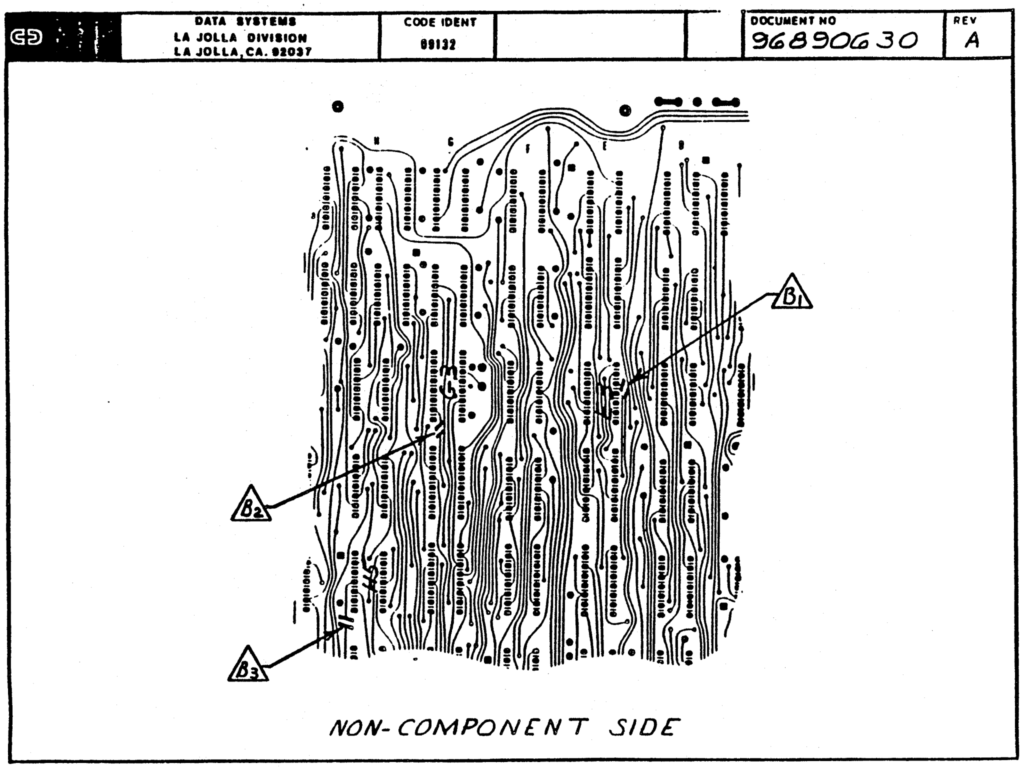
B. CUT THE FOLLOWING CLAD -
NON-COMPONENT SIDE (SEE SH 3)
1. CUT @ E3-10
2. CUT @ G3-2
3. CUT @ H5-4
COMPONENT SIDE (SEE SH 4)
4. CUT @ H5-4
5. CUT BETWEEN R59 AND B5-8
6. CUT BETWEEN B5-5 AND B5-10
7. CUT BETWEEN B5-3 AND B5-11

C. INSTALL NEW IC 74S11 P/N 88884100 (F/N 3) AT LOCATION B5.

D. ADD THE FOLLOWING WIRE (F/N 1) [SEE SH 4]
EPOXY (F/N 2) WIRES TO SURFACE AS REQUIRED

1. G5-14 TO E3-10
2. F5-11 TO G3-2
3. H5-4 TO F5-6
4. G5-6 TO H7-5
5. R59 (LEG) TO B5-8
6. B5-1 TO B5-11
7. B5-10 TO A6-10

Figure 7-7. MOS Memory Interface Address/Control PWA (96890630) (Sheet 1 of 3)



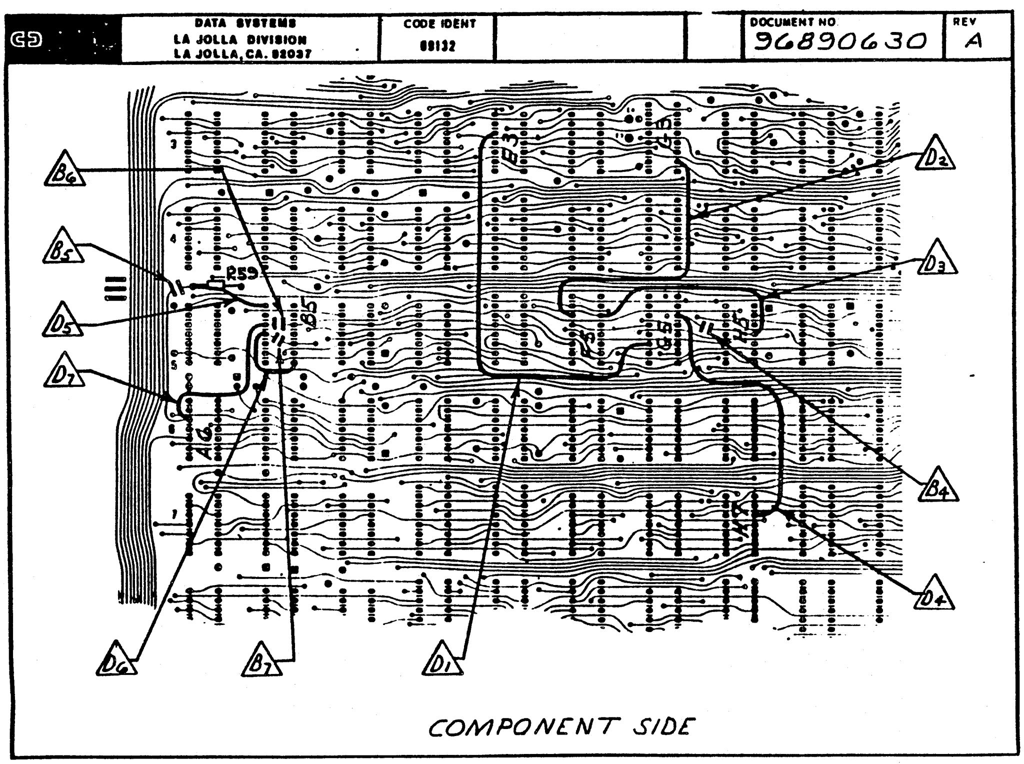


Figure 7-7. MOS Memory Interface Address/Control PWA (96890630) (Sheet 2 of 3)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96890630	C	I	A	PWA-MEM I/F ADDR EARLY VERSION	DSM	CBR 18	06/11/82	022296	07/20/81	

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	S OR N
1	C	11899724	2.00	PC	WIRE,KYNAR,30GA,25IN, 52629946	IN					N
2	A	62019900	0.02	OZ	EPOXY, 2 PART 5 MIN(CLEAR)TURF	IN			REF4		N
3	A	88884100	1.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			OPP4		N
4	D	96752173	1.00	PC	PWA-MOS MEM I/F ADDR/CONT AGWT	IN			AYH4		N
5	C	96890851	REF	PC	LOGIC DIAG MEM I/F ADDR 81PUT	IN					N

NUMBER OF LINE ITEMS = 5
HIGHEST FIND NUMBER = 5

INACTIVE

Figure 7-7. MOS Memory Interface Address/Control PWA (96890630) (Sheet 3 of 3)

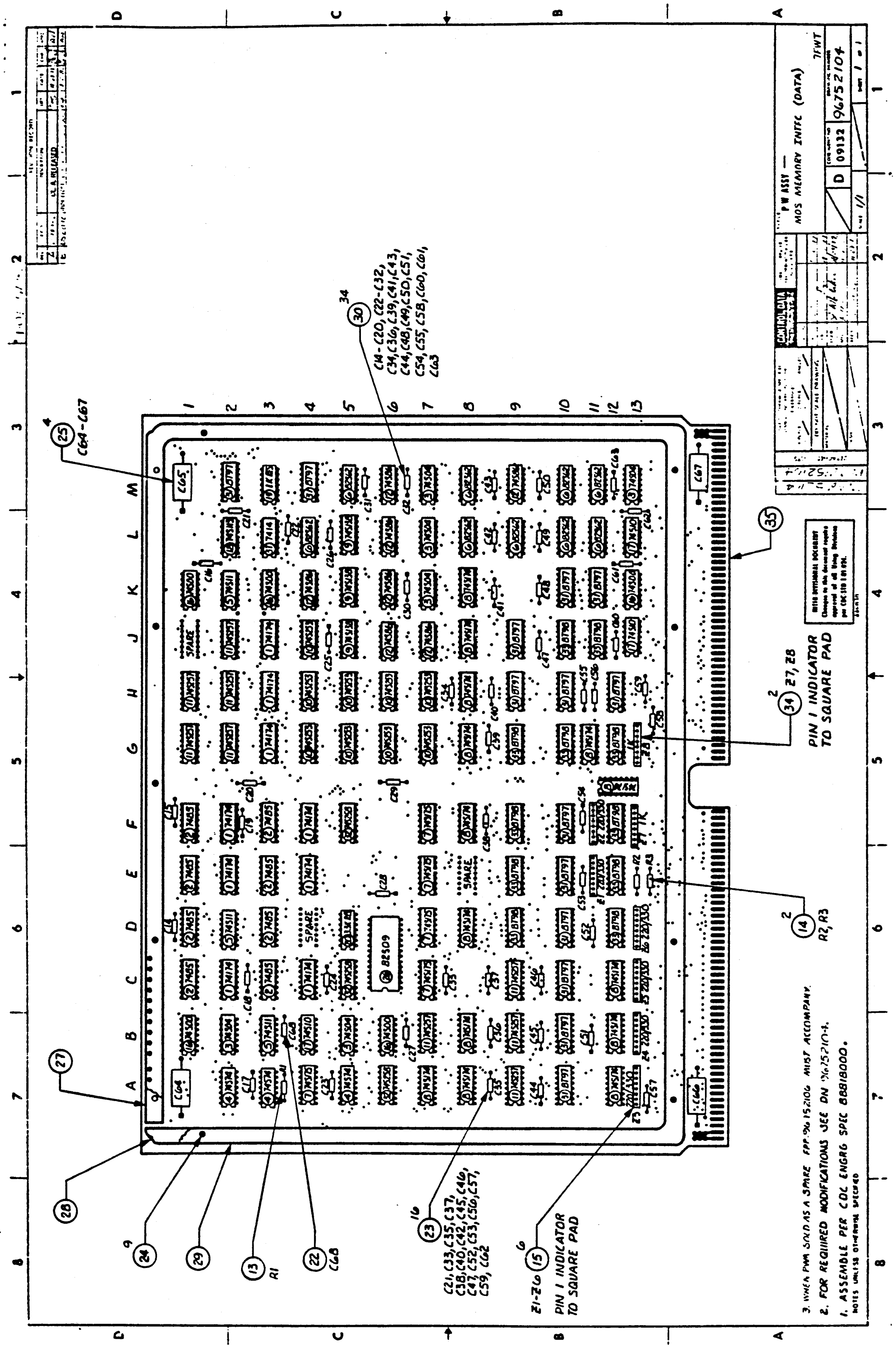


Figure 7-8. MOS Memory Interface Data PWA (96752104) (Sheet 1 of 4)

(CA-CTA)

CONTROL DATA CORPORATION — ASSEMBLY PARTS LIST

Assembly Number	Rev	CL	DW SZ	Assembly Description	Design Source	First Usage	Release Date	Change Ord. Number	Processing Date	Page Number
96752104	B	I	D	PWA-MOS MEM I/F DATA 7FWT	DSM	CBP 18	11/16/77	022172	03/23/82	MF

Find Number	DW SZ	Part Number	Quantity	Unit Meas.	Part Description	In/Out Status	Change Ord. Number	Date Effective	Make/Buy Part Type	PH NC	S or N
34	C	15164593	2.00	PC	RESISTOR NETWORK,10 PIN SIP	IN	022172	032382			N
13	C	24500039	1.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
~~14~~	~~C~~	~~24500063~~	~~2.00~~	~~PC~~	~~RES FXD .25W 1000 OHMS~~	~~OUT~~	022172	032382	PPP4		N
40	C	24563700	1.00	IN	INSULATION SLEEVING HIGH TEMP	IN			PPP3		N
15	A	39452200	6.00	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
38	C	52629949	36.00	IN	WIRE ELEC 30 GA WHITE	IN	039382		PPP1		N
19	A	75009901	1.00	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
20	A	75009906	1.00	PC	RESISTOR MODULE 3.3K	IN			PPP4		N
22	A	84996719	1.00	PC	CAP,CER 100V 330 PF	IN			PPP4		N
39	A	84996721	1.00	PC	CAP,CER 100V 470 PF	IN			PPP4		N
23	A	84996743	16.00	PC	CAP,CER 100V .01 MF	IN			PPP4		N
24	A	88812400	9.00	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
25	A	88880500	4.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
2	A	88880900	8.00	PC	IC 7485 TTL 4-BIT MAGN COMPAR	IN			PPP4		N
1	A	88882800	9.00	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPP4		N
11	A	88883300	9.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
3	A	88883700	6.00	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
5	A	88884100	3.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP4		N
17	A	88884200	3.00	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN			PPP4		N
16	A	88884500	5.00	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
18	A	88884600	1.00	PC	IC 74S113 SCHOTTKY TTL DUAL	IN			PPP4		N
9	A	88885100	3.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
7	A	88885200	5.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
26	A	88886200	1.00	PC	IC 82S09 TTL 576 BIT RAM	IN			PPP4		N
37	A	88896100	1.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
27	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
28	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
29	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
30	A	88897800	34.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
31	A	88918800	14.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
32	A	88920800	3.00	PC	IC 74S258 TTL QUAD 1-L SEL/MUX	IN			PPP4		N
33	A	88920900	11.00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
6	A	88922800	9.00	PC	IC 93S62/82S62 TTL PAR/GEN/CHK	IN			PPP4		N
12	A	88922900	7.00	PC	IC 74S86 QUAD 2IN EXCLUSIVE OR	IN			PPP4		N
4	A	88923000	3.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
8	A	88923100	14.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N

AA5100-1 REV 2-80 PRINTED IN U.S.A.

SCMD MFG INFO INTERDIVISIONAL DOCUMENT

INACTIVE

CONTROL DATA CORPORATION — ASSEMBLY PARTS LIST

Assembly Number	Rev	CL	DW SZ	Assembly Description	Design Source	First Usage	Release Date	Change Ord. Number	Processing Date	Page Number
96752104	B	I	D	PWA-MOS MEM I/F DATA 7FWT	DSM	CBR 18	11/16/77	022172	03/23/82	MF

Find Number	DW SZ	Part Number	Quantity	Unit Meas.	Part Description	In/Out Status	Change Ord. Number	Date Effective	Make/Buy Part Type	PH NC	S or N
10	A	88924200	9.00	PC	IC 74S253 TTL TRI-ST D 4/1 MUX	IN			PPP4		N
~~24~~	~~A~~	~~88924700~~	~~2.00~~	~~PC~~	~~RES NETWORK-SIP,8 PIN,1K OHM~~	~~OUT~~	022172	032382	PPP4		N
35	D	96740700	1.00	PC	PWB-MOS MEM INTFC (DATA)	IN			PPP4		N
36	C	96752105	REF	PC	LOGIC-MOS MEM I/F DATA 7FWT	IN			RFE4		N

NUMBER OF LINE ITEMS = 40
HIGHEST FIND NUMBER = 40

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SCMD MFG INFO INTERDIVISIONAL DOCUMENT

INACTIVE

Figure 7-8. MOS Memory Interface Data PWA (96752104) (Sheet 2 of 4)

DWN	DSS	10-5-77	CONTROL DATA	TITLE PWA MOS MEM INTFC DATA 7FW7	PREFIX DN
CHKD	B. [illegible]	10-17-77	DATA SYSTEMS LAJOLLA DIVISION		DOCUMENT NO. 96752104
ENG	[illegible]	11-[illegible]		FIRST USED ON	REV B
MFG	[illegible]	11-16-77	CODE IDENT 09132		SHEET
APPR	[illegible]				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS14992	CL A RELEASED	[illegible]	11-29-77	AW
B	DS22172	INACTIVATED REP BY 96800065	BR	4-2-82	AW

INACTIVE

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA[illegible]030

NOTES:

DETACHED LISTS

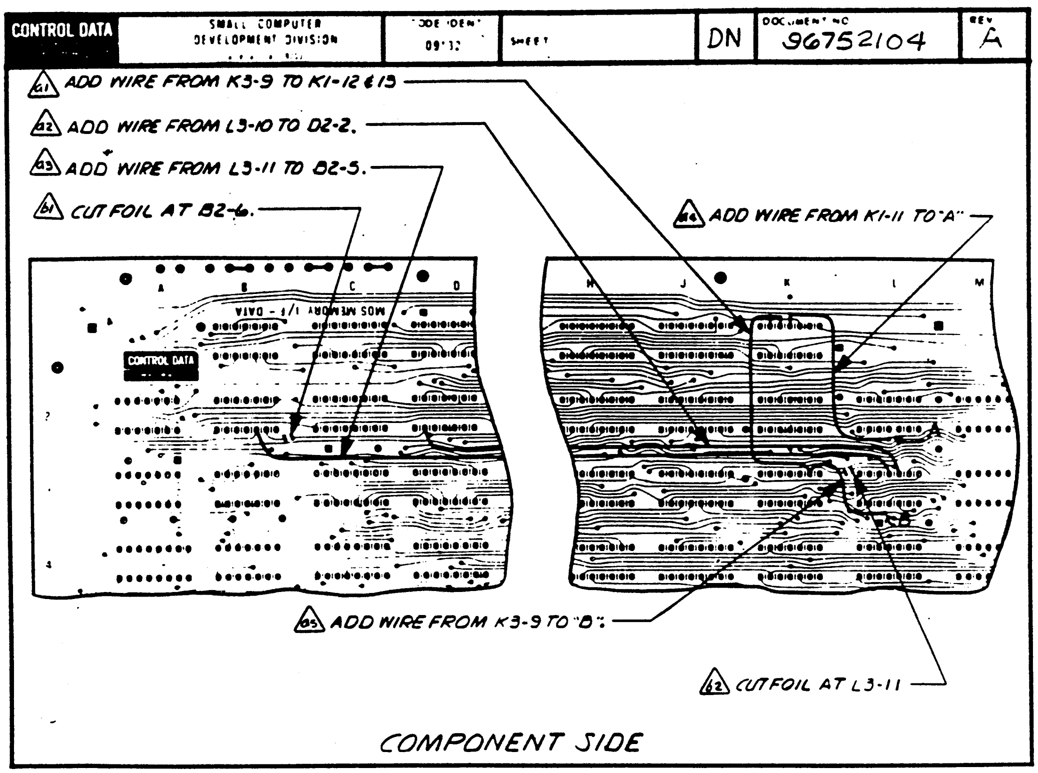
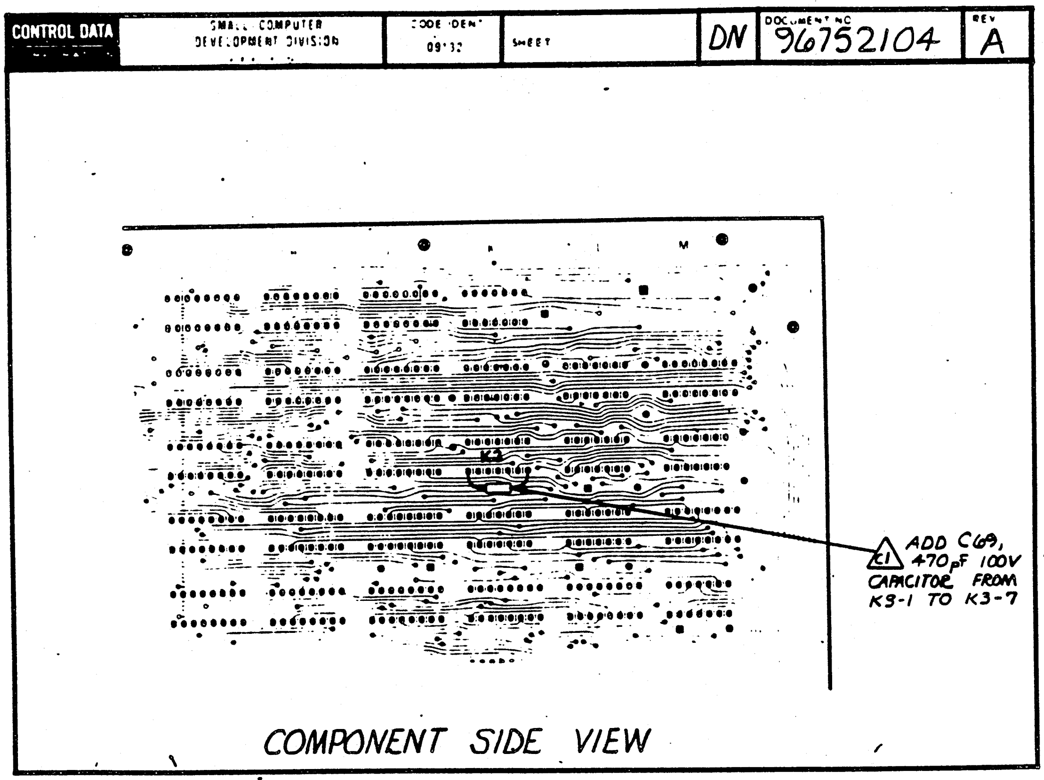


Figure 7-8. MOS Memory Interface Data PWA (96752104) (Sheet 3 of 4)



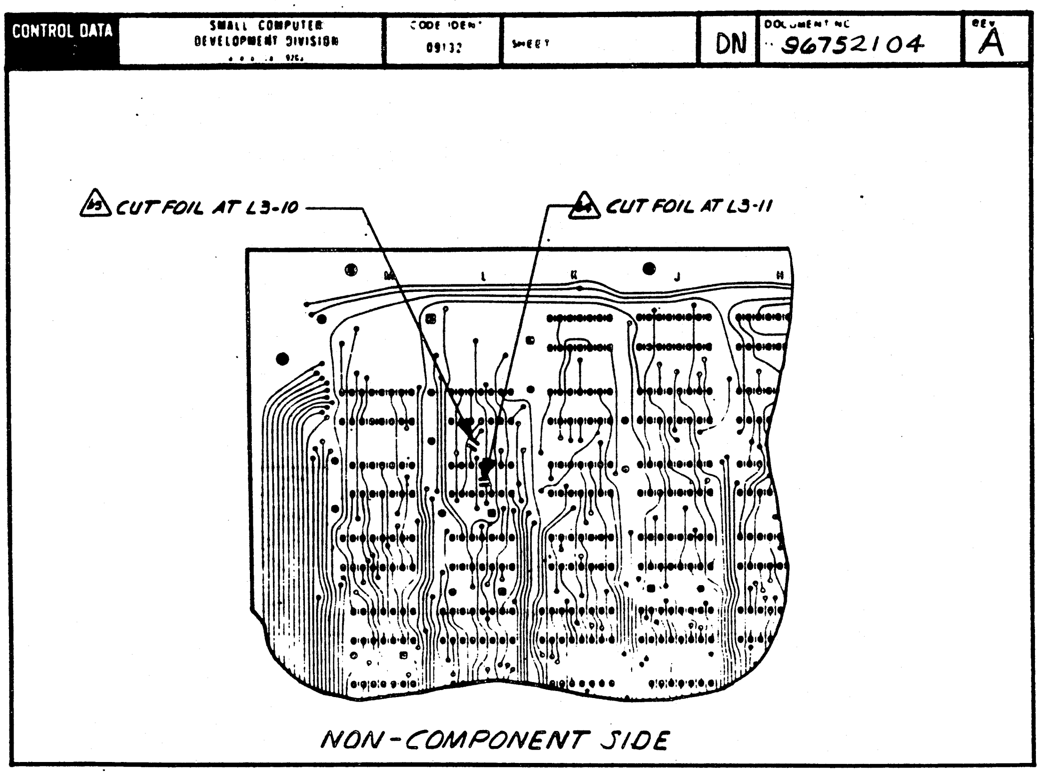


Figure 7-8. MOS Memory Interface Data PWA (96752104) (Sheet 4 of 4)

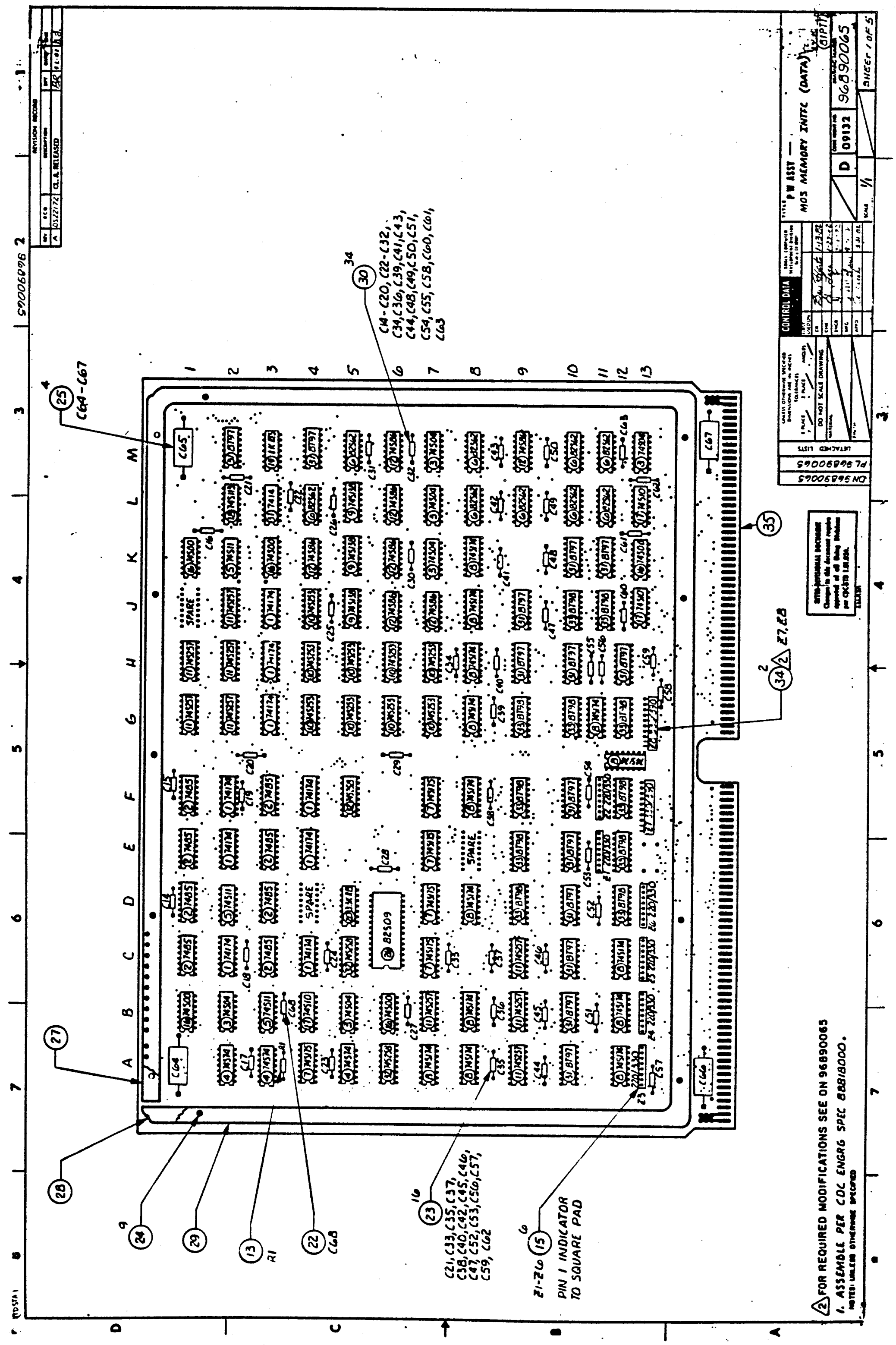


Figure 7-9. MOS Memory Interface Data PWA (96890065) (Sheet 1 of 5)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96890065	A	A	D	PW ASSY-MOS MEMORY INTF (DATA)	DS	CBR 18	03/23/82		03/23/82	2 MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PR NC	S OR N
41	C	15164593	2.00	PC	RESISTOR NETWORK,10 PIN SIP	IN					N
13	C	24500039	1.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
40	C	24563700	1.00	IN	INSULATION SLEEVING HIGH TEMP	IN			PPP3		N
15	A	39452200	6.00	PC	RES NETWORK-VOLTAGE DIVIDR-SIP	IN			PPP4		N
38	C	52629949	36.00	IN	WIRE ELEC 30 GA WHITE	IN			PPP1		N
19	A	75009901	1.00	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
20	A	75009906	1.00	PC	RESISTOR MODULE 3.3K	IN			PPP4		N
22	A	84996719	1.00	PC	CAP,CER 100V 330 PF	IN			PPP4		N
39	A	84996721	1.00	PC	CAP,CER 100V 470 PF	IN			PPP4		N
23	A	84996743	16.00	PC	CAP,CER 100V .01 MF	IN			PPP4		N
24	A	88812600	9.00	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
25	A	88980500	4.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
2	A	88880900	8.00	PC	IC 7485 TTL 4-BIT MAGN COMPAR	IN			PPP4		N
1	A	88882800	9.00	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPP4		N
11	A	88883300	9.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
3	A	88883700	6.00	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
5	A	88884100	3.00	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP4		N
17	A	88884200	3.00	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN			PPP4		N
16	A	88884500	5.00	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
18	A	88884600	1.00	PC	IC 74S113 SCHOTTKY TTL DUAL	IN			PPP4		N
9	A	88885100	3.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
7	A	88885200	5.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
26	A	88886200	1.00	PC	IC 82S09 TTL 576 BIT RAM	IN			PPP4		N
37	A	88895100	1.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
27	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
28	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
29	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
30	A	88897800	34.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
31	A	88919800	14.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
32	A	88920800	3.00	PC	IC 74S258 TTL QUAD 1-L SEL/MUX	IN			PPP4		N
33	A	88920900	11.00	PC	IC 8T98 TTL TRI-ST HEX BFR/INV	IN			PPP4		N
6	A	88922800	9.00	PC	IC 93S62/82S62 TTL PAR/GEN/CHK	IN			PPP4		N
12	A	88922900	7.00	PC	IC 74S86 QUAD 2IN EXCLUSIVE OR	IN			PPP4		N
4	A	88923000	3.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
8	A	88923100	14.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
10	A	88926200	9.00	PC	IC 74S253 TTL TRI-ST D 4/1 MUX	IN			PPP4		N

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SCMD MFG INFO

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96890065	A	A	D	PW ASSY-MOS MEMORY INTF (DATA)	DS	CBR 18	03/23/82		03/23/82	3 MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PR NC	S OR N
34	A	88924706	2.00	PC	RES NETWORK-SIP,8 PIN,1.K OHM	IN			PPP4		N
35	D	96740700	1.00	PC	PWB-MOS MEM INTFC (DATA)	IN			PPP4		N
36	C	96890066	REF	PC	LOGIC DIAG-MOS MEM INTF (DATA)	IN					N

NUMBER OF LINE ITEMS = 39
HIGHEST FIND NUMBER = 41

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SCMD MFG INFO

Figure 7-9. MOS Memory Interface Data PWA (96890065) (Sheet 2 of 5)

DWN		1-15-82	CONTROL DATA CORPORATION DATA SYSTEMS LA JOLLA DIVISION	TITLE PW ASSY- MOS MEMORY INTERFACE (DATA) 81PTT	PREFIX DN	DOCUMENT NO. 96890065	REV. A
CHKD							
ENG							
MFG			CODE IDENT 09132	FIRST USED ON		SHEET	
APPR		4-2-82					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS22172	CL. A. RELEASED	BR	4-2-82		

NOTES:

DETACHED LISTS

AA8100 REV. 8/71

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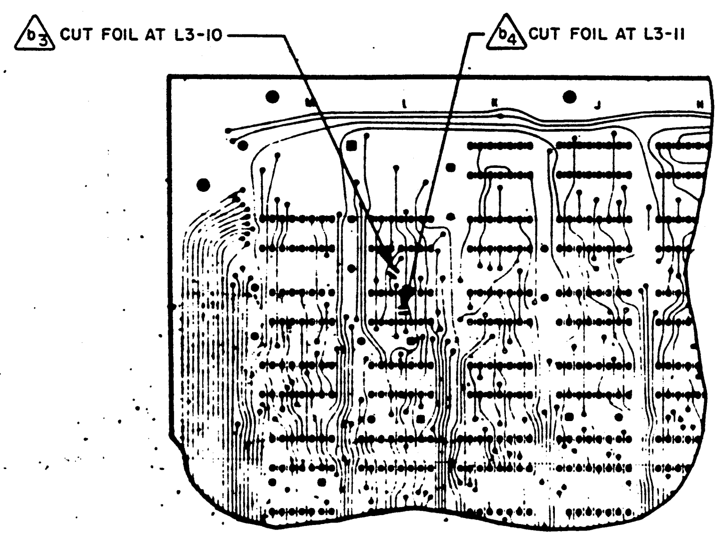
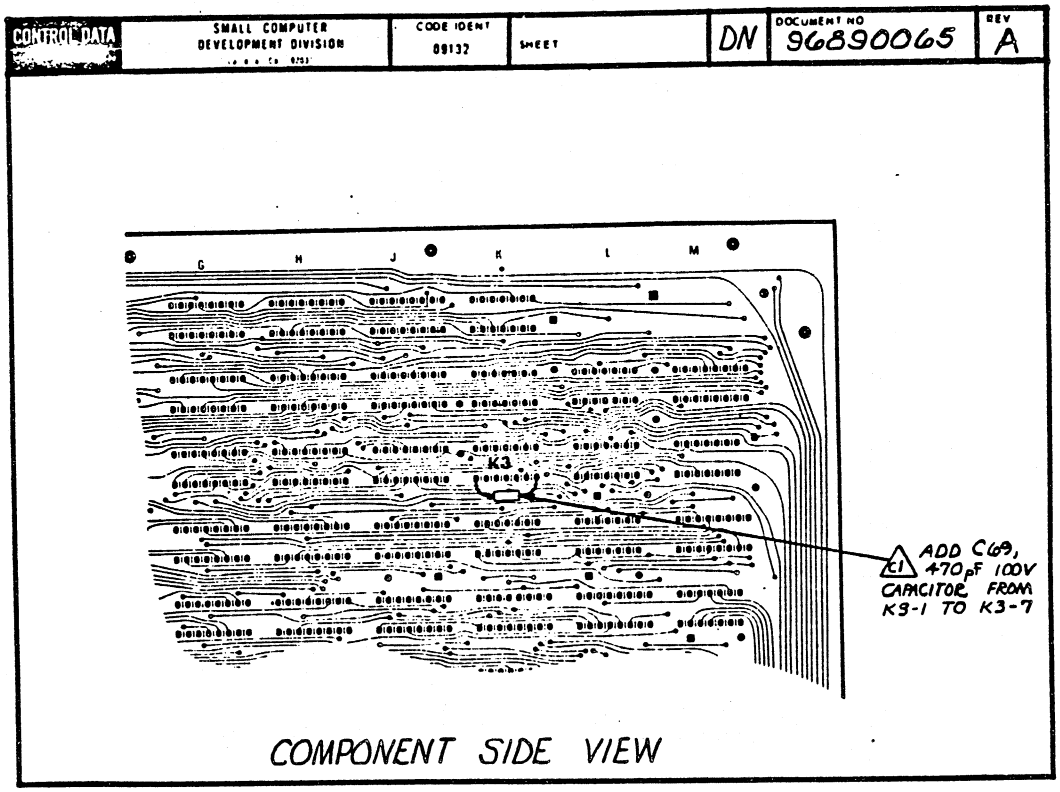
CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION	CODE IDENT 09132	SHEET	DN	DOCUMENT NO 96890065	REV A



NON-COMPONENT SIDE

Figure 7-9. MOS Memory Interface Data PWA (96890065) (Sheet 3 of 5)



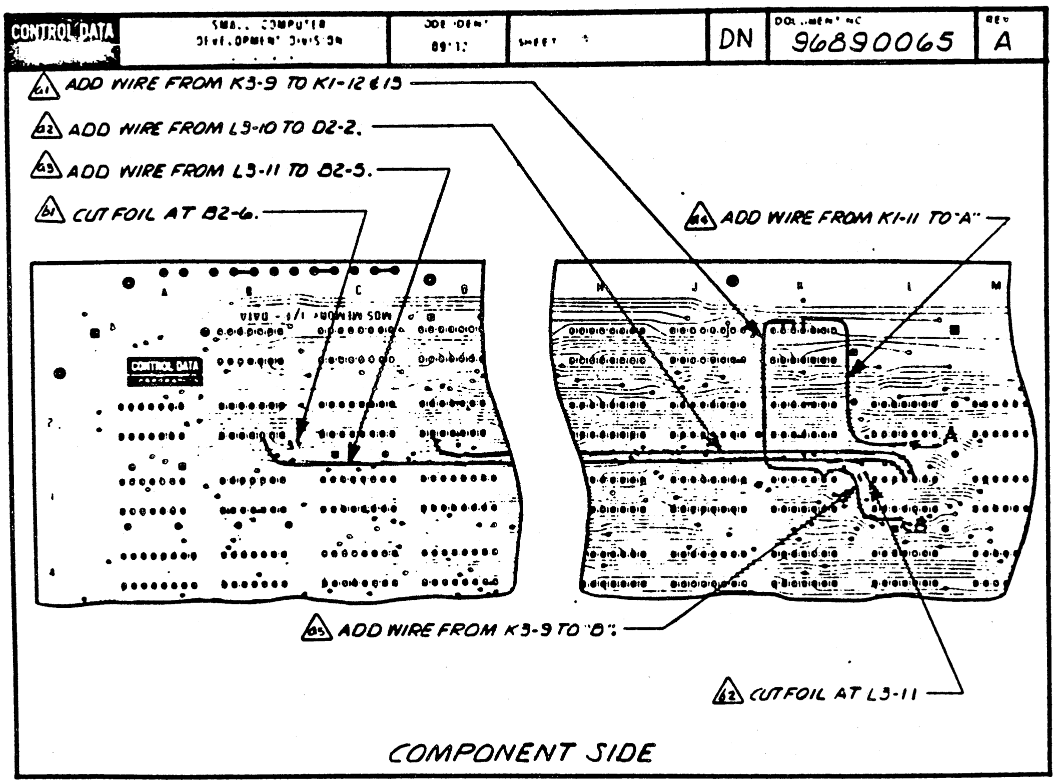


Figure 7-9. MOS Memory Interface Data PWA (96890065) (Sheet 4 of 5)

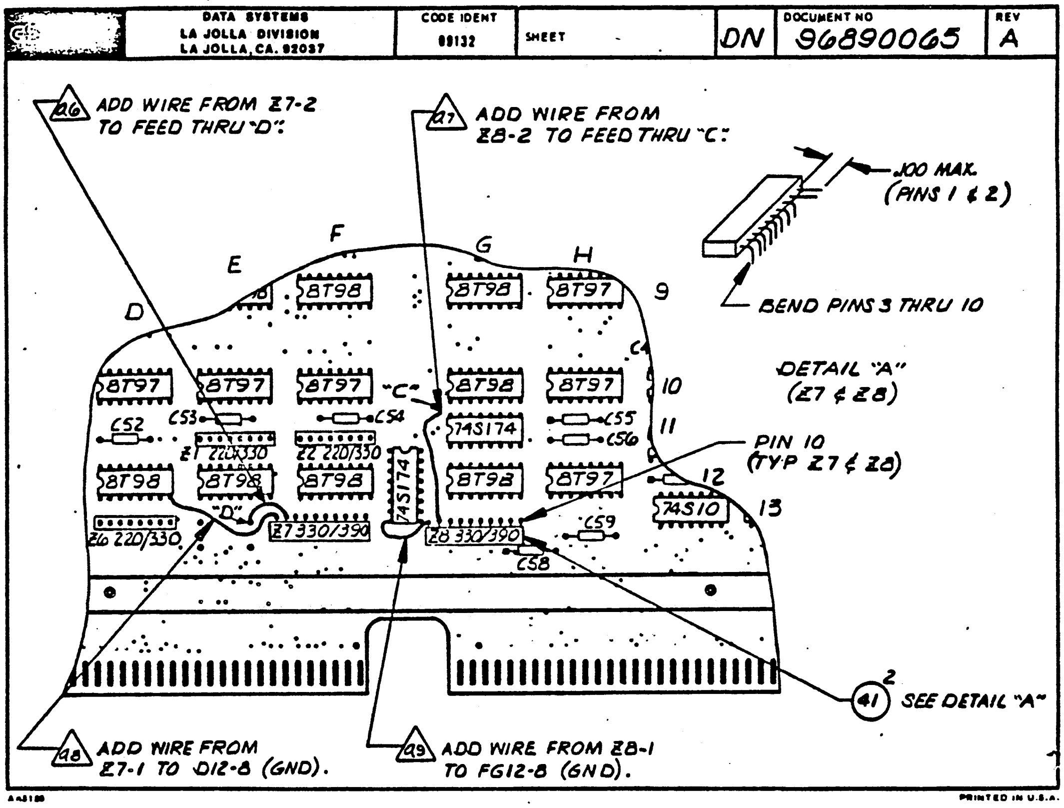


Figure 7-9. MOS Memory Interface Data PWA (96890065) (Sheet 5 of 5)

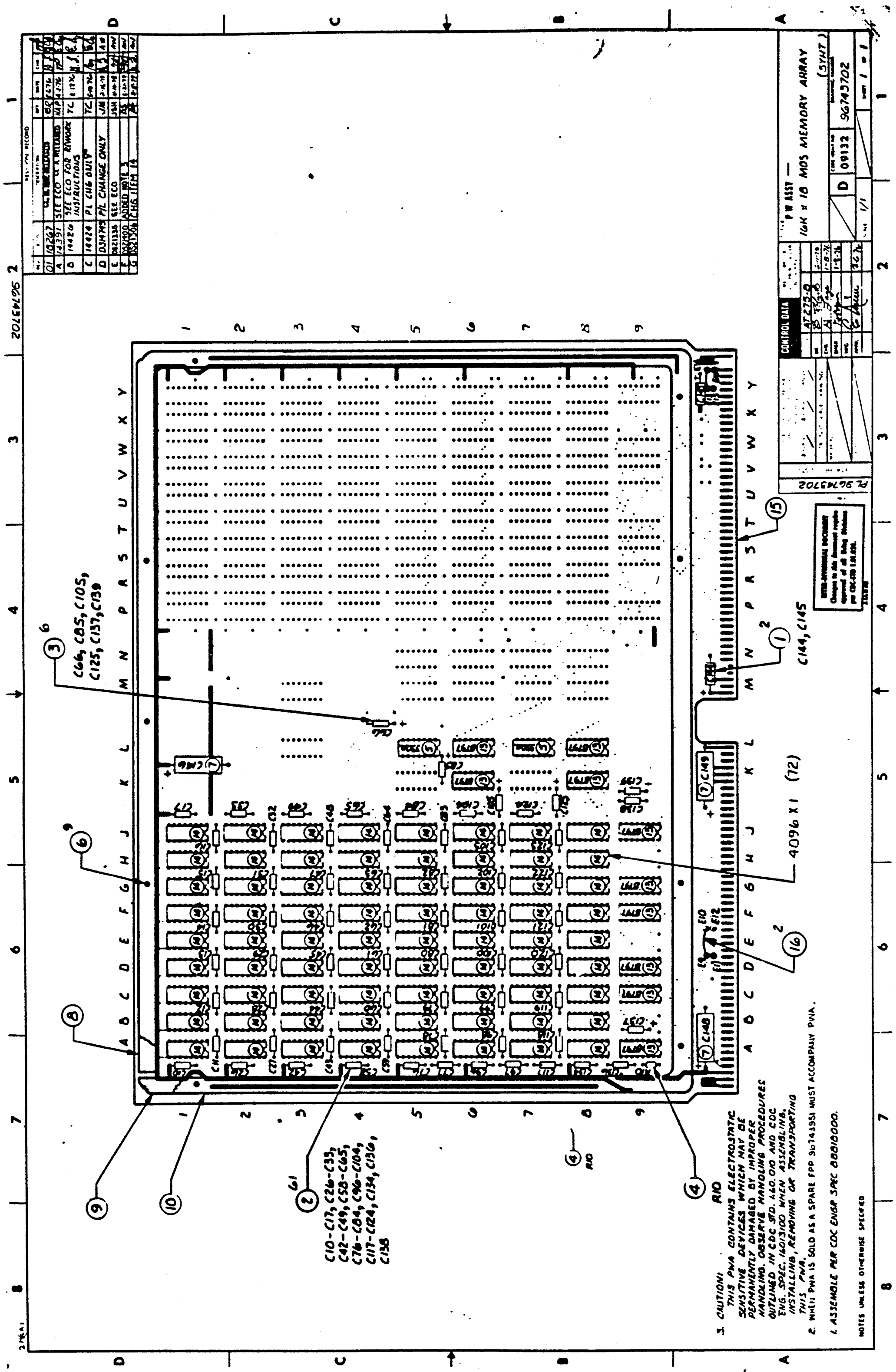


Figure 7-10. 16K MOS Memory Array PWA (96743702) (Sheet 1 of 2)

2M…

DWN	B. Roberts	12-15-75	CONTROL DATA	TITLE PW ASSY- 16K x 18 MOS MEMORY ARRAY (5YHT)	PREFIX PL	DOCUMENT NO. 96743702	REV G
CHKD	B. Fage	1-8-76	SMALL COMPUTER DEVELOPMENT DIVISION	FIRST USED ON AT275-B		SHEET	
ENG		1-8-76	CODE IDENT 09132				
MFG							
APPR		2-6-76					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	18267	CL. B. PRE-RELEASED	FR	2-6-76	
A	14391	CL. A. RELEASED	HAP	4-1-76	
B	14426	SEE ECO	TC	4-12-76	
C	14424	DELETED FN 17 (96743702)	TC	5-10-76	
D	DS14749	SEE ECO	JM	2-16-7	A.W.
E	DS21335	SEE ECO	JSH	11-13-78	AW
G	DS21381	CHG FN 14		3-5-79	AW

INTER-DIVISIONAL DOCUMENT
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AA6030

NOTES:

DETACHED LISTS

AA3188 REV. 8-71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96743702	G	A	D	PWA 16K X 18 MOS MEMORY ARRAY	DSM	MP16C	01/06/76	021381	04/06/83	1/ 1 PR

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PR NC	S OR N
~~14~~	~~A~~	~~15152700~~	~~72.00~~	~~PC~~	~~IC N-MOS RD/WRITE MEM MK4096P6~~	~~OUT~~	~~021381~~	~~072779~~	~~PPP4~~		~~N~~
14	A	15153806	72.00	PC	4096X1 DYNAM MOS RAM 210NS DIP	IN	021381	072779	PPP4		N
1	C	24504382	2.00	PC	CAP, FXD TANT 10MFD	IN			PPP4		N
4	C	24563041	1.00	PC	RES FXD COMP 1/8W 4700 OHMS	IN			PPP4		N
5	A	75009915	2.00	PC	RESISTOR PAC, 330 OHMS	IN			PPP4		N
2	A	84996743	61.00	PC	CAP,CER 100V .01 MF	IN	014749	031876	PPP4		N
7	A	88880500	3.00	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
~~12~~	~~A~~	~~88889200~~	~~8.00~~	~~PC~~	~~SOCKET-SPR,MINI .017-.019 PIN~~	~~OUT~~	~~021335~~	~~110678~~	~~PPP4~~		~~N~~
8	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
9	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
10	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
3	A	88897800	6.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
11	C	88916000	REF	PC	LOGIC DIAGRAM-5WKT	IN			RFE4		N
13	A	88918800	10.00	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
16	A	88945400	2.00	PC	JUMPER 24AWG TEF INSULATED .50	IN			AYE4		N
6	A	92030018	9.00	PC	EYELET	IN					N
15	D	96735900	1.00	PC	PWB 32K X 18 MOS MEMORY ARRAY	IN			PPP4		N
~~17~~	~~A~~	~~96762000~~	~~1.00~~	~~PC~~	~~MOS ARRAY ADDRESS CONNECTOR~~	~~OUT~~	~~014424~~	~~041576~~	~~AYM4~~		~~N~~

NUMBER OF LINE ITEMS = 18
HIGHEST FIND NUMBER = 17

SCMD MFG INFO INTERDIVISIONAL DOCUMENT

Figure 7-10. 16K MOS Memory Array PWA (96743702) (Sheet 2 of 2)

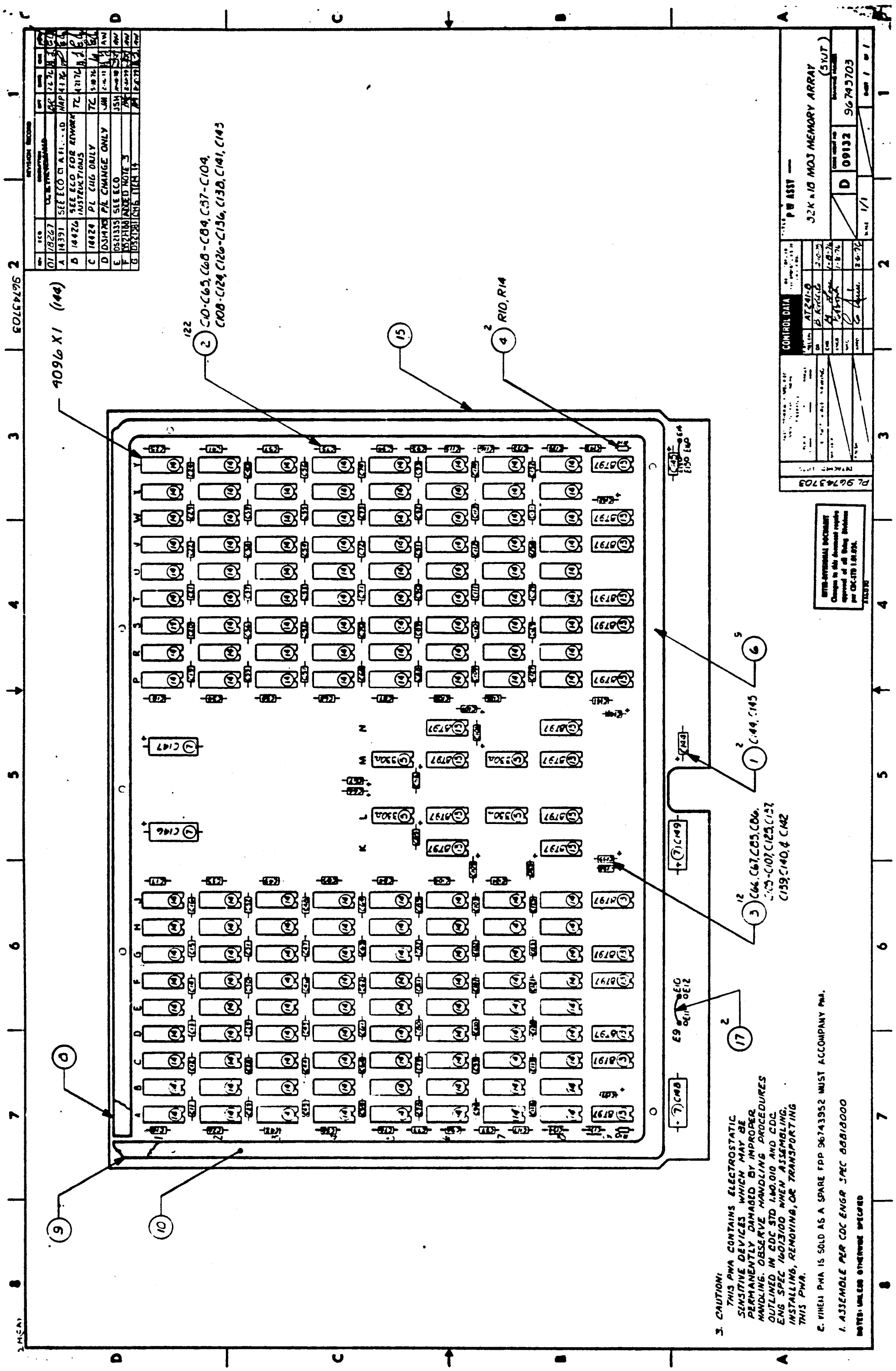

Figure 7-11. 32K MOS Memory Array PWA (96743703) (Sheet 1 of 2)

2NCA1

DWN	B. Roberts	12-5-75	CONTROL DATA	TITLE PW ASSY- 32K×18 MOS MEMORY ARRAY (5YJT)	PREFIX PL	DOCUMENT NO. 96743703	REV. G
CHKD		1-8-6	SMALL COMPUTER DEVELOPMENT DIVISION	FIRST USED ON AT241-B		SHEET	
ENG		1-8-6	CODE IDENT 09132				
MFG							
APPR		2-6-76					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	18267	CL. B PRE-RELEASED	BR	2-6-76	
A	14391	CL. A RELEASED	HAP	4-1-76	
B	14424	DELETED FN 16 96762000	TC	5-10-76	
D	DS14749	SEE ECO	JM	2-16-77	A.W.
E	DS21335	SEE ECO	JSH	11-10-78	AW
G	DS21381	CHG FN 14		3-5-79	AW

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

NOTES:

DETACHED LISTS

AA3106 REV. 8/71

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E

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96743703	G	CLA	D	PWA 32K X 18 MOS MEMORY ARRAY	DSM	MP16C	01/05/76	02/24/79	-

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PW NC	S OR N
~~14~~	~~A~~	~~15152700~~	~~14400~~	~~PC~~	~~IC N-MOS RD/WRITE MEM MK4096P6~~	~~OUT~~	~~021381~~	~~072779~~	~~PPP4~~		N
14	A	15153806	14400	PC	4096X1 DYNAM MOS RAM 210NS DIP	IN	021381	072779	PPP4		N
1	C	24504382	200	PC	CAP,FXD SOLID TANTALUM	IN			PPP4		N
4	C	24563041	200	PC	RES FXD COMP 1/8W 4700 OHMS	IN			PPP4		N
5	A	75009915	400	PC	RESISTOR PAC, 330 OHMS	IN			PPP4		N
2	A	84996743	12200	PC	CAP,CER 100V .01 MF	IN	014749	031876	PPP4		N
6	A	88812400	900	PC	RIVET-SEMI-TUBULAR,HRS .312 LG	IN			PPP4		N
7	A	88880500	400	PC	CAP-FIXED AL,16VDC,100UF	IN			PPP4		N
12	A	~~88889200~~	~~800~~	~~PC~~	~~SOCKET-SPR,MINI .017-.019 PIN~~	~~OUT~~	~~021335~~	~~110678~~	~~PPP4~~		N
8	C	88896600	100	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
9	C	88896700	100	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
10	C	88896800	100	PC	FRAME-CARD (CASTING)	IN			PPP4		N
3	A	88897800	1200	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
11	C	88915900	REF	PC	LOGIC DIAGRAM-5WGT	IN			RFE4		N
13	A	88918800	2000	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
17	A	88945400	200	PC	JUMPER 24AWG TEF INSULATED .50	IN			PPP4		N
15	D	96735900	100	PC	PWB 32K X 18 MOS MEMORY ARRAY	IN			PPP4		N
~~16~~	~~A~~	~~96762000~~	~~100~~	~~PC~~	~~MOS ARRAY ADDRESS CONNECTOR~~	~~OUT~~	~~014424~~	~~041576~~	~~AYM4~~		~~N~~

NUMBER OF LINE ITEMS = 18
HIGHEST FIND NUMBER = 17

PROJECT ENGINEER G BOWN   SCHD   INTERDIVISIONAL DOCUMENT

AA 2709-1 REV 7-75

Figure 7-11. 32K MOS Memory Array PWA (96743703) (Sheet 2 of 2)

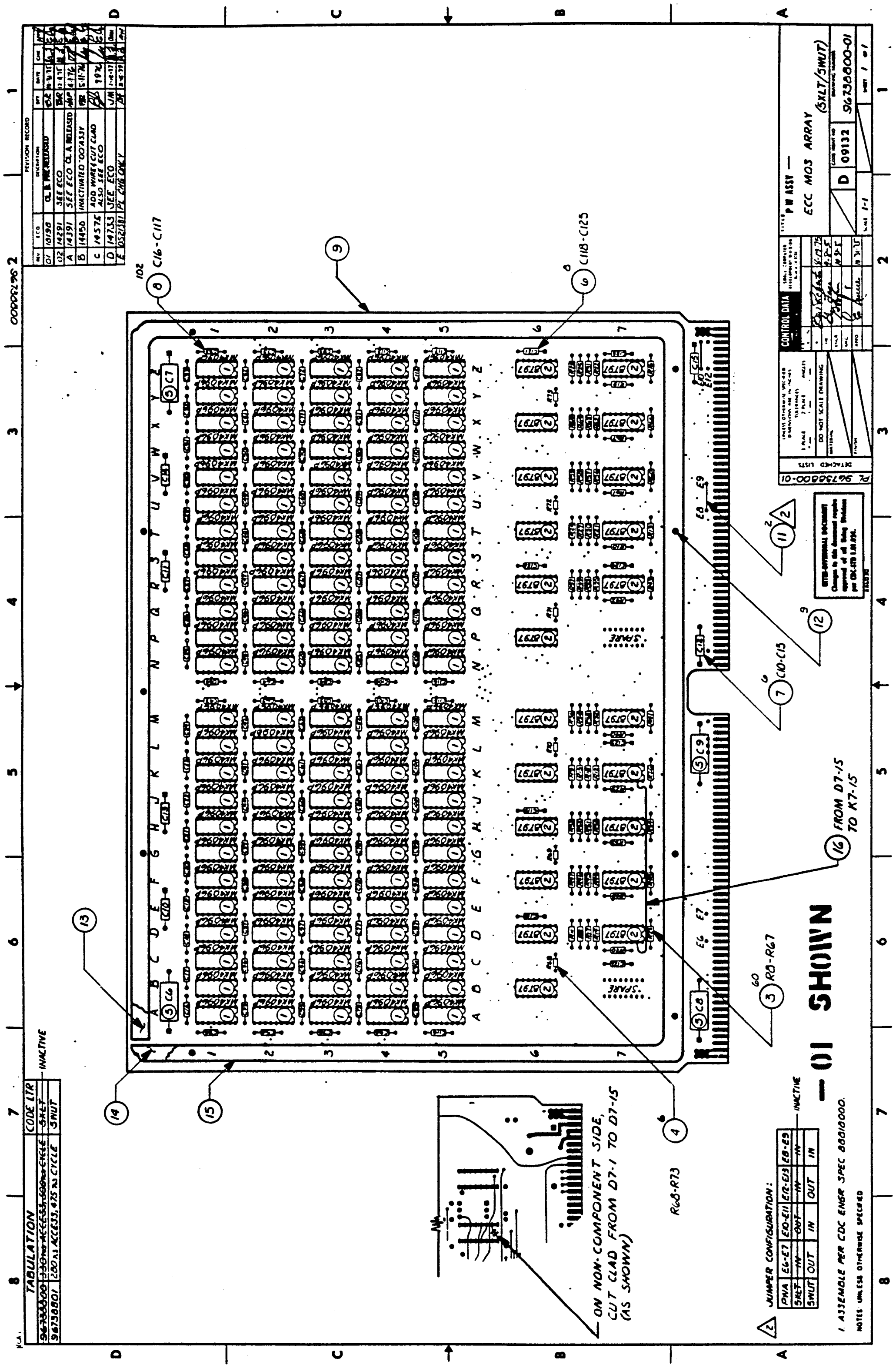

Figure 7-12. Error Checking and Correction Array PWA (96738801) (Sheet 1 of 2)

1̧CA

			CONTROL DATA	TITLE PW ASSY— ECC MOS ARRAY (5XLT/5WUT)	PREFIX PL	DOCUMENT NO 96738800-01	REV E
DWN	B. Roberts		SMALL COMPUTER DEVELOPMENT DIVISION	FIRST USED ON		SHEET	
CHKD		10-31-75	CODE IDENT 09132				
ENG		12-9-75					
MFG							
APPR		11-21-75					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	13198	CL. B. PRE-RELEASED	BR	10-31-75	
02	14291	-00 F/N 11 QTY WAS 3	BR	12-9-75	
A	14391	CL. A. RELEASED	HAP	4-1-76	
B	14450	INACTIVATED "00" ASSY	BR	5-11-76	
C	14575	SEE ECO		9-8-76	
D	14733	SEE ECO	JM	1-12-77	AW
E	DS21381	CHG FN 1		3-5-79	AW

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
AA6038

NOTES:

DETACHED LISTS

AA3100 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96738801	E	CLA	D	PWA-ECC MOS ARRAY 5WUT	DSM	MP17	09/10/75	02/24/79	

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PM NC	S OR N
16	A	15006509	600	IN	WIRE-ELEC W/W TEFZEL 30GA.WHT	IN	014575	080476	PPP1		N
~~1~~	~~A~~	~~15152700~~	~~12000~~	~~PC~~	~~IC N-MOS RD/WRITE MEM MK4096P6~~	~~IN~~	~~014575~~	~~080476~~	~~PPP4~~		~~N~~
~~1~~	~~A~~	~~15152700~~	~~12000~~	~~PC~~	~~IC N-MOS RD/WRITE MEM MK4096P6~~	~~OUT~~	~~021381~~	~~072779~~	~~PPP4~~		~~N~~
1	A	15153806	12000	PC	4096X1 DYNAM MOS RAM 210NS DIP	IN	021381	072779	PPP4		N
7	C	17706766	600	PC	CAP FIXED SOLID TANTALUM I10	IN	014391	031876	PPP4		N
3	C	24500043	6000	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
4	C	24563041	600	PC	RES FXD COMP 1/8W 4700 OHMS	IN			PPP4		N
8	A	84996743	10200	PC	CAP,CER 100V .01 MF	IN			PPP4		N
12	A	88812400	900	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
5	A	88880500	400	PC	CAP-FIXED AL,16VDC,100UF	IN			PPP4		N
13	C	88896600	100	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
14	C	88896700	100	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
15	C	88896800	100	PC	FRAME-CARD (CASTING)	IN			PPP4		N
6	A	88897800	800	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
2	A	88918800	2200	PC	IC 8T97 TTL TRI-STATE HEX BFR	IN			PPP4		N
11	A	88945400	200	PC	JUMPER 24AWG TEF INSULATED .50	IN	014575	080476	PPP4		N
9	D	96738700	100	PC	PWB-ECC MOS ARRAY	IN			PPP4		N
10	C	96738900	REF	PC	LOGIC DIAGRAM-ECC MOS ARRAY	IN			RFE4		N

NUMBER OF LINE ITEMS = 18
HIGHEST FIND NUMBER = 16

PROJECT ENGINEER KEN JOHNSON   SCMD   INTERDIVISIONAL DOCUMENT

AA 2700-1 REV 7-73

Figure 7-12. Error Checking and Correction Array PWA (96738801) (Sheet 2 of 2)

COMMENT SHEET

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COMPANY: ____________________

STREET ADDRESS: ____________________

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